Cl **33** *SC* **33.2.5.3** *P* **55** *L* **52** # 3

Jones, Chad Cisco

Comment Type **E** *Comment Status* **X** *Editorial*

There were complaints about this text in Manchester, trying to make it better: "In the presence of an offset voltage up to Vos max and an offset current up to Ios max as specified in Table 33–5, a PSE shall accept as a valid PD detection signature a pair set within a link section with both of the following characteristics:
a) Signature resistance Rgood, and
b) Parallel signature capacitance Cgood."

SuggestedRemedy

note to comment editor: this is NOT an 'easy' bucket comment.
A pair set within a link section with the following characteristics:
a) Signature resistance Rgood, and
b) Parallel signature capacitance Cgood
c) in the presence of an offset voltage up to Vos max, as specified in Table 33–5
d) in the presence of an offset current up to Ios max, as specified in Table 33–5
shall be accepted as a valid PD detection signature by a PSE.

Proposed Response *Response Status* **W**

I would like to hear group's opinion.

See comment 179.

Cl **33** *SC* **33.1.4** *P* **22** *L* **6** # 4

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Cabling*

Maintenance Request #1271, on behalf of GEOFF THOMPSON, GRACASI S.A./LINEAR TECHNOLOGY

Move as much of the cabling specification to cabling documents as possible. (This RR was entered as a tracking mechanism for Thompson Comment #59 against P802.3REVbx/D2.0 during initial WG ballot. Resolution of this comment was given over to P802.3bt as they will have Cl 33 open.)

SuggestedRemedy

See attached sheet for proposed new text.
(http://www.ieee802.org/3/maint/requests/maint_1271.pdf, page 2)
A number of these changes have already been adopted. The two remaining changes are:
Replacing the first sentence in 33.1.4 with:
"A power system, consists of a single PSE, a single PD and the link section connecting them. A power system is
characterized as Type 1 or Type 2 by lowest type number of the PSE or PD in the system, see Table 33–1."
and replacing the first paragraph of 33.1.4.1 with (as well as changing the title of the subclause to "Cabling requirements"):
"The supply of power over the data connection is intended to operate with no additional requirements to the cabling that is
normally installed for data usage. This is approximately true but may require some further attention. Power at Type 1
power levels may be transmitted over all specified premises cabling without further restrictions. Higher power levels may
require heavier gauge conductors than are found in Class C/Category 3 cabling and (more uncommonly) in some lighter
gauge Class D or better cable. The requirements for Type 2 are met by Category 5 or better cable and components as
specified in ANSI/TIA/EIA-568-A."

Proposed Response *Response Status* **W**

Waiting for Yair to review.

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 5

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Pres: PD PI*

Maintenance Request #1274 on behalf of George Zimmerman, CME Consulting/LTC

Text in the existing standard is ambiguous and is inconsistent with terminations and usage commonly found in Ethernet equipment. The intent is to require PDs to be able to withstand application of common-mode PoE voltage. Application of 57V DC voltages in across the pins corresponding to the two pairs twisted differentially to form a balanced pair of the link segment would run a DC current across the transformer windings commonly found in BASE-T Ethernet equipment and burn them out.

SuggestedRemedy

Change: The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.
To: The PD shall withstand any common-mode voltage from 0 V to 57 V applied to any two sets of two pins at the PI indefinitely without permanent damage. The two pins in each set shall correspond to the balanced twisted wire pairs of the connected link segment.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 189, 145

Cl **33** *SC* **33.2.7** *P* **66** *L* **52** # 6

Abramson, David Texas Instruments

Comment Type **TR** *Comment Status* **X**

This comment applies to Table 33-11, item 4.

The Icon-2p value is not correct for Type 3/4 PSEs when operting over 4-pair, class 0-4. Class 0-4 PDs have no unbalance requirement and can draw their entire current over one pairset. This is not represented in item 4.

SuggestedRemedy

remove "2-pair mode" from middle row of item 4 so that it applies to both 2-pair and 4-pair mode.

Add "Class 5-8 only. See 33.2.7.4." to additional information row for bottom row of item 4.

Proposed Response *Response Status* **W**

Need to hear from group as this is my comment.

Will OBE comment 112 if accepted.

Cl **33** *SC* **33.2.4.6** *P* **41** *L* **23** # 7

Abramson, David Texas Instruments

Comment Type **TR** *Comment Status* **D** *PSE SD*

This comment applies to the "invalid" entry for the variable "PD_Signature" in the do_connection_check function.

The entry "invalid" and its definition are misleading. If a PSE does connection check with an open circuit on one pairset and something plugged in on the other pairset, it should return "Dual".

Furthermore, the connection check does not do detection, no conclusions as to whether a PD is valid or invalid (or open) should be made here, it is part of detection.

SuggestedRemedy

Remove "Invalid" option for PD_Signature varaible.
Rename PD_Signature to Signature_Type.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See comments 175, 124

Cl **33** *SC* **33.2.5** *P* **52** *L* **45** # 8

Abramson, David Texas Instruments

Comment Type **TR** *Comment Status* **D** *PSE Power*

The line:

"In any operational state, the PSE shall not apply operating power to a pair set until the PSE has successfully detected a valid signature over that pair set."

forbids turning a pairset off and back on in order to check disconnect. This behavior has consensus as something we want to allow.

SuggestedRemedy

As this is a new topic, I would like to prepare a presentation for September.

For now, add:

"Editor's note (to be removed before D2.0): This sentence needs to be addressed as it forbids turning off and on a single pairset when connected to a SS class 0-4 PD."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This is my own comment. Group to decide…

Cl **33** *SC* **33.3.8** *P* **102** *L* **36** # 9

Bennett, Ken — Sifos Technologies, In

Comment Type **TR** *Comment Status* **D** *Pres: MPS*

Item 1 in table 33-19, PD Maintain Power Signature, specifies an input resistance of 26.3k-Ohm max. The new DC MPS could enable average DC currents as low as 250uA, however the resistance requirement of 26.3k max. requires average currents on the scale of 2mA.

The 26.3k resistance requirement should be removed for Type 3 and 4 PD's so that the efficiency provided by the new DC MPS rules can be fully realized.

SuggestedRemedy

In the additional information of item 1 table 33-19, add the following:
Type 1 and Type 2 Only

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Waiting for presentation.

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **5** # 15

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *Editorial*

Table 33-3 has now become very long and narrow.

SuggestedRemedy

Table can be compacted now that DLL permutations are out. See yseboodt_Table_33_3.pdf

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.6** *P* **78** *L* **1** # 33

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *Pres: MPS*

"Editor's Note: Yair to review AC MPS for 4-pair."
Pending acceptance of AC MPS removal for Type 3+4, this note is redundant.

SuggestedRemedy

Remove note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Wait for presentation.

Cl **33** *SC* **33.2.4.7** *P* **46** *L* **5** # 39

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *PSE SD*

Finding related sub diagrams is not easy in state diagram Fig 33-9a.

SuggestedRemedy

Add figure number in the empty box of the sub state diagrams

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.7** *P* **46** *L* **26** # 40

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *PSE SD*

POWER_DENIED is a state, not a sub diagram. It should a subdiagram (dashed box) called
"Power Denied" with Figure number 33-9e.

SuggestedRemedy

Rename block and refer to Figure 9e.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **41** # 41

Yseboodt, Lennart — Philips

Comment Type **E** *Comment Status* **D** *Connection Check*

"If the voltage at the PI, on either pair set, rises above V valid max, defined in Table 33-4, the PSE shall reset
the PD by bringing the voltage at the PI below V off max, defined in Table 33-7."

Table reference is wrong.

SuggestedRemedy

Remove:
33-7 => 33-11.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change 33-7 to 33-11.

Possible OBE by comment 209.

Cl **33** *SC* **33.2.6** *P* **60** *L* **22** # 43

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *Pres: Autoclass*

"Editor's Note: Measurement method and PSE margin for Autoclass still need to be addressed."
This has been done (by adopting comment to D1.1).

See yseboodt_Autoclass_measurement_baseline_v120.pdf (July meeting)

SuggestedRemedy

Remove note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Wait for presentation.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **39** # 46

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **X** *Pres: Inrush*

"Input inrush current at startup is limited by the PSE if C_Port per pair set < 180 mF, as specified in Table 33-11."
Cport is not defined in Table 33-11

SuggestedRemedy

Cport is defined in Table 33-18. Change reference.

Proposed Response *Response Status* **W**

waiting for presentation.

Cl **33** *SC* **33.5.1.1** *P* **118** *L* **10** # 51

Yseboodt, Lennart Philips

Comment Type **E** *Comment Status* **D** *Management*

"1 = Deny 4-pair power when connection check return Dual
0 = Do not deny 4-pair power when connection check returns Dual"

Bad language.

SuggestedRemedy

"1 = Deny 4-pair power when connection check returns dual-signature
0 = Do not deny 4-pair power when connection check returns dual-signature"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 271

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **5** # 57

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Editorial*

Comment #227 D1.0 partially implemented.

SuggestedRemedy

Remove column pse_dll_capable from Table 33-3.
See yseboodt_Table_33_3.pdf

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.7** *P* **47** *L* **1** # 60

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *PSE SD*

In subdiagrams of the statemachine, we have T3 coming in without a source visible.

SuggestedRemedy

Add "pse_reset + error_condition * (mr_pse_enable = enable)" to T3 arrow.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.6.2** *P* **62** *L* **21** # 62

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *PSE Classification*

"When connected to a single-signature PD, a PSE shall classify the PD only once or both of the pair sets."

SuggestedRemedy

"When connected to a single-signature PD, a PSE shall classify the PD only once on one or both of the pair sets."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 109.

Cl **33** *SC* **33.1.4.1** *P* **23** *L* **12** # 69

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Cabling*

"Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995, and Type 3 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002"

Is inconsistent with Table 33-1 which refers to the 2002 version of ISO/IEC 11801 for Type 2.
Note: if we choose for different cable requirements between Type 2 and Type 3, we hint to the
user that these are not interoperable between Type 2 and Type 3. Probably not what we want.

SuggestedRemedy

TF to discuss how to make consistent.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **38** # 71

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Editorial*

IPort-2P is also per pair set
original text:
"IInrush-2P
Output current per pair set during POWER_UP (see Table 33-11 and Figure 33-13).
IPort-2P
Output current (see 33.2.7.6)."

SuggestedRemedy

"IPort-2P
Output current per pair set (see 33.2.7.6)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We need to be careful. We should not change the Type 1/2 State Diagram variables if we are going to leave that diagram as is. We need to create new variables for Type 3/4.

Group to discuss.

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **5** # 72

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *Pres: Types*

A Type 4 PSE is distinct from a Type 3 PSE in ways other than power (Vpse min, polarity, must implement 4P).
A Type 4 PSE that is powering below class 7 should still be a Type 4 PSE.
Currently Table 33-3 requires a Type 4 PSE to have class_num_events = 5, possibly restricting it to Class 7 and 8.

(This is an updated version of the comment against D1.0).

Presentation on this topic "Type 4 Classrange"

SuggestedRemedy

Add class_num_events 1, 2 and 4 also for Type 4.

Proposed Response *Response Status* **W**

Waiting for Presentation

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **41** # 76

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Connection Check*

For connection check, first we say:
"In addition, only tests that result in a voltage at the PSE PI that is below V valid (max) as specified in Table 33-4 shall be used to
determine whether a single-signature or dual-signature is attached to the two pair sets in the link section."

And then:
"If the voltage at the PI, on either pair set, rises above V valid max, defined in Table 33-4, the PSE shall reset
the PD by bringing the voltage at the PI below V off max, defined in Table 33-7."

Since it is not allowed to use voltages > Vvalid(max), we do not need to define this.

SuggestedRemedy

Remove:
"If the voltage at the PI, on either pair set, rises above V valid max, defined in Table 33-4, the PSE shall reset
the PD by bringing the voltage at the PI below V off max, defined in Table 33-7."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Just because the voltage is in the valid range when the PSE makes it's decision, does not mean that the voltage never left that range. For example, if a PD got plugged in during the CC and the PSE figure out the correct answer in the 2nd half of the CC.

Cl **33** *SC* **33.2.7** *P* **66** *L* **33** # 77

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **X** *PSE Power*

Tpud value is TBD. [Table 33-7, Item 1b].

SuggestedRemedy

Tdelay-2P = 80ms
Tinrush-2p = [50ms - 75ms]
Therefore a T_pud = 4ms seems reasonable.

Proposed Response *Response Status* **W**

I would like to hear the group's thoughts on this.

Cl **33** *SC* **33.3.7.4** *P* **97** *L* **6** # 80

Yseboodt, Lennart Philips

Comment Type **T** *Comment Status* **D** *Editorial*

"At any static voltage at the PI, c lass 6 or class 8 PDs in ..."
Extra space in 'c lass'.

SuggestedRemedy

Change to 'class'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 64.

Cl **33** *SC* **33.2.7** *P* **69** *L* **28** # 84

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Power*

Note 1:
"The total port current of both pairs of the same polarity shall not exceed P Type /V Port_PSE = 0.5*(P Type /V Port_PSE_2P)*(1+a)
+ 0.5*(P Type /V Port_PSE_2P)*(1-a), where a is the effect of system end to end pair to pair resistance/current unbalance that
is not specified in the standard explicitly."

Note 1 has a few problems:
- it contains a shall, which is not appropriate for a note
- a is undefined
- it puts an additional total current restriction that would require a PSE to maintain a dynamically levered current limit over the two pairsets
- The total maximum current according to this note is exactly enough to deliver PType which leaves no margin to set the current cut-off in certain classes.

SuggestedRemedy

Replace the note by:
"In a compliant system, under normal operating conditions, the total current of pairs with the same polarity will not exceed Ptype/Vport_pse-2P =
(Icon_2P_unb) + (2*Icon_2P - Icon_2P_unb)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

I would like to hear group's opinion.

The note definitely cannot have a shall in it.

See comment 244, 230

Cl **33** *SC* **33.2.7** *P* **70** *L* **54** # 85

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power*

Description of the new T_pud value is needed.

SuggestedRemedy

Add a new section 33.2.7.x "Pair set power up delay".
Content:
"A PSE that will power a single signature PD using both pairsets shall transition both pair sets to
the POWER_UP state with a maximum delay of T_pud between the transition of the first pair set to POWER_UP and
the transition of the second pair set to POWER_UP."

Proposed Response *Response Status* **W**

See comment 77.

Cl **33** *SC* **33.2.7.5** *P* **72** *L* **48** # 87

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

"POWER_UP mode occurs on each pair set between the PSE's transition to the POWER_UP state on that
pair set..."
transition to the POWER_UP state is not correct

SuggestedRemedy

'transision to the POWER_ON state'

Proposed Response *Response Status* **W**

PROPOSED REJECT.

POWER_UP is correct.

Cl **33** *SC* **33.2.6** *P* **76** *L* **33** # 88

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Power*

CommentID: LEN1
Nearly every variable in Table 33-11 has a corresponding description in the sections following the table.
PType does not. With the addition of the new Types (3 and 4) we now need a definition that makes sense.

SuggestedRemedy

Insert a section with number 33.2.7.12 "Type power" and bump up the following section numbers.
Content:
"P_Type (min) is the minimum power a PSE must support to enable the highest class that a PSE of that Type can support.
Type 3 PSEs are not required to support P_Type if they are restricted to class 5 power or lower.
Type 4 PSEs are not required to support P_Type if they are restricted to class 7 power or lower."

"Type 4 PSEs shall not source more power than P_Type max as specified in Table 33-11 for a duration longer than 1 second."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See comment 98

Cl **33** *SC* **33.2.6** *P* **77** *L* **33** # 89

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *Pres: MPS*

"The PSE shall monitor either the DC MPS component, the AC MPS component, or both."

There is no need for Type 3/4 PSEs to support multiple MPS mechanisms as this wastes power.

SuggestedRemedy

Baseline in yseboodt_baseline_mps_ac_v100.pdf (or updated version).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Wait for presentation.

Cl **33** *SC* **33.3.5** *P* **87** *L* **3** # 90

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *4PID*

"A Type 3 or Type 4 dual-signature PD shall present a valid detection signature on the unpowered pair
** in order to receive 4-pair power from Type 3 and Type 4 PSEs **."

The part of the sentence in ** ** seems to indicate that Type 3/4 PDs can 'reject' 4P power by showing an invalid
signature on the unpowered pair. This extra statement weakens the 'shall' and reduces clarity.

SuggestedRemedy

Strike the part of the line between ** and **.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.5.2** *P* **91** *L* **12** # 91

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PD Classification*

Table 33-16a does not have a row for Type 3 / CLass 0 PDs.
There is no reason to disallow this.

SuggestedRemedy

Add row with following values:
PD Type, Class, class_sig_A, class_sig_B
3, 0, 0, 0

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7** *P* **94** *L* **5** # 92

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PD Power*

Table 33-18 currently lists two different parameter descriptions for Pclass_PD:
0-5 + 7 says "Input average power, Class x"
6 + 8 says "Input guaranteed available average power, Class y"

This was done to enable extended power, because the original wording implicitly forbids exceeding the input average power.
Extended power is only allowed for PDs in Class 6 or 8, this is mentioned several times in later normative text.
The word 'guaranteed' may be confusing (are the others not guaranteed?)

SuggestedRemedy

Solution 1:
- We keep a distinction between 'extended' and 'normal' classes also in Table 33-18
- Strike the word 'guaranteed' in Table 33-18 for Class 6 and Class 8
- Editor to update section 33.3.7.2 also (remove 'guaranteed')

Solution 2:
- Remove distinction between 'extended' and 'normal' classes in Table 33-18
- Extended power rules do NOT change, only allowed for Class 6+8!
- Relabel parameter for Item 4/Pclass_PD for ALL classes to:
"Input available average power, Class x"
- Editor to update section 33.3.7.2 also (remove 'guaranteed')

Solution 3:
- No changes.

Commenters preference is solution 2.

Proposed Response *Response Status* **W**

I would like to hear group's opinion on their preffered solution.

Would OBE comment 147.

Cl **33** *SC* **33.3.7** *P* **94** *L* **46** # 93

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PD Power*

Value of Input current transient (absolute value) (Table 33-18, item 8) is TBD for Type 3 and Type 4.

SuggestedRemedy

Since this actual value results from intrinsic properties of the PD, and because both PSE and PD need to interoperate with legacy Types, it would be almost meaningsless to have a different
value for Type 3 and 4.

Replace TBD by 4.70 for Type 3 and Type 4 (and merge with Type 1/2 line).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.6** *P* **43** *L* **8** # 94

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **X** *PSE Power*

According to this paragraph, a PSE is allowed to use the Ilim(min) of the PSE Type, regardless of
the attached PD.
Corner example: a Type 4 PSE may allow currents up to 1.9A to a Class 1 PD.
This would only happen under fault conditions obviously.

Issues:
- The channel may be incapable of supporting this current (Type 1 channel would be valid in this example)
- Can be of indefinite duration
- Would allow the PD to self-destruct with a *substantial* power budget
- Current text would even allow the PSE to mix and match, eg. T_lim from Type 1 and I_lim from Type 4.

SuggestedRemedy

Since we are now supporting much higher power, while not previously a feature, PSEs now should protect
the channel and downstream PD.

Delete the whole statement (lines 8 to 13).

Revert Type 2 text back to the original:
"When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a
Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I Con , I LIM ,
T LIM , and P Type (see Table 33-11)."

Add:
"When a Type 3 or Type 4 PSE powers a PD of lower Type (Type_PD) than its own Type (Type_PSE), the PSE
shall meet the PI electrical requirements of the PD Type (Type_PD), except for I_Con-2P, T_LIM-2P and PType
see (Table 33-11), for which the PSE shall meet the requirements of any PSE Type, Type_PD <= PSE Type <= Type_PSE.
The PSE shall use I_Con-2P, T_LIM-2P and PType parameters from the same Type.
If, based on the outcome of physical layer classification and connection check, the PD Type cannot be determined,
the PSE shall use the lowest Type the PD could be for Type_PD."

Proposed Response *Response Status* **W**

I would like to hear the group's opinion on this.

Cl **33** *SC* **33.2.6** *P* **58** *L* **12** # 95

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Classification*

"Rchan is the channel DC pair loop resistance."
Needs to be updated for 2P and 4P.

SuggestedRemedy

"Rchan is the channel DC loop resistance."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.6.3** *P* **64** *L* **45** # 97

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *Pres: Autoclass*

There is no specification on how a PSE is to measure the power consumed during Autoclass.

SuggestedRemedy

See yseboodt_Autoclass_measurement_baseline_v120.pdf (July meeting)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Wait for presentation

Cl **33** *SC* **33.2.7** *P* **65** *L* **44** # 98

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D**

"33.2.7 Power supply output
PSE behavior conforms to the state diagrams in Figure 33-9, Figure 33-9 continued, and Figure 33-10.
When the PSE provides power to the PI, it shall conform with Table 33-11."

We need to comply with LPS (Limited Power Supply) requirements.
To that effect we have introduced P_Type max for Type 4 at 99.9W
This alone is not enough and we need to introduce a normative statement.

If comment LEN1 is adopted, this comment is OBE.

SuggestedRemedy

Insert at the end of 33.2.7 (Power supply output):
"Type 4 PSEs shall not source more power than P_Type max as specified in Table 33-11 for a duration longer than 1 second."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment 88

Cl **33** *SC* **33.2.7** *P* **66** *L* **33** # 99

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PSE Power*

Page 74, line 15 says:
"Power shall be removed from the pair set of a PSE before the pair set current exceeds the "PSE upperbound template" in Figure 33-14."

This essentially allows a PSE to disconnect 1 pairset from a PD that is in over-current. This over-current will then instantly be carried by the remaining pairset, causing high thermal stress.

We cannot expect that a PSE can synchronize the shutdown of two pair sets perfectly,as this would preclude separate controllers, but we should
specify the maximum time and try to limit thermal stress on the PD and PSE as much as possible.

SuggestedRemedy

Add the following line to Table 33-11:

1c, "Power down delay between pair sets for single-signature PDs, T_pdd, s, , TBD, (3,4), See 33.2.7.TBD, 33.2.7.5

I would prefer a value of 6ms for T_pdd (=Tlim for Type 4), TF to discuss.

Add a new section to explain item 1c (after the Tpud section):
"A PSE that is powering a single signature PD of class 5 or higher and turns a pair set off, shall turn the remaining pair set off within T_pdd of turning off the first pair set."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add the following line to Table 33-11:

1c, "Power down delay between pair sets for single-signature PDs, T_pdd, s, , TBD, (3,4), See 33.2.7.TBD, 33.2.7.5

Add a new section to explain item 1c (after the Tpud section):
"A PSE that is powering a single signature PD of class 5 or higher and turns a pairset off shall turn the remaining pair set off within T_pdd of turning off the first pair set."

Cl **33** *SC* **33.3.7.4** *P* **97** *L* **43** # 101

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PD Power*

Formula 33-11a describes the maximum current for PDs in class 6 or 8 and is TBD.

SuggestedRemedy

Eq 33-11a:
I_portmax = P_Class / V_PSE (Ampere)

where
I_portmax is the RMS input current
P_Class is the allocated class power as defined in 33.2.6 and Equation 33-3
V_PSE is the voltage at the PSE PI as defined in 1.4.426

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7** *P* **98** *L* **13** # 102

Yseboodt, Lennart Philips

Comment Type **TR** *Comment Status* **D** *PD Power*

"When the input voltage at the PI is static and in the range of V Port_PD defined by Table 33-18, the transient
current drawn by the PD shall not exceed 4.70 mA/ms in either polarity. This limitation applies after inrush
has completed (33.3.7.3) and before the PD has disconnected."

Refer to pair sets rather than PI.

SuggestedRemedy

"When the input voltage at the PI is static and in the range of V Port_PD defined by Table 33-18, the transient
current drawn by a single-signature PD shall not exceed 4.70 mA/us in either polarity.
A dual-signature PD shall not exceed 4.70 mA/us in either polarity per pairset in the same conditions.
This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.7.5** *P* **72** *L* **50** # 104

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Pres: Inrush*

HOLD OVER for Ken Bennett:
There is a recommendation that POWER_UP mode persist for the complete duration of TInrush in section 33.2.7.5 of the existing standard. Commensurately, there is a recommendation against using LEGACY POWER_UP in section 32.2.4.4. This is because legacy power-up can end POWER_UP mode prior to the end of PD Inrush.
The result of an early exit of POWER_UP mode is that current is not limited to the levels in figure 33-13, and inrush current could exceed expected values for a PD, potentially damaging an existing Type 1 or Type 2 PD. Type 3 and Type 4 PSE's could deliver higher currents during PD Inrush in this scenario, increasing the probability of damage to a legacy PD.
The recommendations used in the existing standard have been applied to Type 3 and Type 4 PSE's in the draft. The suggested remedy makes it a requirement for Type 3 and Type 4 PSE's. For reference, the existing text is shown below:
However, for practical implementations, it is recommended that the POWER_UP mode on a pair set persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

SuggestedRemedy

Change the text to:
However, for practical implementations, it is recommended that POWER_UP mode in Type 1 and Type 2 PSE's persist for the complete duration of TInrush-2P, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior. Type 3 and Type 4 PSE's shall remain in POWER_UP mode until the Tinrush_2P period in table 33-11 is met.

Proposed Response *Response Status* **W**

Waiting for Yair's presentation.

Cl **33** *SC* **33.2.4.4** *P* **39** *L* **6** # 105

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *Types*

HOLD OVER for Lennart Yseboodt:
A Type 4 PSE is distinct from a Type 3 PSE in ways other than power (Vpse min, polarity, must implement 4P).
We do not want to prevent Type 4 PSEs from providing also power below class 7.
Currently Table 33-3 requires a Type 4 PSE to have class_num_events = 5, possibly restricting it to Class 7 and 8.

SuggestedRemedy

Add class_num_events 1, 2 and 4 also for Type 4.

Proposed Response *Response Status* **W**

Replaced by comment #72.

Chad, please withdraw this comment.

Cl **33** *SC* **33.3.7** *P* **94** *L* **48** # 106

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

HOLD OVER for Dave Dwelley:
Table 33-18, item 9: Change to "per pair set capacitance" allows 360uF. We changed this to 180uF per Straw Poll 2 in Pittsburgh.

SuggestedRemedy

Change back to "PD capacitance"
Chair note: This is done? It's now called "PI capacitance during MDI_POWER states" and "C_port"

Proposed Response *Response Status* **W**

Wait for presentation

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **48** # 107

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **D** *PD Inrush*

HOLD OVER for Yair Darshan:
We don't want to wait 50- 75msec in Type 3 and 4 systems for Iinrush to be ended if not required due to measuring PD voltage/current/time profile by the PSE and knowing that it was ended earlier.
In some large mutiport systems time for all ports to be ON is affected by Tinrush*N. N number of ports and PSE power supply power capability and its response to dynamic load behavior.

SuggestedRemedy

To add Editor Note at the end of 33.3.7.3.
To address the following issues:
1. Shortening Tinrush if PSE has the knowledge that PD is done with its Inrush.
2. Fastening Tinrush by allowing higher Iinrush_max during Tinrush time frame to shorten Tinrush with big PD capacitors.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Yair resubmitted this comment. Chad, please withdraw this one.

Cl **33** *SC* **33.2.7.5** *P* **73** *L* **2** # 108

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

HOLD OVER for Yair Darshan:
It is usefull to allow higher Inrush current than 450mA after TBD time from POWER UP start for the following reasons:
a)Reducing dynamic stress on the MOSFET during POWER UP and
b)Reach faster startup with lower probability for startup oscilations
c) Handle different load behaviour during startup that is time dependent.

SuggestedRemedy

Add the following text after line 36.
The maximum inrush current sourced by the PSE per pair set may exceed the per pair set PSE inrush template in Figure 33–13 only TBD msec after POWER UP has started and shall not excedd ILIM-2P maximum as specified by Table 33-11 item 9.

Proposed Response *Response Status* **W**

Waiting for Yair's presentation.

Cl **33** *SC* **33.2.6.2** *P* **20** *L* **20** # 109

Johnson, Peter Sifos Technologies

Comment Type **E** *Comment Status* **D** *PSE Classification*

Typo - '...classify the PD only once or both of the pair sets.'

Replace 'or' with 'on'.

SuggestedRemedy

...classify the PD only once on both of the pair sets.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace with "classify the PD only once on a single pairset or both pairsets simultaneously."

See comment 227, 182, 62

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **52** # 111

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X** *Pres: Inrush*

legacy_powerup state variable definition.

This refers to a commonly implemented inrush behavior associated with 802.3af and many 802.3at PSE's whereby inrush is deemed completed as soon as port voltage is in a nominal range. This behavior is not recommended in 802.3at because Type-2 PSE's are allowed to set Type-2 parameters for Icut and Ilim upon the completion of inrush meaning all PD's that delay or stagger inrush loads might not experience inrush current limiting at all resulting in effective inrush currents at 684mA or higher. Type-3 and Type-4 may allow even higher inrush currents to Type-1 / Type-2 PD's if they implement the "traditional" legacy_powerup. This should be avoided.

SuggestedRemedy

legacy_powerup....

FALSE: The PSE does not support legacy power up. Type-3 and Type-4 PSEs shall use this value. It is highly recommended Type-1 and Type-2 PSEs use this value.

Proposed Response *Response Status* **W**

Wait for Yair's Inrush presentation.

Cl **33** *SC* **33.2.7** *P* **67** *L* **7** # 113

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *PSE Power*

Table 33-11, Item 4a., Icon-2P-unbal

The specified MAXIMUM value for Icon-2P-unb is actually less than Ilim_min and load currents below Ilim_min can be sourced indefinitely by a PSE according to figure 33-14, the operating current template. So Icon-2P-unbal cannot be a MAXIMUM value for PSE source current, even in a perfectly balanced system.

Are these in fact MINIMUM values? If so, then they are only applicable to one pair set and in accordance with footnote 1, the other pair must provide some value less than Icon-2P.

There is also a second problem that Icon-2P-unbal is an absolute value and not PSE voltage dependent like Icon and Pclass. This disparity undermines the benefit of specifying Icon and Pclass as formulas.

SuggestedRemedy

This is a tough one to solve given the current structure of Table 33-11.

One possibility would be to specify 'Icon' as the minimum total continuous current on all powered pair sets, noting that with Type-1 and Type-2 and perhaps certain cases of Type-3, there is only one powered pair set. In this case, the minimum for Icon is Pclass/Vport-PSE-2p regardless of pair-to-pair unbalance.

Then separately specify 'Icon-Pair-max' as the minimum total continuous current on a single pair set including effects of pair-to-pair unbalance. For 2-pair powering, this would be Icon but for 4-Pair powering, would be a formula used to compute maximum pair set current assuming Vport-PSE-2p and worst case system unbalance.

Proposed Response *Response Status* **W**

Should Icon be a total current rather than per pairset?

Cl **33** *SC* **33.2.7.4** *P* **71** *L* **27** # 114

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *PSE Power*

For Type 3 and Tyep-4 PSEs, Icon-2P as specified in Table 33-11 shall be met when there is no end to end pair-to-pair current unbalance. When end to end pair-to-pair current unbalance is present, the Icon-2P may incrase up to the value of Icon-2P-UNB...."

These sentences suggests that somehow the PSE KNOWS of the presence of end-to-end unbalance and then MAY increase Icon-2P UP TO Icon-2P-unb as a result. This is confusing and hard to interpret.

SuggestedRemedy

No replacement language is suggested at this time and the fix may require changes in Table 33-11.

If Icon were always enforced as a sum of all powered pair sets, then in terms of furnishing minimum required power (continuous output current) to a PD, there is no concern about pair-to-pair unbalance at all.

Beyond this, any means by which a PSE escalates Icon-2P to Icon-2P-unb needs to be clarified. For example, a PSE could 'KNOW' that pair-to-pair unbalance should be considered following a Single Signature connection check. Conversely, a Dual Signature PD with dissimilar class signatures might exempt the PSE from Icon-2P-unb escalation.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Need to discuss this as a group. Should Icon be a total current?

Cl **33** *SC* **33.2.7** *P* **69** *L* **28** # 115

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **D** *PSE Power*

1 The total port current to both pairs of the same polarity shall not exceed PType/Vport_PSE = 0.5*(PType/Vport_PSE_2P)*(1+a) + 0.5*(Ptype/Vport_PSE_2P)*(1-a), where a is the effect....

This is not a true. A PSE may furnish up to Ilim-2P_min continously according to Figure 33-14, the operating current template. Ilim-2P_min is greater than 0.5*(PType/Vport_PSE_2P) that really represents the minimum required output power of a PSE port operating at Vport_PSE-2P_min.

SuggestedRemedy

The solution here depends on any structural changes to Icon-2P and Icon-2P-unb that might be forthcoming.

One option is to simply remove the footnote altogether.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

I know Yair and Jean are working on a new figure for Type 4 that would address this.

Cl **33** *SC* **33.2.7.4a** *P* **72** *L* **17** # 116

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **D** *Unbalance*

...The sum of the current of all pairs with the same polarity shall not exceed Pclass/VPSE.....

This statement is not true. At the PSE interface, current can continously be sourced up to the value of Ilim_min-2P as shown in Figure 33-14, the operating current template. Pclass/VPSE is the minimum required current capacity at the PSE interface given a particular Pclass_PD.

Also, "VPSE" is not a defined parameter in Table 33-11.

SuggestedRemedy

Remove this statement.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.5** *P* **89** *L* **1** # 117

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X** *PD Classification*

Table 33-15a

While we have improved the PSE portion of this table, the PD portion has become confusing now that it is separate. It can be simplified.

SuggestedRemedy

Replace 33-15a with:

Type	Class	Class Signature	DLL
1,3	0-3	see Table 33-16	Optional
2,3	4	see Table 33-16	Mandatory
3	5-6	see Table 33-16a	Mandatory
4	7-8	see Table 33-16a	Mandatory

Remove footnote from Table 33-15a.

Remove following sentence "Type 2, Type 3, and Type 4 PDs implement...." as it is completely redundant with the table now.

Proposed Response *Response Status* **W**

I would like to hear the group's opinion on this.

Cl **33** *SC* **33A.3** *P* **153** *L* **10** # 119

Bullock, Chris Cisco Systems

Comment Type **E** *Comment Status* **D**

The section defines Intra pair resistance unbalance.....not Inter pair resistance unbalance

SuggestedRemedy

Change "Inter Pair Resistance Unbalance" to "Intra Pair Resistance Unbalance"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

I agree that this should be Intra Pair. Where did "Inter" come from?

Would OBE comment 196

Cl **33** *SC* **33.2.4.6** *P* **41** *L* **22** # 124

Bullock, Chris — Cisco Systems

Comment Type **TR** *Comment Status* **D** *PSE SD*

If connection check is performed prior to detection, a result of invalid will keep you from entering detection state. As such, an result of "open_circuit on one of the pair sets" should not cause an "invalid" result.

SuggestedRemedy

replace "open_circuit on one of the pair sets" to "open_circuit on both of the pair sets"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 7.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **47** # 125

Picard, Jean — Texas Instruments

Comment Type **TR** *Comment Status* **D** *PD Inrush*

The note needs some clarifications, Cport is the capacitance the PSE will see during inrush and operation.

SuggestedRemedy

Cport per pair set is the port capacitance seen by an attached PSE during startup and steady-state operation on two twisted pairs.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Cport per pair set is the port capacitance seen by an attached PSE during startup and steady-state operation on a pair set.

Cl **33** *SC* **33.1.4** *P* **23** *L* **13** # 126

Shariff, Masood — CommScope

Comment Type **T** *Comment Status* **D** *Cabling*

Comment: text incorrectly identifies ISO/IEC 11801:2002 as lacking the additional requirement on DC loop resistance, this applies to ISO/IEC 11801:1995, but not 2002. Additionally, specification does not imply which requirements link to Cat 5e and which to cat 5, or, if they are all the same.

SuggestedRemedy

rewrite as follows:

Type 2 operation requires Class D or better cabling as specified in ISO/IEC 11801:1995 with the additional requirement that channel DC loop resistance shall be 25 ohms or less. These requirements are also met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A and Category 5e or better cabling components specified in ANSI/TIA-568-C.2. Type 3 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002. These requirements are also met by Category 5e or better cable and components specified in ANSI/TIA-568-C.2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See comments 248, 160.

Cl **33** *SC* **33.1.4** *P* **22** *L* **45** # 127

Shariff, Masood — CommScope

Comment Type **T** *Comment Status* **X** *Cabling*

Baseed on initial information received from IEEE 802.3bt, the maximum current per pair studied and specified in drafts ISO/IEC TR 29125 Ed2 and TIA TSB 184-A are 1000 mA per pair with all 4 pairs powered. Repeating the work with higher currents will take a lot of time and effort.

SuggestedRemedy

Adjust the maximum Icont-2p_unb from 1087 mA to 1000 mA in the Editors note:

Type 4: Icont-2p=865mA, Icont-2p_unb=1087mA

Proposed Response *Response Status* **W**

I believe Yair is working to lower this number. I would like to hear from him.

Cl **33** *SC* **33.1.1** *P* **20** *L* **5** # 128

Shariff, Masood CommScope

Comment Type **T** *Comment Status* **X** *Cabling*

The sentence below is confusing and does not include TIA specifications.

Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling, and Type 3 operation requires ISO/IEC 11801:2002 Class D or better cabling, and a derating of the cabling maximum ambient operating temperature.

SuggestedRemedy

Rewrite the sentences as shown below:

Type 2 operation requires Class D or better cabling as specified in ISO/IEC 11801:1995 with the additional requirement that channel DC loop resistance shall be 25 ohms or less. These requirements are also met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A and Category 5e or better cabling components specified in ANSI/TIA-568-C.2. Type 3 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002. These requirements are also met by Category 5e or better cable and components

Proposed Response *Response Status* **W**

This is different from 5 other comments on the same thing (in the easy bucket). I would like to hear the group's opinion.

Cl **33** *SC* **33.A.4** *P* **153** *L* **31** # 129

Shariff, Masood CommScope

Comment Type **T** *Comment Status* **D** *Cabling*

Draft ISO/IEC TR 29125 Ed2 and TIA TSB-184-A both have 7% maximum channel pair to pair resistance unbalance values and for consistency annex 33A should reflect the same.

SuggestedRemedy

Change pair to pair DCRUNB from 7.5 % to 7 % globally including any calculations that use pair to pair resistance unbalance. Hopefully this may change the 1087 mA Rcont_2p_unb from 1087 mA to 1000 mA bringing the max current within the scope of ISO TR 29125 Ed2 and TIA TSB 184-A?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7** *P* **94** *L* **37** # 132

Darshan, Yair Microsemi

Comment Type **T** *Comment Status* **D** *PD Power*

Table 33-18 item 7:
In June we have changed eq-33-12a to be used for all classes above class 4.
We need to update Table 33-18 item 7 accordingly.

SuggestedRemedy

Table 33-18 item 7:
1. Change the row with the parameter: Peak operating power, class 5 as follows:
parameter name: Change to: Peak operating power, class 5, 6, 7 and 8.
Max value: Change from 1.11xPclass_PD to 1.05xPclass_PD
PD Type: change to 3, 4.
2. Delete the next rows of item 7 for classes 6, 7, and 8.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.4** *P* **36** *L* **49** # 133

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D**

At the system level we need to know if we have over load condition over pair set A and pair set B.
The current text says "...over at least one pair set.." means that if we know the status on pair set A it is sufficient and it is not.
What about the status of pair set B?
As a result, the variable ovld_detected text need to be updated.

SuggestedRemedy

Change from:
A variable indicating if the PSE output current over at least one pair set has been in an overload condition (see 33.2.7.6) for…"

To:
A variable indicating if the PSE output current over 1st pair-set or 2nd pair set has been in an overload condition (see 33.2.7.6) for…"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

I believe the existing text and what you are proposing mean the exact same thing.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **27** # 134

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

33.3.7.3 Input inrush current
Inrush current per pair-set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33-18, and ending before TInrush-2P min per Table 33-11. After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level.

The time point when PD Inrush is ending is not function of PSE Tinrush Timer.
It is only a function of the PD internal design that regardless of the choices it has to use Cport between 5uF to 180uF e.g. for Type 1 and 2 and load current of up to 350mA during POWERUP phase, it has to complete Iinrush within 50msec which is the number equivalent to Tinrush_min at Table 33-11 which is a PSE requirements.
See detailed analysis in darshan_01_0715.pdf,
titled: "Only PD affects PD POWERUP Tinrush max (Not the PSE Tinrush Timer).

SuggestedRemedy

See detailed analysis and updated suggested remedy in darshan_01_0715.pdf.

Change lines 26-27 from:
"Inrush current per pair set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in To:
"Inrush current per pair set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33–18, and ends when Vport_PD-2P reaches steady state within time duration TInrush-2P min per Table 33–11. After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level."
"

Proposed Response *Response Status* **W**

waiting for presentation.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **48** # 135

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

(WAS ALSO IN D1.0 COMMENT #334)
We don't want to wait 50- 75msec in Type 3 and 4 systems for Iinrush to be ended if not required due to measuring PD voltage/current/time profile by the PSE and knowing that it was ended earlier.
In some large mutiport systems time for all ports to be ON is affected by Tinrush*N. N number of ports and PSE power supply power capability and its response to dynamic load behavior.

SuggestedRemedy

Withdrawn comment #334 from D1.0.

Proposed Response *Response Status* **W**

Waiting for presentation.

Cl **33** *SC* **33.2.7.5** *P* **73** *L* **15** # 136

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

It is usefull to allow higher Inrush current than 450mA after TBD time from POWER UP start for the following reasons:
a)Reach faster startup with lower probability for startup oscilations
b)Handle different load behaviour during startup that is time dependent e.g1: Adress the issue of some PDs that turn ON full power during POWERUP. e.g.2: Supports PDs with high input capacitance to reach steady state faster.
I doesnt add any burden on PSE as PSE move from Inrush limits to ILIM any way.
See darshan_02_0715.pdf

SuggestedRemedy

Add the following text after line 36.

The maximum inrush current sourced by the PSE per pair set may exceed the per pair set PSE inrush template in Figure 33–13 only TBD msec after POWER UP has started and shall not excedd ILIM-2P maximum as specified by Table 33-11 item 9.

Proposed Response *Response Status* **W**

I asked for a presentation on this for July. Is there one?

Cl **33** *SC* **33.3.7** *P* **94** *L* **48** # 137

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

Table 33-18 item 9: Cport_min.
The current values may not adress the need to keep the same transient voltage requirements as in Type 2 etc for Type 3 and 4.
Cport-2P_min need to be defined for Type 3 and 4 in the following way:
If Type 1/2 Cportmin=5uF
than for SS PD:
Type 3 needs total 4P input capacitance 10uF.
Type 4 needs 20uF 4P input capacitance 10uF.
Dual Signatture PD will need:
Type 3: 5uF per pair set.
Type 4: 10uF per pair set

I addition Cport meaning need to be specified in a clear way.
(There are two possible interpretations for 33.3.7.3 lines 39-40 and Note in line 47-48 that try to define what is Cport.)
See details in darshan_04_0715.pdf : Table 33-18 item 9 Cpd_min value for Type 3 and 4.

SuggestedRemedy

Make the following updates for Table 33-18 item 9 and related text per page 5 of darshan_04_0715.pdf

Proposed Response *Response Status* **W**

Wait for presentation

Cl **33** *SC* **33.2.4.4** *P* **35** *L* **45** # 138

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

There is missing word "only" in the text:
The text "This variable is provided for PSEs that (only)monitor the per pair set voltage output and use that information ....".

The above text should match lines 46-47 that do use the word "only" which is the correct intent:
lines 46-47 says:
Using only the PI pair set voltage information may be insufficient..."

SuggestedRemedy

Repalce The text "... for PSEs that monitor the per pair set voltage output and use that information ...."
with:
"... for PSEs that monitor only the per pair set voltage output and use that information ...."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Yair, if we add the word only, then this variable would not apply to PSEs that use more than the output voltage. Thus, your PSE would not be allowed to leave inrush early. I don't think this is what you want.

Cl **33** *SC* **33.3.7.3** *P* **90** *L* **43** # 139

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Inrush*

The following comment adresses Iinrush in Table 33-11 item 5a and PD Cport max to be supported by PSE Iinrush. Since both parameters aretied together, they are adressed at the same comment.
See detailes in darshan_02_0715.pdf titled: Type 3 and 4 PD Cport_max to be supported by PSE Iinrush_min.

SuggestedRemedy

1. No changes to Table 33-11 item 5a Iinrush. It is in line with the work done on September 2014.
2. For capacitance valuse for Type 3 and 4 for SS and DS PD:
see darshan_02_0715.pdf.

Proposed Response *Response Status* **W**

Waiting for presentation.

Cl **33** *SC* **33.2.7.4b** *P* **72** *L* **40** # 140

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **X** *Pres: Unbalance*

We need to complete the TBD in clause 33.2.7.4b. It adresses the test setup and test conditions for completion the infrastructure work needed for PSE PI P2PRUNB.
1. In previous drafts we add the equations needed for designing Rpair_max/min relationship in order to guarantee compliance with system E2EP2PIunb/Runb objectives (see equation 33-4b).
As we already know, E2EP2P_Iunb is function of power level and we care only for the worst case condition at maximum system operating power class level.
Due to th efact that E2EP2P_Iunb is decreased when load power is increased, we need to define equation 33-4b for each operating class.
So far we have supplied the requirements for Type 3 and Type 4 maximum power i.e. class 6 and 8 and we need to complete it for class 5 and 7 as well. This part will be addressed by expanding equation 33-4b to include requirements for class 5 and 7.
2.In order to check for compliance, we need test setup that will include Channel and PD effective resistance to ensure that the PSE under test meets the requirements. This part will be cover by Annex B which is a normative Annex.

SuggestedRemedy

Follow the details of the suggested remedy at pages 2-5 at darshan_06_0715.pdf for updated comment and suggested remedy.
The title of this presentation/attachment is:
"ANNEX 33B [Normative] PSE PI Pair-to-Pair Resistance/Current Unbalance"

Proposed Response *Response Status* **W**

waiting for presentation

Cl **33** *SC* **33.2.4.6** *P* **42** *L* **12** # 141

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D**

Existing text,
"Values:open_circuit: The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B, or by Type 3 and 4 PSEs performing detection over each pair set, if either pair set yields an open circuit."
Limits implentations that want to power one or both pair sets.

SuggestedRemedy

Replace the existing text called out with,
"Values: open_circuit: The PSE has detected an open circuit on the pair set used for detection for PSE Types that will use this information to power only on one pair set. This value is optionally returned by PSE Types performing detection using Alternative B, that will used this information to power only on one pair set. The PSE has detected an open circuit on both pair sets used for detection for Type 3 or 4 PSEs, which will use this information to power on both pair sets."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace the existing text called out with,
"Values: open_circuit: Type 1 and Type 2 PSEs performing detection using Alternative B optionally return this value if the PSE has detected an open circuit. Type 3 and Type 4 PSEs return this value if the PSE has detected an open circuit on both pairsets."

I believe the above text covers all cases and how they will be used in the state diagrams.

Cl **33** *SC* **33.2.4.7** *P* **52** *L* **19** # 142

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *PSE SD*

The Editor's note references figure 33-9, will not be modified because the Task Force decided to keep the legacy Type 1 and Type 2 PSE state diagram. Variables denny_dual_sig_4p_power and maintain_4pair_power do not exist anymore. The 4PID state diagram needs to be developed.

SuggestedRemedy

Replace the Editors note starting on line 29 and ending on line 40, with

Editor's Note: The State diagram shown in Figure 33-9(TBD) needs incorporate the 4PID requirements that is also covered in section 33.2.5.6.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See comment 260.

Cl **33** *SC* **33.2.5.6** *P* **60** *L* **12** # 143

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PSE Classification*

Dual Signature PDs may present different classification values on each pair set. Therefore, PSEs powering both pair sets need to identify the PD class to meet the PD power requested. A Dual Signature, PDs with isolated loads will need to see the classification steps to achieve mutual ID.

SuggestedRemedy

Strike the "(TBD)" in the draft sentence on line 12.

The text reads, "Subsequent to successful detection, all Type 3 and Type 4 PSEs perform classification using at least one of the following: Multiple-Event Physical Layer classification; or Multiple-Event Physical Layer classification and Data Link Layer classification. Both pair sets attached to a Dual-signature PD shall be classified by Type 3 and Type 4 PSEs that will deliver 4-pair power.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

I don't remember why we added the TBD

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 145

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **X** *Pres: PD PI*

New PD Types will need to accept up to 57V on each pair set. Fix text,
The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

SuggestedRemedy

Replace the Draft text with,
Type 1 and Type 2 PDs shall withstand any voltage from 0 V to 57 V at the powered pair set indefinitely without permanent damage. Type 3 and Type 4 PDs shall withstand any voltage from 0 V to 57 V on both pair sets indefinitely without permanent damage.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 189, 5

Cl **33** *SC* **33.3.7** *P* **94** *L* **16** # 147

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *PD Power*

The word "guaranteed" means a formal assurance that certain conditions shall be fulfilled. It is used in Table 33-18 item 4 in two places. On page 95, line 52 and on page 96 line 3.

The word was used to differentiate between average power and average power used for extended power that may be exceeded. This word has caused confusion for me and others (see Draft 1.0 #172). For example, a reader of Table 33-18 sees "Input average power, Class 5" min is 40.0 W but the next line says "Input guaranteed available average power, Class 6" min is 51.0 W. Now I am worried that the Class 5 has less commitment to the minimum value than the Class 6 minimum value, which is not the case.

The comment Editor provided this guidance for #172,
I believe this word was added as part of the Extended Power work and is needed to distinguish between those classes with extended power and those without.

I believe less confusion will result by striking the word "guaranteed". Table 33-18 already references section 33.3.7.2, which provides the sentence,

If such a PD has additional information and does not cause the PSE to source more than PClass it may exceed the maximum input guaranteed average power.

The change provides the same details. Designers that want to use extended power may uses the exception pointed out in section 33.3.7.2.

SuggestedRemedy

Strike the word "guaranteed" in all Draft locations.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment 92

Cl **33** *SC* **33.5.1.1.1** *P* **118** *L* **42** # 148

Schindler, Fred — Seen Simply

Comment Type **ER** *Comment Status* **D** *Management*

Section reference is 33.5.1.1.1a
The variable deny_dual was deleted, and referencing text should be fixed.

SuggestedRemedy

Strike the Draft referenced text.

33.5.1.1.1a Deny dual-signature PD 4-pair power
The provision of 4-pair power to dual-signature PDs by physical layer 4-pair ID shall be inhibited by setting bit 11.6 to one. Writing a one to this register bit shall set deny_dual_sig_4pair_power to true, and writing a zero to this register bit shall set deny_dual_sig_4pair_power to false.

Replace Table 33-21 bit(s) 11.6 name column with reserved and description as "Ignore when read", and R/W column as "RO".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7.6** *P* **99** *L* **48** # 150

Schindler, Fred — Seen Simply

Comment Type **TR** *Comment Status* **D** *PD Power*

New PD Types need to have their current demands constrained. The text region to be modified is,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed PClass_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after
TLIM min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current
limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current
limit meets Equation (33–14) and the voltage ramps from VPort_PSE min to VPort_PSE max at
2250 V/s.

A Type 2 PD shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 ?, and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM per Equation (33–14).

SuggestedRemedy

Replace referenced Draft text starting on line 48 with,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. Type 2, Type 3, and Type 4 PDs,
with peak power draw that does not exceed PClass_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

- The input current for Type 1 and Type 3 PDs consuming less than class-4 power levels, shall not exceed the PD upperbound template (see Figure 33-18) after TLIM min (see Table 33-11 for Type 1 and Type 3 PSEs) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33-1). The current limit meets Equation (33-14) and the voltage ramps from VPort_PSE min to

VPort_PSE max at 2250 V/s.

A Type 2, Type 3 PDs consuming more than class-4 power levels, and Type 4 PDs, shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 [ohms], and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM per Equation (33-14).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace referenced Draft text starting on line 48 with,

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. Type 2, Type 3, and Type 4 PDs, with peak power draw that does not exceed Pclass_PD max and has an input capacitance of 180 µF (TBD) or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

- The input current for Type 1 and Type 3 PDs consuming less than class-4 power levels, shall not exceed the PD upperbound template (see Figure 33-18) after TLIM min (see Table 33-11 for Type 1 and Type 3 PSEs) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33-1). The current limit meets Equation (33-14) and the voltage ramps from Vport_PSE min to Vport_PSE max at 2250 V/s.

Type 3 PDs consuming more than class-4 power levels, and Type 4 PDs, shall meet both of the following:
a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33-18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 [ohms], and a source that supports a current greater than 2.5 A.

B) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from Vport_PSE min to 56 V at 2250 V/s, the source impedance is RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM per Equation (33-14).

Cl **33** *SC* **33.4.1** *P* **104** *L* **13** # 152

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **X** *References*

Several changes were made to reference the latest IEC 62368-1 rather than IEC 60950-1 (without date). Now the standard refers to both standards. The IEC 62368-1 supersedes the old specification.

I do not know whether the sections referenced have changed. However, if they have, then it is not clear which standard the IEEE is referencing to meet the IEEE requirements. If the reference sections have not changed then the older specification is satisfactory.

SuggestedRemedy

The Task Force should review the new specification to determine if changes have been made to the IEEE referenced sections. If these sections have changed then the group should review whether the changes are acceptable for the .3BT specification. If they are then strike "IEC 60950-1 and" from the Draft.

If the IEC specifications are the same the group should decide whether referencing the new standard is necessary. More legacy IEC specifications exist than new ones. Therefore, I would prefer that the Draft strike "and IEC 62368-1".

Proposed Response *Response Status* **W**

The group needs to discuss this.

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **46** # 153

Schindler, Fred Seen Simply

Comment Type **ER** *Comment Status* **D** *PD Inrush*

The PD inrush requirements are dependent on PSE operations that are not disclosed in the PD section.

SuggestedRemedy

Add the following note above the existing note on line 46.

NOTE-PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or when PSE time Tinrush expires. See 33.2.7.4 for PSE details.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add the following note above the existing note on line 46.

NOTE-PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or when PSE time Tinrush expires. See 33.2.7.4 for details.

Cl **33** *SC* **33.5.1.1.4** *P* **119** *L* **36** # 154

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *Management*

The text,
"Setting bits 11.3:2 to '11' shall allow the PSE to use both PSE Pinout Alternative A and PSE Pinout Alternative B simultaneously."
is implentation specific. Some PSE will not power Alternatives simultaneously.

SuggestedRemedy

Strike the text "simultaneously" in the referenced sentence.

Then replace Table 33-21 11.3:2 Description, reference 11,which is "Reserved" with, "PSE pinout Alternative A and Alternative B."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.5.1.2** *P* **120** *L* **11** # 155

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *Management*

Table 33-22 does not cover all required options for new Types.
I have run out of time to provide a complete solution.

SuggestedRemedy

Add Editor's Note: Table 33-22 requires new fields to support new Types and features. Reviewers are encouraged to provide the required definitions.

Alternatively, have the Task Force provide the definitions.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add Editor's note suggested.

Cl **33** *SC* **33.3.4** *P* **86** *L* **54** # 156

Schindler, Fred Seen Simply

Comment Type **TR** *Comment Status* **D** *4PID*

The existing sentence,
"When a Type 1 or Type 2 PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power. A Type 3 or Type 4 dual-signature PD shall present a valid detection signature on the unpowered pair in order to receive 4-pair power from Type 3 and Type 4 PSEs. Any PD may indicate the ability to accept power on both pair sets using LLDP variable 4P-ID in Table 79-6b or TBD."

Does not complete address all PD Types and some text may confuse the reader.

SuggestedRemedy

Replace the sentence with,
"When a Type 1 or Type 2 PD or Type 3 or Type 4 Single Signature PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power. A Type 3 or Type 4 dual-signature PD shall present a valid detection signature on the unpowered pair. Any PD may indicate the ability to accept power on both pair sets using LLDP variable 4P-ID in Table 79-6b or TBD."

Alternatively this better option could be used,
"When a Type 1 or Type 2 PD or Type 3 or Type 4 Single Signature PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power. A Type 1 or Type 2 PD or Type 3 or Type 4 dual-signature PD shall present a valid detection signature on the unpowered pair. Any PD may indicate the ability to accept power on both pair sets using LLDP variable 4P-ID in Table 79-6b or TBD."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Looking for better language, but the following text seems to be technically correct.

Replace the sentence with,
"When a Type 1 or Type 2 PD or Type 3 or Type 4 Single Signature PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power. A Type 3 or Type 4 dual-signature PD shall present a valid detection signature on the unpowered pair. Any PD may indicate the ability to accept power on both pair sets using LLDP variable 4P-ID in Table 79-6b or TBD."

Cl **33** *SC* **33.1.4.1** *P* **23** *L* **15** # 160

Balasubramanian, Koussalya self

Comment Type **ER** *Comment Status* **D** *Cabling*

The statement "...with the additional requirement that channel DC loop resistance shall be 25ohms or less" when read along with full sentence is not clear that it applies to both Type 2 and Type 3.

SuggestedRemedy

Make "with the additional requirement that channel DC loop resistance shall be 25Ohms or less" into a separate sentence and add Type 2 and Type 3 explicitly. The new sentence would be - "The additional requirement that channel DC loop resistance shall be 25Ohms or less shall be met for Type 2 and Type 3 operation".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 126.

Cl **33** *SC* **33.2.4.6** *P* **43** *L* **8** # 163

Balasubramanian, Koussalya self

Comment Type **TR** *Comment Status* **D** *Editorial*

New variables Type_sub_PSE and Type_sub_PD are used without definition.

SuggestedRemedy

Define new variables Type_sub_PSE and Type_sub_PD.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The definition is contained within the sentence.

Cl **33** *SC* **33.2.4.7** *P* **51** *L* **2** # 165

Balasubramanian, Koussalya self

Comment Type **TR** *Comment Status* **D** *PSE SD*

Figure 33-9g starts with off page connectors A, A1 etc., - which are not defineed. We moved this figure over and called it Type 3 and 4 Class state diagram.

SuggestedRemedy

Connections A, A1 need to be defined for Figure 33-9g.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

State Diagram is being continually updated. This needs to be addressed to match the latest version.

Cl **33** *SC* **33.2.2** *P* **28** *L* **17** # 172

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **D** *Editorial*

"Figure 33–5a—10BASE-T/100BASE-TX Alternative A and Alternative B Endpoint PSE location overview"

In every other figure, we've used "4-Pair" in the title instead of "Alternative A and Alternative B."

SuggestedRemedy

Rename Figure 33-5a:

"Figure 33–5a—10BASE-T/100BASE-TX 4-Pair Endpoint PSE location overview"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 250.

Cl **33** *SC* **33.2.4.4** *P* **34** *L* **40** # 174

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **D**

Values for variable "PD_signature" do not match the values shown within the do_connection_check function (see page 41, line 14) where the variable is assigned.

SuggestedRemedy

Change the value "Invalid" to "Open_circuit" as follows:

"Open_Circuit: Open circuit detected on both pairsets."

Also, modify the value "Single" to be the default case and applicable to PDs that operate over a single pairset:

"Single: Either connection check has not been performed or a single-signature PD configuration is connected through one or both of the two pairsets at the PI."

Corresponding comment entered against the variable values within the function flagged with DW1

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Do not implement suggested remedy.

Remove "PD_Signature" from variable section since it is in the Functions section under "do_connection_check".

Cl **33** *SC* **33.2.4.6** *P* **41** *L* **17** # 175

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **D** *PSE SD*

Values for variable "PD_signature" within the do_connection_check function do not match the values shown in Section 33.2.4.4 (see page 34, line 40).

SuggestedRemedy

Delete the "Invalid" value.

Change the value "Open_circuit" as follows:

"Open_Circuit: Open circuit detected on both pairsets."

Modify the value "Single" to be the default case and applicable to PDs that operate over a single pairset:

"Single: Either connection check has not been performed or a single-signature PD configuration is connected through one or both of the two pairsets at the PI."

Corresponding comment entered against the variable values flagged with DW1

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 7.

Cl **33** *SC* **33.2.4.3** *P* **34** *L* **29** # 176

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PSE SD*

To allow for PSEs that perform connection check before, during, between, or after detection, a new constant is needed to define the disparate pathways these PSEs take through the state diagram and their associated timing requirements.

SuggestedRemedy

Add constant "PSE_CC_DET_SEQ" as follows:

PSE_CC_DET_SEQ
A constant indicating the sequence in which the PSE performs connection check and detection.
Values: 1: Connection check and detection performed simultaneously
2: Connection check performed prior to detection
3: Connection check performed between detections
4: Connection check performed after detection

Proposed Response *Response Status* **W**

Wait for presentation.

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **34** # 178

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PSE SD*

In Table 33-3a, under Additional Information for Item 2, it's stated that "Applies only when connected to a single-signature PD."

This may not be true if we allow connection check to occur between the 2 detections and don't want to create new timing parameters.

SuggestedRemedy

Presentation forthcoming to cover this and other aspects of connection check.

Proposed Response *Response Status* **W**

Wait for presentation

Cl **33** *SC* **33.2.5.3** *P* **55** *L* **52** # 179

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **D** *Editorial*

This sentence still doesn't read well. We don't need to mention the link since section 33.2.5 (see page 52, line 50) states it won't be for clarity.

SuggestedRemedy

Replace:

"In the presence of an offset voltage up to Vos max and an offset current up to Ios max as specified in Table 33–5, a PSE shall accept as a valid PD detection signature a pair set within a link section with both of the following characteristics:"

With:

"In the presence of an offset voltage up to Vos max and an offset current up to Ios max (as specified in Table 33–5), a PSE shall deem a PD detection signature valid on a pairset with both of the following characteristics:"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

We don't need to call out link section (pg. 52, line 50).

I would like to hear the group's opinion on "deem"

See comment 3.

Cl **33** *SC* **33.2.6** *P* **60** *L* **20** # 181

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **X** *PSE Power*

"A PSE may choose not to power dual-signature PDs."

This is redundant. A PSE can deny power for any reason irrespective of PD architecture.

SuggestedRemedy

Remove it.

Proposed Response *Response Status* **W**

I would like to hear group's opinion on this.

I believe this should be removed based on our 4PID compromise.

Cl **33** *SC* **33.2.6.2** *P* **62** *L* **21** # 182

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **D** *PSE classification*

Misspelling.

SuggestedRemedy

Replace:

"When connected to a single-signature PD, a PSE shall classify the PD only once or both of the pairsets."

With:

"When connected to a single-signature PD, a PSE shall classify the PD only once on both of the pairsets."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 109.

Cl **33** *SC* **33.2.7** *P* **68** *L* **46** # 183

Walker, Dylan Cisco

Comment Type **T** *Comment Status* **D** *PSE MPS*

Table 33-11, Item 17b, Max column

After rounding, the DC MPS max for the sum is not double the per pairset max of 0.005A, which looks a little strange.

SuggestedRemedy

Change 0.009 to 0.010.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The 9mA was chosen to add margin to the PD that only has to source 10mA.

Cl **33** *SC* **33.3.1** *P* **80** *L* **47** # 189

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *Pres: PD PI*

The following sentence is ambiguous:

"The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage."

SuggestedRemedy

Presentation forthcoming.

Proposed Response *Response Status* **W**

Waiting for Presentation

See comment 5, 145

Cl **33** *SC* **33.2.5** *P* **52** *L* **46** # 190

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **X** *PSE Power*

If a PSE and a single-signature PD agree to transition from 4-pair to 2-pair power via LLDP, they should be allowed to transition back to 4-pair power - again via LLDP - without redetecting as long as the other pairset has not been powered down in the interim.

SuggestedRemedy

After:

"In any operational state, the PSE shall not apply operating power to a pair set until the PSE has successfully detected a valid signature over that pair set."

Insert:

"If a PSE and single-signature PD have agreed to transition from 4-pair power to 2-pair power over LLDP, 4-pair power can subsequently be resumed via negotiation over LLDP without another detection as long as power has not been removed from the other pairset in the interim."

Proposed Response *Response Status* **W**

I would like to hear group's opinion on this.

Cl **33** *SC* **33.3.6** *P* **93** *L* **5** # 191

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **X** *PD Classification*

The following sentence seems to imply that "pse_power_level" must be set to 2, 3, or 4, but it can remain at its default value of 1.

SuggestedRemedy

Change:

"After a successful Multiple-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_level is set to either 2, 3 or 4."

To:

"After a successful Multiple-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_level may be set to either 2, 3, or 4."

Proposed Response *Response Status* **W**

I would like to hear the groups opinion as this changes the original sentence.

Cl **33** *SC* **33.5.1.1** *P* **118** *L* **10** # 192

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **D** *Management*

Table 33-21.

Bit 11.6 "Deny dual-signature PD 4-pair Power" doesn't need to exist since a PSE can deny power for any reason, irrespective of PD architecture.

SuggestedRemedy

Delete the row for bit 11.6 in Table 33-21, move bit 6 back into the Reserved range, and delete Section 33.5.1.1.1a, which describes "Deny dual-signature PD 4-pair Power".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 271.

Cl **33** *SC* **33.5.1.1** *P* **118** *L* **24** # 194

Walker, Dylan Cisco

Comment Type **TR** *Comment Status* **D** *Management*

Table 33-21, bits 11.1:0, value "10 = Force Power Test Mode"

There aren't enough encodings to specify pairset specific Force Power Test Modes, which are of value.

SuggestedRemedy

Allocate 2 of the reserved bits to create a "Force Power Test Mode Pairset Selection" field, where:

11 = Both Alternative A and Alternative B powered when Force Power Test Mode enabled
10 = Alternative B powered when Force Power Test Mode enabled
01 = Alternative A powered when Force Power Test Mode enabled
00 = Reserved

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33A** *SC* **33A.3** *P* **153** *L* **11** # 196

Walker, Dylan Cisco

Comment Type **ER** *Comment Status* **X** *Editorial*

"33A.3 Inter Pair Resistance Unbalance"

This section describes resistance unbalance within a twisted pair, not between twisted pairs.

SuggestedRemedy

"33A.3 Intra Pair Resistance Unbalance"

Proposed Response *Response Status* **W**

See comment 119.

Cl **00** *SC* *P* *L* # 197

Dwelley, David Linear Technology

Comment Type **TR** *Comment Status* **X** *PD Power*

Resubmitted comment from D1.0:

Table 33-18: Several symbols have -2p added to them. This breaks continuity with AF/AT - an AT device that claims to meet Vport_pd will not find a spec with that name anymore. New titles with "per pair set" can stay, as all valid AF/AT devices operated over a single pairset.

SuggestedRemedy

Remove -2p suffixes from Table 33-18, Items 1-3

Proposed Response *Response Status* **W**

I would like to hear the group's opinion on this.

Cl **33** *SC* **33.1.4** *P* **22** *L* **34** # 199

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Cabling*

Table 33-1 note 1: See Section 33.1.4.2. See informative annex 33A for channel pair-to-pair resistance unbalance.

Channel unbalance is important but doesn't belong in this note - this note covers Cabling Type, not cabling parameters. Section 33.1.4.1 (Cabling requirements) does belong in this note.

SuggestedRemedy

Change note 1 to: See Sections 33.1.4.1 and 33.1.4.2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.1.4** *P* **22** *L* **35** # 200

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Cabling*

Table 33-1 Note 2: "In Type 3 and Type 4 operation, the current per pair set might be impacted by pair-to-pair system resistance unbalance. See details in 33–11 item 4a"

"might" isn't strong enough, and the reference is too narrow

SuggestedRemedy

Change Note 2 to: "In Type 3 and Type 4 operation, the current per pair set will be impacted by pair-to-pair system resistance unbalance. See Section 33.2.7.4a." (fix reference when finalized)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2** *P* **25** *L* **4** # 201

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Editorial*

Note 3: "1-Event Classification of Type 3 is different from Type 1. Please refer to Table 33–10 items 11, 12 and Section 33.2.6.1
for details."

Marginal grammar, and Section 33.2.6.1, while covering 1-event classification, doesn't make any mention of the differences between Types 1 and 3

SuggestedRemedy

Change Note 3 to: "1-Event Classification differs between Types. Please refer to Table 33–10 items 11 and 12 for details."

...or add explanatory text to Section 33.2.6.1.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.1** *P* **33** *L* **41** # 202

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Editorial*

"If power is to be applied, the PSE turns on power after a valid detection in less than Tpon as specified in Table 33–11. If the PSE cannot supply power within Tpon, it initiates and successfully completes a new detection cycle before applying power."

Missing "shalls" - both of these behaviors are mandatory.

SuggestedRemedy

Change sentences to: "If power is to be applied, the PSE shall turn on power after a valid detection in less than Tpon as specified in Table 33–11. If the PSE cannot supply power within Tpon, it shall initiate and successfully complete a new detection cycle before applying power."

Proposed Response *Response Status* **W**

Not sure what to do here. This is an existing paragraph that applies to all types, so adding "shalls" seems like a bad idea. On the other hand, these are requirements and at least the one related to Tpon is not clearly spelled out in section 33.2.7.12 (but is in the state diagram).

Cl **33** *SC* **33.2.5** *P* **52** *L* **50** # 206

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Detection*

"The PSE PI is connected to a PD through a link segment."

Should be "link section"

SuggestedRemedy

Change "segment" to "section". Also, this paragraph should probably be swapped with the one above it.

Note: this is an old error from AT and may need to be submitted as a maintenance request

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This should be filed as a maintenance request.

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **7** # 207

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Connection Check*

"Type 3 and Type 4 PSEs that operate over both pair sets shall complete..."

"operate over" is somewhat ambiguous - does it mean that the PSE is about to operate over both pair sets, or that is contains hardware capable of operating over both pair sets? A PSE should not need to complete Connection Check if it is not preparing to provide 4P power.

SuggestedRemedy

Change "operate over" to "preparing to deliver 4-pair power"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change "operate over both pair sets" to "will deliver power on both pairsets"

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **16** # 208

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Connection Check*

"The connection check shall be completed before classification."

This implies that connection check should finish before classification finishes - I don't think that is what we want

SuggestedRemedy

Change sentence to: "The connection check shall be completed before classification is performed on any pairset."

This is a significant change from the existing text - we should make sure this is really what the group wants. An alternate fix would be: "The connection check shall be completed before the PSE enters POWER_UP." This is more flexible but may subject a NIC to classification voltages.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Your suggestion is what I intended when I wrote the text.

Cl **33** *SC* **33.2.5.0a** *P* **53** *L* **41** # 209

Dwelley, David Linear Technology

Comment Type **TR** *Comment Status* **D** *Connection Check*

"If the voltage at the PI, on either pair set, rises above Vvalid max, defined in Table 33–4, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, defined in Table 33–7."

This prevents operation over a 2P channel!

SuggestedRemedy

Change sentence to: "If the voltage on either pair set rises above Vvalid max, (defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, (defined in Table 33–7) before performing detection."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change sentence to: "If the voltage on either pair set rises above Vvalid max, (defined in Table 33–4) during connection check, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, (defined in Table 33–11) before performing detection."

See comment 41.

Cl **33** *SC* **33.2.5.1** *P* **55** *L* **4** # 210

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **X** *PSE Detection*

Most of the parameters in Table 33-4 are not per pair set. In general, current specs apply per pair set while voltage specs do not.

SuggestedRemedy

Remove "per pair set" in table title. Add "per pair set" to parameter 2: "Short circuit current per pair set"

Proposed Response *Response Status* **W**

I would like to hear the group's opinion on this.

Cl **33** *SC* **33.3.5.1** *P* **90** *L* **16** # 213

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PD Classification*

Table 33-16: Class 0 min is still TBD

2mA min is consistent with text on page 61 line 42

SuggestedRemedy

Replace TBD with 2mA

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

2mA seems way to high.

I recommend 1mA which would discharge the port in time.

See comment 241

Cl **33** *SC* **33.3.6** *P* **92** *L* **50** # 215

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PD Classification*

"A Type 3 PD shall identify the PSE Type as either Type 1 or Type 2 if it is class 4 PD and be able to identify the PSE Type as Type 1, Type 2, or Type 3 if it is class 5 or 6 PD."

This sentence doesn't quite say what we want it to. It would be better split into two sentences.

SuggestedRemedy

Change to: "A Type 3 Class 1-4 PD shall identify the PSE Type as either Type 1 or Type 2. A Type 3 Class 5 or 6 PD shall identify the PSE Type as Type 1, Type 2, or Type 3."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Should we also include Type 3 for class 1-4 if it detects the lcf?

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **28** # 216

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **D** *PD Power*

"After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level."

PDs are limited to power, not current, in POWER_ON mode. SS PDs are treated differently in this regard than DS PDs are.

SuggestedRemedy

Change to: "After TInrush-2P min, a single-signature PD shall not exceed the power level, Pclass_pd, corresponding to its class level."
"After TInrush-2P min, a dual-signature PD shall not exceed its per pair set power level, Pclass_pd, corresponding to the class level advertised at that pair set."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.7.6** *P* **100** *L* **8** # 217

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PD Power*

"The current limit per pair set at the MDI (MDI ILIM-2P) is defined by Equation (33–14):"

MDI should be PI

SuggestedRemedy

Replace MDI with PI through line 15

Note: this is old text from AT and may need to be submitted as a maintenance request

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This should be a maintenance request.

Cl **33** *SC* **33.3.7** *P* **94** *L* **23** # 219

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **D** *PD Inrush*

Table 33-18 item 5: This places a new inrush requirement on Type 1/2 PDs when connected to a Type 3/4 PSE - can't do this

SuggestedRemedy

Move _2p text to item 5a, add PD Type "3,4"
Restore original item 5 from AT

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is not a new requirement as we have now increased the max inrush current from 400mA total to 400mA per pairset (800 total). However, we do need to make sure this is in alighnment with the PSE inrush numbers.

If PDs are limited to 400mA per pairset, they will work with existing Type 1 and Type 2 PSEs that supply at least 400mA over a single pairset.

Cl **33** *SC* **33.3.7** *P* **94** *L* **25** # 220

Dwelley, David — Linear Technology

Comment Type **TR** *Comment Status* **D** *PD Inrush*

Table 33-18 item 6: "Inrush to operating state delay per pair set"

The per-pair-set requirement suggests a SS PD must delay until the 2nd pair set has completed inrush - an SS PD may not be able to tell

SuggestedRemedy

Move _2p text to item 6a, add new condition "Dual Signature PDs only"
Restore item 6 to original AT text.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.5.6** *P* **57** *L* **20** # 221

Dwelley, David — Linear Technology

Comment Type **E** *Comment Status* **D** *4PID*

"4PID shall be initially (TBD) determined as a logical function of the detection state of both Alternative A and Alternative B pair sets, the result..."

"Alternative A and Alternative B" are redundant here

SuggestedRemedy

Remove "Alternative A and Alternative B"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.6** *P* **58** *L* **20** # 222

Dwelley, David — Linear Technology

Comment Type **E** *Comment Status* **D** *PSE Power*

This feels like it's already been wordsmithed to death, but "supported" feels like the wrong word here

SuggestedRemedy

Change "supported" to "available" (also in Note 1).

Alternately, change to "Minimum power level the PSE must support at its output (Pclass)"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change both occurances of "supported" to "available"

Cl **33** *SC* **33.2.6** *P* **59** *L* **8** # 223

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Classification*

"A PSE shall meet one of the allowable classification permutations listed in Table 33–8."

Lennart has improved Table 33-8 immensely, but now it is virtually identical to Table 33-3.

SuggestedRemedy

Change reference to Table 33-3. Delete Table 33-8.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Table 33-3 no longer has DLL information. In addition it doesn't have Classification Type, just class_num_events.

Cl **33** *SC* **33.2.6.1** *P* **60** *L* **32** # 224

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Classification*

"The PSE shall provide to the PI VClass with a current limitation of IClass_LIM, as defined in Table 33–10 only for a pair set with a valid detection signature. Polarity shall be the same as defined for VPort_PSE-2P in 33.2.3 and timing specifications shall be as defined by Tpdc in Table 33–10."

This text appears in 33.2.6.1 but should apply to 33.2.6.2 as well

SuggestedRemedy

Move text to 33.2.6 (perhaps near page 57 line 45)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.6.2** *P* **61** *L* **5** # 225

Dwelley, David — Linear Technology

Comment Type **E** *Comment Status* **D** *PSE Classification*

"The PSE shall measure IClass and classify the PD based on the observed current according to Table 33–9."

This text appears three times in this section (lines 5, 20, and 27)

SuggestedRemedy

Remove all three lines. Add a new sentence near line 29: "In all CLASS_EVn states, the PSE shall measure IClass and classify the PD based on the observed current according to Table 33–9."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Remove all three lines and add:

"In states CLASS_EV1, CLASS_EV2, and CLASS_EV3, the PSE shall measure IClass and classify the PD based on the observed current according to Table 33–9."

at line 29.

Cl **33** SC **33.2.6.2** P **61** L **47** # 226

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Classification*

"The class events shall meet the IClass_LIM current limitation. The mark events shall meet the IMark_LIM current limitation."

This is the PSE section but these sound like PD requirements.

SuggestedRemedy

Change sentences to: "The PSE shall limit class event currents to IClass_LIM, and shall limit mark event currents to IMark_LIM."

Note: this is old text from AT and may need to be submitted as a maintenance request

Proposed Response *Response Status* **W**

PROPOSED REJECT.

These are PSE requirements on the current limit provided by the PSE.

Cl **33** SC **33.2.6.2** P **62** L **20** # 227

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Classification*

"When connected to a single-signature PD, a PSE shall classify the PD only once or both of the pair sets."

Typo, but even when fixed, the meaning is not completely clear

SuggestedRemedy

"When connected to a single-signature PD, a PSE shall classify the PD only once, using either or both of the pair sets."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment 109.

Cl **33** SC **33.2.7** P **66** L **17** # 228

Dwelley, David Linear Technology

Comment Type **TR** *Comment Status* **X** *PSE Power*

Resubmitted comment from D1.0:

Table 33-11: Several symbols have _2p added to them. This breaks continuity with AF/AT - an AT device that claims to meet Vport_pse will not find a spec with that name anymore. New titles with "per pair set" can stay, as all valid AF/AT devices operated over a single pairset.

SuggestedRemedy

Remove _2p suffixes from Items 1 and 4-10. Change Table 33-11 title to "PSE output electrical requirements per pair set for all PD classes, unless..."

Proposed Response *Response Status* **W**

I would like to hear the group's opinion on this.

Cl **33** SC **33.2.7** P **69** L **12** # 229

Dwelley, David Linear Technology

Comment Type **T** *Comment Status* **D** *Unbalance*

Table 33-11 item 20: "Current unbalance" is the old 2P AT parameter - we have two unbalance specs now.

SuggestedRemedy

Change parameter title to "Inter-pair current unbalance" to match Annex 33A-3 title

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment 119, 196.

Cl **33** *SC* **33.2.7** *P* **69** *L* **28** # 230

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **X** *PSE Power*

Note 1: "The total port current of both pairs of the same polarity shall not exceed PType/VPort_PSE = 0.5*(PType/VPort_PSE_2P)*(1+a) + 0.5*(PType/VPort_PSE_2P)*(1-a), where a is the effect of system end to end pair-to-pair resistance/current unbalance that is not specified in the standard explicitly."

"Shall" in a note is not normative.

SuggestedRemedy

Delete Note 1. Move text to section 33.2.7.4a (where Additional Information for item 4a already points) - perhaps near page 72 line 13.

Proposed Response *Response Status* **W**

See comment 84, 244

Cl **33** *SC* **33.2.7.4** *P* **71** *L* **26** # 231

Dwelley, David — Linear Technology

Comment Type **E** *Comment Status* **D** *PSE Power*

"For Type 3 and Type 4 PSEs, ICon-2P as specified in Table 33-11 shall be met when there is no end to end pair-to-pair current unbalance. When end to end pair-to-pair current unbalance is present, the ICon-2P may increase up to the value of ICon-2P-UNB as specified by Table 33-11 item 4a."

These two sentences belong in section 33.2.7.4a (which should be named 33.2.7.4.1)

SuggestedRemedy

Move two sentences to the beginning of section 33.2.7.4a. Rename section to 33.2.7.4.1 (and .4b to .4.2).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Icon specs should be in section 33.2.7.4 which is the Icon section, the other sections are unbalance sections.

Do not: implement suggested remedy.

Do: Rename section 33.2.7.4a to 33.2.7.4.1 and .4b to .4.2.

Cl **33** *SC* **33.2.7.7** *P* **74** *L* **15** # 233

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D** *PSE Power*

"A PSE may remove power from the PI if the PI current meets or exceeds..."

I believe this should be per pair set, not sum of all pairsets (which is what PI implies).

SuggestedRemedy

Change to: "A PSE may remove power from the PI if the current on a pair set meets or exceeds..."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The current draft is confusing because Icut-2p is a pairset spec and the lowerbound template in Figure 33-14 has a TBD in it, but the goal was to be able to police the PD by total power drawn (as well as per pairset). I would prefer to see the other things fixed and this left alone (or cleaned up to show the true intention).

Cl **33** *SC* **33.2.7.11** *P* **76** *L* **26** # 235

Dwelley, David — Linear Technology

Comment Type **T** *Comment Status* **D**

"33.2.7.11 Current unbalance"

We have more than one kind of current imbalance now.

SuggestedRemedy

Change title to: "33.2.7.11 Inter-pair current unbalance"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Shouldn't this be intra?

Cl **33** *SC* **33.3.7.3** *P* **96** *L* **39** # 236

Yseboodt, Lennart Philips

Comment Type **ER** *Comment Status* **D** *Pres: Inrush*

The following three statements in D1.1 are correct but highly misleading:
"Input inrush current at startup is limited by the PSE if C_Port per pair set < 180 mF, as specified in Table 33-11."
"If C Port per pair set >=180 mF, input inrush current shall be limited by the PD so that I Inrush_PD per pair set max is satisfied."
"NOTE-- C port per pair set is the C port seen by an attached PSE on two twisted pairs"

The note changes the technical meaning of the first two statements.

SuggestedRemedy

"For single-signature PDs, the input inrush current at startup is limited by the PSE if C_Port < 180 uF, as specified in Table 33-11."
"For dual-signature PDs, the input inrush current at startup is limited by the PSE if C_Port per pair set < 180 uF, as specified in Table 33-11."
"A single-signature PD with C_Port > 180uF, or a dual-signature PD with C_Port > 180uF shall limit the input inrush current
below I_Inrush_PD-2P max."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Wait for presentation

"For single-signature PDs, the input inrush current at startup is limited by the PSE if C_Port < 180 uF, as specified in Table 33-11."
"For dual-signature PDs, the input inrush current at startup is limited by the PSE if C_Port per pair set < 180 uF, as specified in Table 33-11."
"A single-signature PD with C_Port > 180uF, or a dual-signature PD with C_Port per pair set > 180uF shall limit the input inrush current
below I_Inrush_PD-2P max."

Cl **33** *SC* **33.2.6.3** *P* **65** *L* **11** # 238

Beia, Christian STMicroelectronics

Comment Type **T** *Comment Status* **X** *Autoclass*

Table 33-10a
Item 3 Autoclass margin definition has a lot of sub-cases, which may confuse the reader.
The margin seems to be quite linear with the power per pair set , so I suggest to simplify the table referring to that.

SuggestedRemedy

Replace Item 3 Autoclass marin, all rows with:

Item | Parameter | Symbol | Units | Min | Max |Additional Information
3 | Autoclass Margin, 2 pair | | % | 0.14*PType| | |
3 | Autoclass Margin, 4 pair | | % | 0.07*PType| | |

Proposed Response *Response Status* **W**

I would like to hear the group's thoughts on this.

It would definitely simplify the spec.

It is a bit confusing as the % margin is itself a % of the Ptype.

Cl **33** *SC* **33.3.8** *P* **103** *L* **34** # 239

Beia, Christian STMicroelectronics

Comment Type **T** *Comment Status* **X** *PD MPS*

Table 33-19a
A convenient way for the PD to change the MPS from Type 1,2 timings to Type 3,4 timings is to keep the same frequency of the pulses and change the duty cycle.
This was the reason why Type 3,4 TMPDO_PD was set to 318ms until Draft 1.0.
Changing it to 300ms adds design complexity to the PD.
TMPDO for type 3,4 PSE can be kept to 320ms leaving a little margin between PSE and PD specs.

SuggestedRemedy

Restore Table 33-19a, last row (Item 3, Parameter PD drop out period TMPDO_PD)

MAX: 318 ; PD Type 3,4 ; if long first class event (TLCF)

Proposed Response *Response Status* **W**

Christian and Dylan are working towards a compromise…

Cl **33** *SC* **33.2.7.7** *P* **74** *L* **17** # 240

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **X** *Pres: PSE Power Removal*

When connected to an overloaded single signature PD, it is recommended that Type 3,4 PSEs remove power from both pair sets before the current exceeds PSE upperbund template on one pair set.
This avoids increasing the turn-off time of the overloaded PD, with the additional time spent with the whole 4-pair current flowing into a single pair set.
Note that is not required that the 2 pair sets turn off together if the sum of the two turn-off times don't exceed Tcut-2P max (or the PSE upperbound template).

See presentation.

SuggestedRemedy

Add the sentence:
When connected to a single signature PD, a Type 3,4 PSE shall remove power from both pair sets before the current exceeds the "PSE upperbound template" on either pair set.

Proposed Response *Response Status* **W**

wating for presentation

Cl **33** *SC* **33.3.5.1** *P* **90** *L* **16** # 241

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **D** *PD Classification*

Table 33-16

The minimum Class 0 current for Type 3 PDs ensures the proper recognition of the mark event discharging the PD port voltage after Class event.
As a worst case, the max input PD capacitance (120nF) has to drop from Vclass max (20.5V) to Vmark_th min (10.1V) in less than Tme min (6ms).

For the PD is helpful to take some time to filter the Vmark threshold, so it is suggested to complete the discharge in less than 2ms.

The calculation gives Iclass=Cin*(Vclass-Vmark)/Tdischarge=624uA.

Choosing Iclass min=1mA, Tdischarge becomes 1.25ms, which gives extra margin to the classification timings with no added complexity.

SuggestedRemedy

Replace "TBD" in Table 33-16 line 2, column 3, with 1.00

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Will be OBE by comment 213

Cl **33** *SC* **33.2.9.1.1** *P* **77** *L* **35** # 242

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **D** *Pres: MPS*

It is very hard for a PD to swith between a condition where the AC MPS component requirements are present, to a condition where those requirements are absent. Since there is no easy way for a froze up PD to reboot, it may be convenient to take advantage of the absence of a DC MPS component.
In order to preserve legacy behavior, the new requirement is for Type3 and Type4 PSE only.
See also the relevant presentation.

SuggestedRemedy

Change the sentence:
The PSE shall monitor either the DC MPS component, the AC MPS component, or both.

With:
Type1 and Type2 PSEs shall monitor either the DC MPS component, the AC MPS component, or both.
Type3 and Type4 PSEs shall monitor the DC MPS component and shall not monitor the AC MPS component.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.8** *P* **102** *L* **26** # 243

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **D** *Pres: MPS*

It is very hard for a PD to swith between a condition where the AC MPS component requirements are present, to a condition where those requirements are absent. Since there is no easy way for a froze up PD to reboot, it may be convenient to take advantage of the absence of a DC MPS component.
In order to preserve legacy behavior, the new requirement is for Type3 and Type4 PSE only.
See also the relevant presentation.

SuggestedRemedy

Replace the text:

Powered PDs that no longer require power shall remove both the current draw and impedance components of the MPS. To cause PSE power removal, the impedance of the PI should rise above Zac2 as specified in Table 33–12

With

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove the current draw and impedance components of the MPS. To cause Type 1 and Type 2 PSE power removal, the impedance of the PI should rise above Zac2 as specified in Table 33–12

Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance component of the MPS.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Waiting for presentation.

Cl **33** *SC* **33.2.7** *P* **69** *L* **28** # 244

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **X** *PSE Power*

Table 33-11

Footnote 1:
"The total port current of both pairs of the same polarity shall not exceed PType/VPort_PSE= 0.5*(PType/VPort_PSE_2P)*(1+a)+ 0.5*(PType/VPort_PSE_2P)*(1-a), where a is the effect of system end to end pair-to-pair resistance/current unbalance that is not specified in the standard explicitly"

introduces a "shall" requirement and at the same time leaves the "a" parameter undefined. It should be just an explicative note instead.

SuggestedRemedy

Modify the footnot 1 as follows:
The total port current of both pairs of the same polarity can be calulated as PType/VPort_PSE= 0.5*(PType/VPort_PSE_2P)*(1+a)+ 0.5*(PType/VPort_PSE_2P)*(1-a), where a is the effect of system end to end pair-to-pair resistance/current unbalance that is not specified in the standard explicitly

Proposed Response *Response Status* **W**

See comment 84, 230

Cl **33** *SC* **33.3.2.6.2** *P* **64** *L* **24** # 245

Beia, Christian STMicroelectronics

Comment Type **TR** *Comment Status* **D** *PD Classification*

Table 33-10
The long finger classification timings (85ms min and 100ms max) have not changed since Draft0.4, so the TBDs can be removed

SuggestedRemedy

remove TBD from Table 33-10, item 12, column Min and column Max

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.1.4** *P* **22** *L* **34** # 247

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **D** *Cabling*

(note 2)"In Type 3 and Type 4 operation, the current per pair set might be impacted by pair-to-pair system resistance unbalance. See details in 33–11 item 4a."
The first sentence of the note gives no guidance, the column already says nominal.
Reference to 33-11 lacks proper identifier (>>Table<< 33-11), and information as to what to find there.

SuggestedRemedy

Strike "In Type 3 and Type 4 operation, the current per pair set might be impacted by pair-to-pair system resistance unbalance. "
Replace "See details in 33-11 item 4a." with
"For details on resistance unbalance effects, see Table 33-11 item 4a."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 200

Cl **33** *SC* **33.1.4.1** *P* **23** *L* **13** # 248

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *Cabling*

"Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995, and Type 3 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002, with the additional requirement that channel DC loop resistance shall be 25ohms or less. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A."

Text incorrectly identifies ISO/IEC 11801:2002 as lacking DC loop resistance requirements (this applies to ISO/IEC 11801:1995) and additionally confuses requirements for type 2 and type 3 which are now different (one is ISO 1995 one is 2002) further, the ordering of the equivalence to TIA specs is reversed from the ISO specs, adding to the confusion.

SuggestedRemedy

Rewrite as separate sentences, replacing as follows:
"Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995, with the additional requirement that channel DC loop resistance shall be 25ƒÇ or less. These requirements are also met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A. Type 3 operation requires Class D or better cabling as specified in ISO/IEC 11801:2002. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 126.

Cl **33** *SC* **33.1.4.1** *P* **23** *L* **19** # 249

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *Cabling*

"Under worst-case conditions, Type 2 and Type 3 operation requires a 10 °C reduction in the maximum ambient operating temperature of the cable when all cable pairs are energized at ICable (see Table 33–1), or a 5 °C reduction in the maximum ambient operating temperature of the cable when half of the cable pairs are energized at ICable. Additional cable ambient operating temperature guidelines for Type 2, Type 3, and Type 4 operation are provided in ISO/IEC TR 29125 [B49]1 and TIA TSB-184 [B61]"

First, we should not be specifying the installation conditions here, but rather refer to the cabling standards (TIA-TSB-184-A and the ISO TR).
Second, Does Type 2 operation, which is 2 pairs in a 4 pair sheath EVER have all cable pairs energized? isn't it half the cable pairs?

SuggestedRemedy

Replace as follows:
"Reduction in the maximum ambient operational temperature may be required for Type 2 and Type 3 operation. When half the cable pairs are energized, as is the case in 2 pair operation, a less reduction is required. For details on the effects of installation conditions and currents on cable temperature rise associated with Type 2, Type 3 and Type 4 operation, see ISO/IEC TR 29125 [B49]1 and TIA TSB-184 [B61]."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This paragraph existed before this project. All we have done is add Type 3 (and eventually 4) to it.

Furthermore, if "X" cables are used two different Type 2 PSEs might be energizing all 4 pairs in a cable.

Cl **33** *SC* **33.2.3** *P* **33** *L* **26** # 251

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *4-Pair Power*

"While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously." (strikeout)
Type 1 and Type 2 PSEs still have the striken restriction - need to rewrite rather than just strike out. Additionally, reference to 'link segment' is unneeded and inaccurate. The alternatives are the pinouts, the link section, has no pinout.

SuggestedRemedy

Reinstate as:
"While a PSE may be capable of both Alternative A and Alternative B, Type 1 and Type 2 PSEs shall not operate both Alternative A and Alternative B simultaneously. Type 3 and Type 4 PSEs may operate simultaneously on both Alternatives."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.4.1** *P* **33** *L* **45** # 253

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **D** *4-Pair Power*

"It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment."

This applies only to two-pair PSEs.

SuggestedRemedy

insert "two-pair" so it says "It is possible that two separate two-pair PSEs".

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This applies to all PSEs. Two 4-Pair PSEs could end up attached to the same cable (Alt A from one and Alt B from the other). They could still work.

This paragraph is completely informative and only explains the reason for the next paragraph.

Cl **33** *SC* **33.2.4.4** *P* **33** *L* **43** # 255

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **X** *Pres: Inrush*

"legacy_powerup:
This variable is provided for PSEs that monitor the PI per pair set voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI pair set voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed TInrush-2P period is recommended. A variable that is set in an implementation-dependent manner.
Values:TRUE:The PSE supports legacy power up; this value is not recommended.
FALSE:The PSE does not support legacy power up. It is highly recommended that new equipment use this value."

Doesn't this only apply to 2 pair PSEs? At a minimum, there should be no legacy-power-up 4pair PSEs.

SuggestedRemedy

insert "two pair" so it reads, "This variable is provided for two-pair PSEs"

Add to TRUE: (after 'not recommended'), "and is not allowed for 4-pair PSE operation."

Proposed Response *Response Status* **W**

Wait for Yair's Presentation.

Cl **33** *SC* **33.2.4.4** *P* **37** *L* **4** # 256

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *PSE SD*

"pd_dll_power_type
A control variable output by the PSE power control state diagram (Figure 33-27) that indicates the type of PD as advertised through Data Link Layer classification.
Values:1: PD is a Type 1 PD (default)
2: PD is a Type 2 PD
3: PD is a Type 3 PD
4: PD is a Type 4 PD"

A dual of this variable will be needed for mutual identification, not requiring it to be "dll". - pd_power_type.
"

SuggestedRemedy

Add Editor's note reminding that mutual identification will require a similar variable "pd_power_type", or, if mutual ID is adopted, add the variable as follows:
"pd_power_type
A control variable determined by mutual identification that indicates the type of PD."
Values:1: PD is a Type 1 PD (default)
2: PD is a Type 2 PD
3: PD is a Type 3 PD
4: PD is a Type 4 PD"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add the editor's note suggested.

We need to be careful of the type/power relationship.

Cl **33** *SC* **33.2.4.6** *P* **43** *L* **4** # 257

Zimmerman, George CME Consulting, Inc.

Comment Type **ER** *Comment Status* **D** *Editorial*

"Editor's Note: "Classification not complete" in above paragraph needs to be clear. Team to pay close attention to above paragraph during reviews."

Text doesn't refer to above text, the term does not appear in that text or has been modified. (it wasn't in 1.0 either)

SuggestedRemedy

Delete editor's note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The note should say "Mutual identification not complete". Please change the note accordingly.

Cl **33** *SC* **33.2.4.6** *P* **43** *L* **8** # 258

Zimmerman, George CME Consulting, Inc.

Comment Type **ER** *Comment Status* **D** *Editorial*

"When a PSE powers a PD of lower Type (Type_sub_PD) than its own native type (Type_sub_PSE), the PSE shall meet the PI electrical requirements of a Type 1 PSE the PD Type(Type_sub_PD), except for ICon-2P, ILIM-2P, TLIM-2P, and PType (see Table 33-11), for which the PSE shall meet the requirements of any PSE Type, Type_sub_PD <= PSE Type <= Type_Sub_PSE."

sub should indicate subscripts. also wording of "for which the PSE shall meet the requirements of any PSE Type" is odd.

SuggestedRemedy

implement subscripts indicated by _sub_

Reword requirement so that it makes sense, "for which the PSE shall select to meet the requirements of it's type or a lesser type such that Type_sub_PD<=..."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Possible OBE by comment # 94.

Cl **33** *SC* **33.2.4.7** *P* **52** *L* **30** # 260

Zimmerman, George CME Consulting, Inc.

Comment Type **ER** *Comment Status* **D** *PSE SD*

"Editor's Note: State diagram shown in figure 33-9 should include the following
1) Process to do connection check following DETECT_EVAL and prior to any classification. After connection
check set variable pd_4pair_candidate = (valid_AB)*[(PD_signature = Single) + (PD_signature =
Dual) * (!deny_dual_sig_4p_power)].
2) Set maintain_4pair_power to initial value of pd_4pair_candidate at POWER_UP state.
3) Add an additional exit condition - !maintain_4pair_power from the POWER_ON state to the POWER_
DENIED state. Change exit D from POWER_ON state to
"power_not_available*!short_detected*!
ovld_detected*tmpdo_timer_not_done*!option_vport_lim+!maintain_4pair_power".If maintain_4pair_power is false then power must be removed from at least one pair set."

Editor's note has been overtaken by other changes, needs updating to deal with deleted variables. Items 2 & 3 no longer apply, item 1 is modified.

SuggestedRemedy

Replace lines 29 to 33 with:
"Editor's Note: State diagram shown in figure 33-9 should include the following
1) Process to do connection check following DETECT_EVAL and prior to any classification. After connection check set variable pd_4pair_candidate = (valid_AB)*[(PD_signature = Single)."
(delete items 2 & 3, lines 34 to 40).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by comment # 142

Cl **33** *SC* **33.2.5.6** *P* **57** *L* **19** # 262

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **D** *4PID*

"4PID shall be initially (TBD) determined as a logical function of the detection state of both Alternative A and Alternative B pair sets, the result of connection check as described in 33.2.5.0 and the results of other system information."

mutual identification is obviously needed, and is omitted from this list of specific information.

SuggestedRemedy

add ", mutual identification" after 33.2.5.0 and before "and" to read:
"4PID shall be initially (TBD) determined as a logical function of the detection state of both Alternative A and Alternative B pair sets, the result of connection check as described in 33.2.5.0, mutual identification and the results of other system information."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.2.7** *P* **65** *L* **48** # 263

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *PSE Power*

"PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10."

This restatement of the earlier requirement needs modification to point to Type 1 and Type 2 PSEs only, and may need an additional statement for Type 3 & 4 PSEs to point to TBD state diagram.

SuggestedRemedy

Delete the redundant restatement "PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10."

Alternatively, change to read: "Type 1 and Type 2 PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10. Type 3 and Type 4 PSE behavior conforms to the state diagrams in Figures (TBD)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Delete the redundant restatement "PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10."

Cl **33** *SC* **33.2.7** *P* **66** *L* **1** # 264

Zimmerman, George CME Consulting, Inc.

Comment Type **ER** *Comment Status* **D**

"Editor's Note: Update the above sentence to reference Type 3/4 state diagram when state diagram is complete."

No need to wait if you know it needs to be done, just put in the TBDs where needed.

SuggestedRemedy

Delete editor's note.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See comment 263.

Cl **33** *SC* **33.4.9.1** *P* **113** *L* **20** # 268

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **X** *AES*

"10GBASE-T connector or telecom outlet Midspan PSE"

what is a '10GBASE-T connector'? is it the 10GBASE-T MDI connector?

SuggestedRemedy

change 'connector' to 'MDI connector'

Proposed Response *Response Status* **W**

Need someone with knowledge in this area to answer this.

Cl **33** *SC* **33.4.9.1** *P* **113** *L* **38** # 269

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **D** *AES*

"For up to 1000BASE-T operation, NEXT loss for Midspan PSE devices"

This should include 1000BASE-T, but exclude 10GBASE-T.

SuggestedRemedy

Replace "for up to 1000BASE-T operation" with "For operation with 1000BASE-T and lower rates".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.4.9.1.2** *P* **114** *L* **19** # 270

Zimmerman, George CME Consulting, Inc.

Comment Type **T** *Comment Status* **D** *AES*

"For 1000BASE-T operation, insertion loss"
should be for rates up to 1000BASE-T, inclusive.

802.3bz is expected to also use these rates, so operation other than 10G would be ok too.

SuggestedRemedy

Replace "for 1000BASE-T operation, " with "For other than 10GBASE-T operation, "

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.5.1.1** *P* **118** *L* **10** # 271

Zimmerman, George CME Consulting, Inc.

Comment Type **TR** *Comment Status* **D** *Management*

Table 33-21 (register 11), bit 6, "Deny dual-signature PD 4-pair Power"
- the variable this was supposed to set was removed, the bit is no longer needed.
Also described in 33.5.1.1.1a

SuggestedRemedy

No change needed to Table 33-21
Delete row for bit 11.6
Reinstate the reserved bits as 11.15:6
Delete new section 33.5.1.1.1a Deny dual-signature PD 4-pair power (lines 40-47)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **33.3.4** *P* **86** *L* **54** # 272

Darshan, Yair Microsemi

Comment Type **TR** *Comment Status* **D** *4PID*

The text:
"When a Type 1 or Type 2 PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs
from which it is not drawing power"

In order to maintain interoperability with all PSEs and PDs in terms of backfeed voltage that supports invalid signature on the un powered pairs specifically in SS PD, this requirements need to be applied for all PDS.

SuggestedRemedy

Change from:
When a Type 1 or Type 2 PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs
from which it is not drawing power

To
When a Single Signature PD Type 1 or Type 2 PD or Type 3 or Type 4 becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

When a Type 1, Type 2, or single-signature Type 3 or Type 4 PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power"