IEEE802.3bt 4-Pair Power over Ethernet Task Force

4P PoE systems use cases and proposed requirements

4P PoE

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Yair Darshan
Microsemi
ydarshan@microsemi.com

Microsemi

Supporters

Supporters:

George Zimmerman

Valerie Maguire / Siemon

Christian Beia / ST

Fred Schindler / SeenSimply

Ron Nordin / Panduit

Koussalya Balasubramanian / Cisco

David Tremblay / HP

David Abramson / TI

Acknowledgments:

Valerie Maguire / Siemon

Wayne Larsen / Comscope

Christian Beia / ST

Fred Schindler / SeenSimply

Rimboim Pavlik / Microsemi

David Abramson / TI

Objectives

- Part A:
- Discussing 4P PoE use cases that need to be supported and some basic system requirements

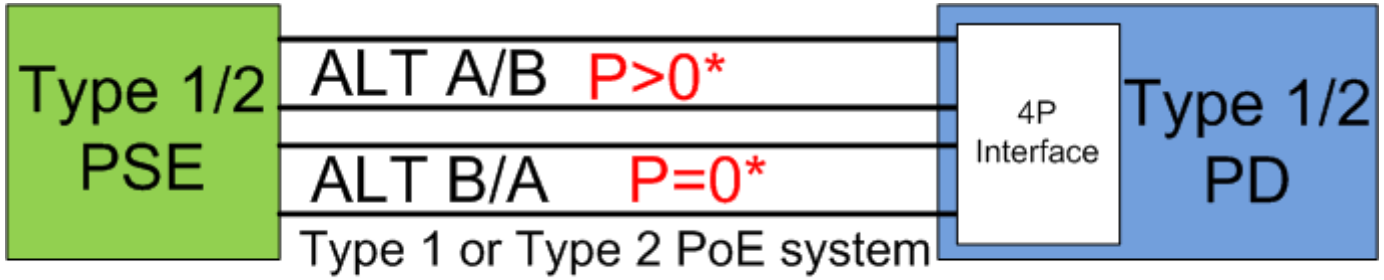
- Part B:
- To discuss a proposal for mutual Identification.

Terms and Abbreviations

- PSE: Power Sourcing Equipment, as defined in IEEE Standard 802.3
- PD: Powered Device, as defined in IEEE Standard 802.3
- ALT A/ ALT B: Alternative A or Alternative B, pairs 1-2,3-6 or pairs 4-5, 7-8, Power Channel A or Power Channel B.
- Detection: Per IEEE802.3 clause 33.1 and 33.3.5: A protocol allowing the detection of a device that requests power from a PSE. In any operational state, the PSE required not apply operating power to the PI until the PSE has successfully detected a PD requesting power. Moreover the PSE is required to turn on power only on the same pairs as those used for detection. (See Annex A)
- Mutual Identification: PSE detects PD power Type and power class which indicates maximum power that PD will need. PD detects PSE Power Type which tells the PD the PSE maximum power capability and Type.

Background - Legacy Equipment main requirements

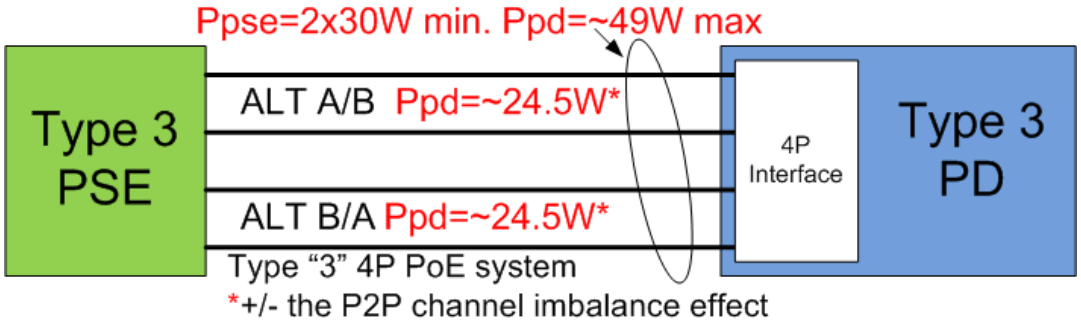
- Legacy Systems
  - PSE Type 1 (802.3af) and PSE Type 2 (802.3at)
    - A PSE is turning on power only on the same pairs as those used for detection.
    - PSE Type 2 is required to support PD Type 1 and Type 2.
  - PD Type 1 (802.3af) and PD Type 2 (802.3at)
    - PD is a 4 pair interface. It was required to work if power was delivered on Mode A (pairs 1,2-3,6) or Mode B (pairs 4,5-7,8) but was not required to work on both mods simultaneously although it is technically possible pending PD implementation.
    - Type 1 PD is backwards compatible with Type 2 PSE.
    - PD Type 2 with Type 1 power levels is supported by Type 1 PSE.
  - Mutual Identification between PSEs and PDs is required

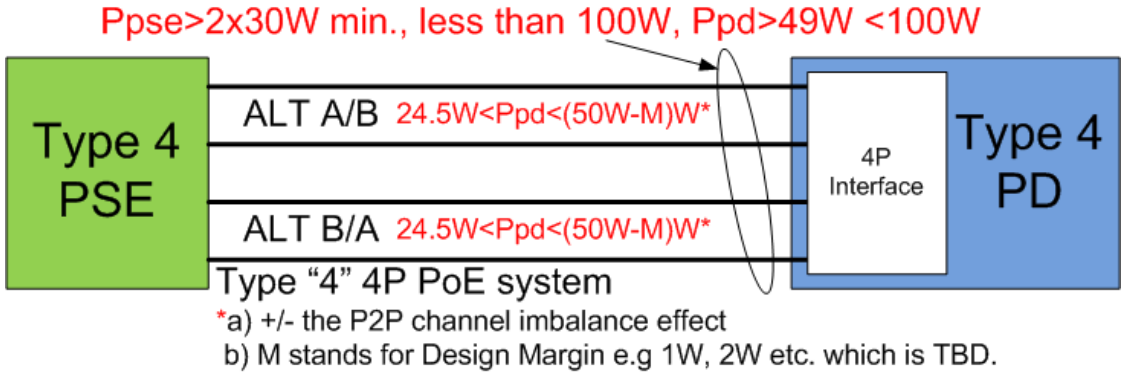


*Only one alternative may be powered at a time.

Type “3” and “4” New PSE and PD types for 4P-PoE

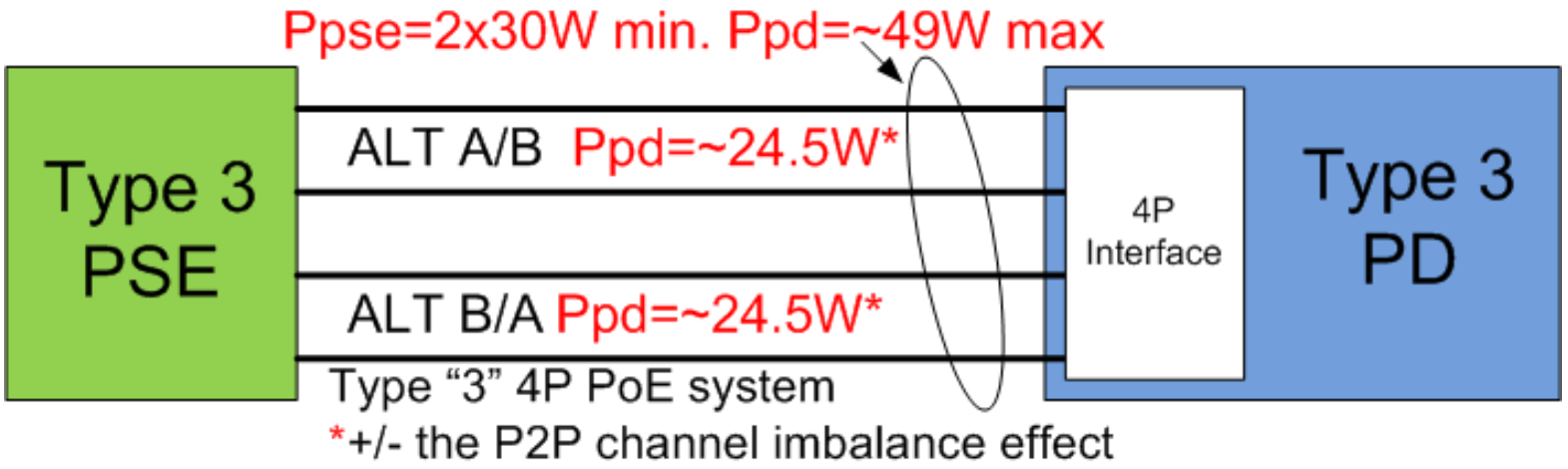
- New 4P PoE standard may consists of two new types:
  - Type “3” (Temporary type name): PDs with up to 49W and PSE to support it.
  - Type “4” (Temporary type name): PDs with >49W and less than 100W and PSE to support it.
- The above differentiation is required to allow system cost optimizations based on market and applications.





PSE Type “3” Requirements

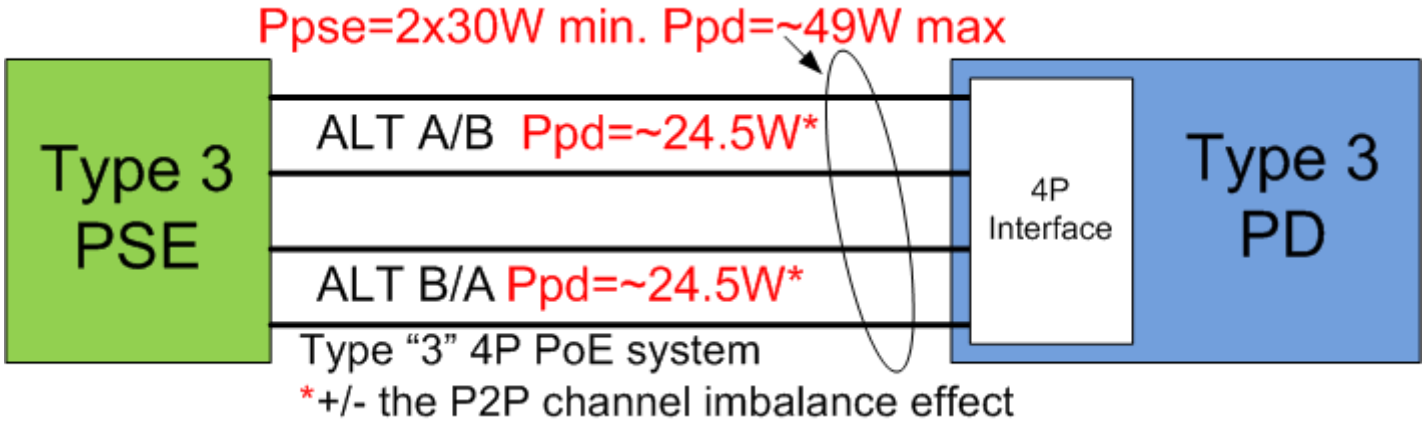
- Delivering 2xType 2 PSE=2x30W=60W min. power simultaneously on ALT A and ALT B.
- Supporting Type “3” PDs, with <25.5W or Type 1/2 PDs over 4P for maximizing system efficiency (*).
- Backwards compatibility to Type 1 and Type 2 PDs.
- Allow PSEs to support Type “3” PDs, with legacy power levels, over 2P, in case of fault on ALT A or B (pending the PD is designed to support it, See Annex B).



(*) 4P Powering is allowed/recommended with 4P PSEs if legacy power is present for maximizing system power efficiency. (CFI)

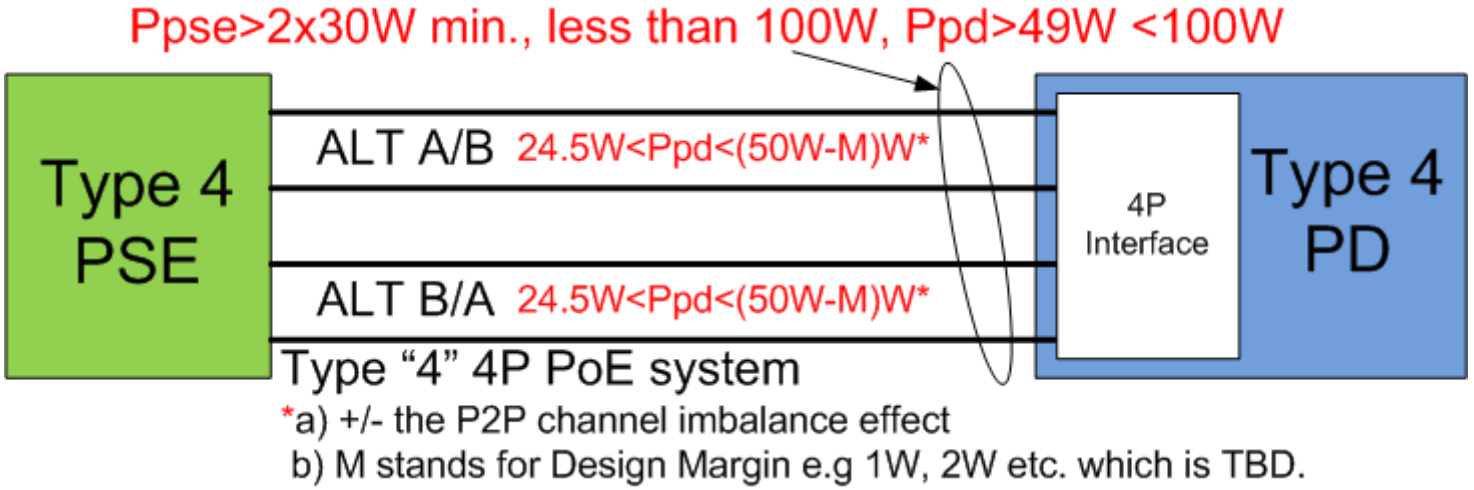
PD Type “3” Requirements

- is required to work with Mode A and B simultaneously with 49W maximum (driven by 4P-PSE Type “3”).
- is required to work with Mode A and B simultaneously with 4P PSE type “4”.
- PDs that have a mode to operate **within** 25.5W, should interoperate with Type 2 PSEs.
- Provisions for under power indication
  i.e. Type 2 PSE may not power a Type 4 PD that requires >30W.



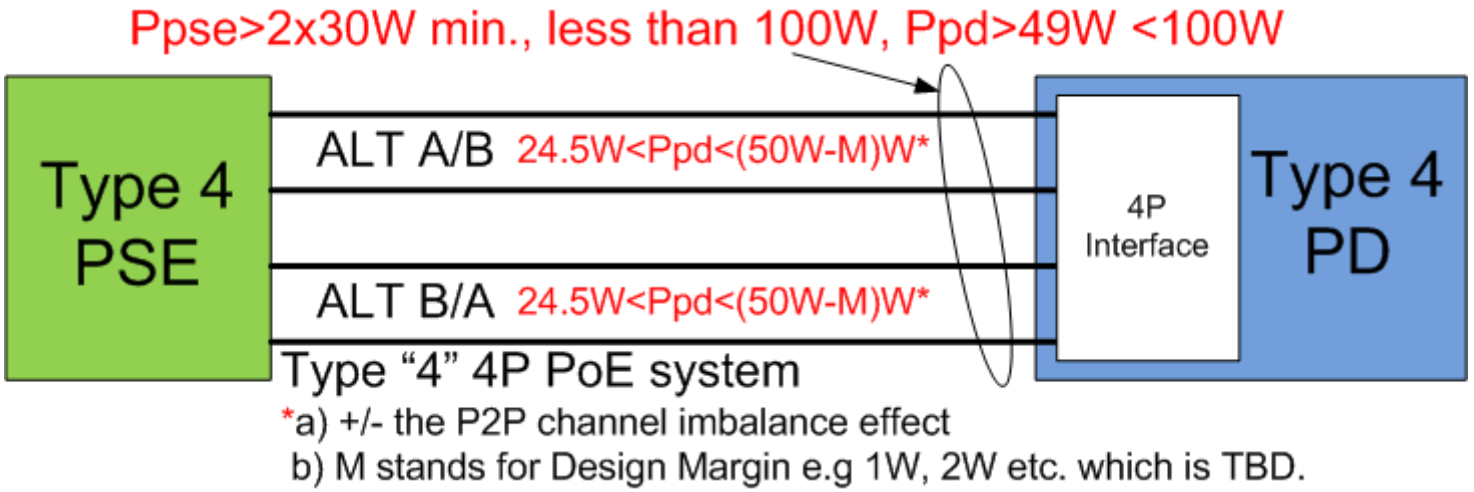
PSE Type “4” Requirements

- Delivering >2xType 2 PSE=2x30W=60W min. and less than 100W power powering ALT A and ALT B.
- Supporting Type “4” and Type “3” PDs, with <25.5W, or Type 1/2 PDs over 4P for maximizing system efficiency over 4P for maximizing system efficiency.
- Backwards compatibility to Type 1 and Type 2 PDs.
- Allow PSEs to support Type “4” PDs, with legacy power levels, over 2P, in case of fault on ALT A or B (pending if the PD is designed to support it, See Annex B).



PD Type “4” Requirements

- Works with Mode A and B simultaneously with >~2x24.5W=49W up to less than 2x(50-M) Watts (driven by 4P-PSE Type “4”).
- To support legacy power levels with legacy PSEs over 2P.
- PDs that have a mode to operate **within** 25.5W, should interoperate with Type 2 PSEs.
- Legacy power levels will be supported with 4P PSEs (Type “3” or “4”) over 4 pairs for maximizing system power efficiency. (CFI)
- Provisions for under power indication
  i.e. Type 2 PSE may not power a Type 4 PD that requires >30W.



PSE/PD Detection

- Same as in Type 1 and Type 2 per the current standard.
- See details in IEEE802.3-12 Clause 33.2.5
  - Same voltages, current and timings per the current standard 802.3 standard.
- the PSE is required to turn on power **only** on the same pairs as those used for detection. (IEEE802.3-12 Clause 33.2.5)
- It is proposed that the detection on ALT A and ALT B will be staggered.
  - This ensures that both alternatives are connected to a PD
  - This is done to prevent damage to network equipment.
  - Prevents problems with simultaneous detection on all pairs that will not detect a break in one of the alternative paths.
  - This prevents a false invalid detection for Type 1/2 PDs including existing 4P PoE) where both diode bridges are tied together at their outputs.
  - It helps simplifying the PD with negligible cost for PSE.

PSE/PD Classification

- **PSE:**
  - Similar concept as in Type 1 and 2 regarding voltages/currents/timing of the classes attempt function per the current 802.3 standard with the following changes:
    - For Type 3, we will have 2 Class Events over each alternative.
    - For Type 4, adding one more Class Event with its mark event etc. over each alternative.
    - It is proposed that the classification cycle on ALT A and ALT B will staggered. It helps simplifying the PD and PSE.
    - Other proposal could be considered.
- **PD:**
- We need more classes/Types without increasing class current
- *The following approach is cost effective, thermally possible and addresses the types and classes numbers that we need.*
- *This proposal is using the classification events as the trigger to change PD class to form new class codes. It opens up new opportunities and design flexibility.*
- *In addition the PD observes the classification events on each alternative.*
- *See Mutual Identification separate topic on next slides for details.*

Startup

- For all PSE/PD types
  - Startup concept is the same as defined for 2P operation.
  - Each 2P will meet the same current/voltage/timings etc. requirements as Type 1 and Type 2 PDs.
  - Startup STATE for both ALT A and ALT B can be at ~same time or at any time limited only by Tpon: TBD
    - If startup happens at the same time e.g. < 100usec time difference PD implementation is much simpler (same as legacy typical implementation however there are cost effective solutions when startup of each channel is not on the same time).
    - TBD time after startup (80msec per table 33-18 item 6 as in Type 2 PD) PD can draw for maximum power (above type 1 power).
  - TPON is met by specifying it from the last detection to startup so all legacy timing limitations are met.
- See Timing Diagrams in next slides.

Power ON state

- Type “3” system
  - Similar numbers as per 2P Type 2 power for I_cut, I_LIM, TLIM
    - Addressing some changes due to P2P current unbalance
  - Under fault condition, the faulty power channel shall be turn Off.
  - *System decision is if to turn OFF both channels.*
    - *Allows supporting PDs with reduced operating mode so they can function with less power e.g. Type 2 or 1 power levels*
- Type “4” system
  - Similar concept as Type “3” with modifying Icut, ILIM thresholds for the higher current range.

Disconnect function

- MPS: same concept as defined for 2P
- Implemented on ALT A and B.
  - Ensures compatibility with legacy devices working on ALT A or ALT B
  - Removes power when disconnect occurs.
  - Prevents multiple hot connect after disconnect due to undiscovered loose connection (connector reliability, sparks, corona etc.)
  - I_hold and TMPS timing is being evaluated by the group.To investigate how we can reduce MPS power.

PSE/PD Type “4” Cabling Requirements - 1

- The existing cabling system with CAT5e supports PoE 4P Type “3” without the need for further work per IEEE802.3-2012 Clause 33.1.4.1.
  - 0.6A per pair for all 4 pairs simultaneously over CAT5e or better
  - Trise=10°C max.
  - Current is distributed ~evenly)
  - This is also supporting the approach of same bundle size (100cables) for all cables CATs which is easier for installers.
- How to handle >60W power *over CAT5e? Considerations:*
  - Higher current than 0.6A is required per pair.
  - Up to maximum of 1A (=100W/50V/2) per pair if we want this to be the final PoE standard. ☺
  - All 4 pairs energized simultaneously with Trise <10°C.

PSE/PD Type “4” Cabling Requirements - 2

- Proposals
  - Option A : To define systems with a lower number of cables per bundle so temperature rise will be kept 10°C. This approach supports current cabling installations of CAT5e at maximum possible power.
    - To supply a table with cable type (CAT5e/6/6A/7 etc. vs. # of cables per bundle) as per the following example on next slide.
    - See example next slide and separate presentation addressing this option by cabling expert.
  - Option B:
  - To define *constant bundle size* for CAT5e and above, Trise =10°C max.
    - This may be easier for installers.
  - I believe that with clear specification wording we can address both options.
  - See separate presentation addressing this option by cabling expert.

PSE/PD Type “4” Cabling Requirements - 3

Option A example:

- Number of cables in Bundle when delivering 0.85A and 1A over each pair on all 4 pairs.
- Worst case temperature rise of 10degC.

	Number of cables in a bundle		**Insulation Diameter [mm]**	**Minimum Conductor Diameter [mm]**
Pair current	0.85A	1A		
Cable Type				
CAT5e	33	22	0.74-0.99 (Estimated)	0.5 (Estimated)
CAT6A UTP	67	44	0.91 – 1.2	0.52 -0.58
CAT6A F/UTP	93	63	1.02 -1.07	0.53 – 0.54
CAT7A S/FTP	141	100	1.37 – 1.53	0.62 – 0.63

-Test data supplied by Valerie Maguire from the Siemon company.
-See updated data per Val’s presentation.

Summary – 1

- **The proposed 4P Concept and Requirements**
  - Benefits from the experience, reliability and compatibility of current IEEE802.3-2012 specifications
  - Backwards compatibility and interoperability between legacy and new devices are met.
  - Cost effective
  - Covers most of use cases existing in the market today and allows flexible future implementations
  - Maintain the high reliability of the PoE systems during fault conditions
  - Reduces the number of missed faults.
  - Not reinventing the wheel and staying with the same $/w or lower cost.

Mutual Identification

Supporters:
George Zimmerman
Valerie Maguire / Siemon
Christian Beia / ST
Fred Schindler / SeenSimply
Ron Nordin / Panduit
David Tremblay / HP

PSE/PD all Types (1,2,”3”,”4”)- Mutual Identification -1

- Mutual Identification is required between PSEs and PDs.
- PSEs and PDs for Type 1 and 2 – as per IEEE802.3-2012
- Higher granularity classification may be required for applications such as lighting prior to power ON state in addition to the DLL classification.

- The following is a proposal for Mutual Identification.
- This proposal is only a starting point for Mutual ID, which may be simplified after we determine our needs

PSEs all types - Mutual Identification -2

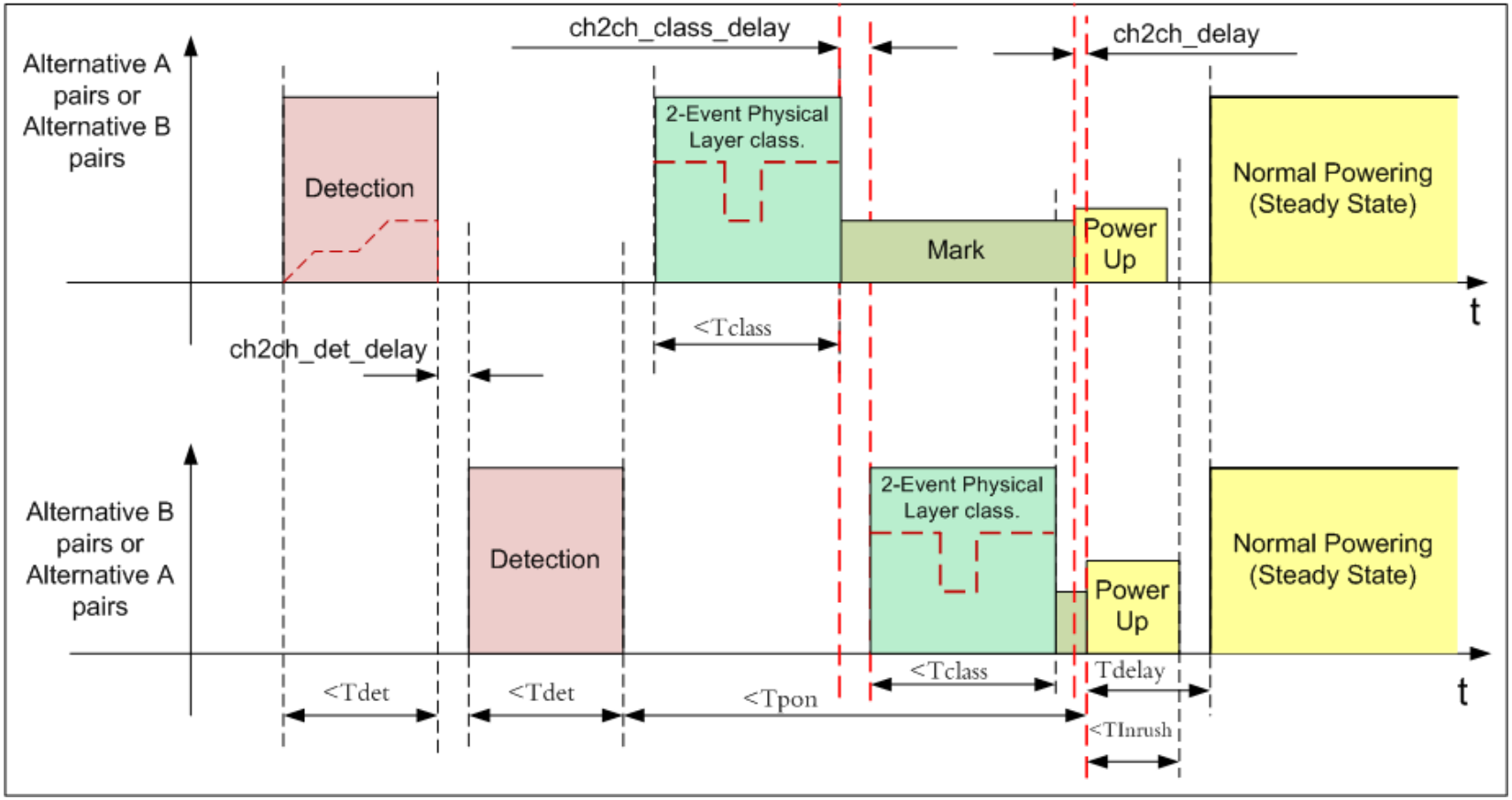
- PSE side
  - Reuse the same class/mark events and timing concept for physical layer classification defined by IEEE802.3-2012.
  - We have sufficient time between detection and POWER ON to add more class/mark events.
  - The number of class events on ALT A and ALT B seen by PD, indicates the PSE type.

PSE Type	PSE Power	# of classification attempts		Seen by PD as
		Pairs A/B	Pairs B/A	
1*	15	0/1	-	0/1
2*	30	2 (**)	-	2 (**)
3	2xType 2=60W	2	2	4 events(**)
4	2X30<Power<2*(50-M)	3	3	6 events(**)

* Legacy systems. ** This presentation is focused on physical layer DLL

Mutual Identification -3

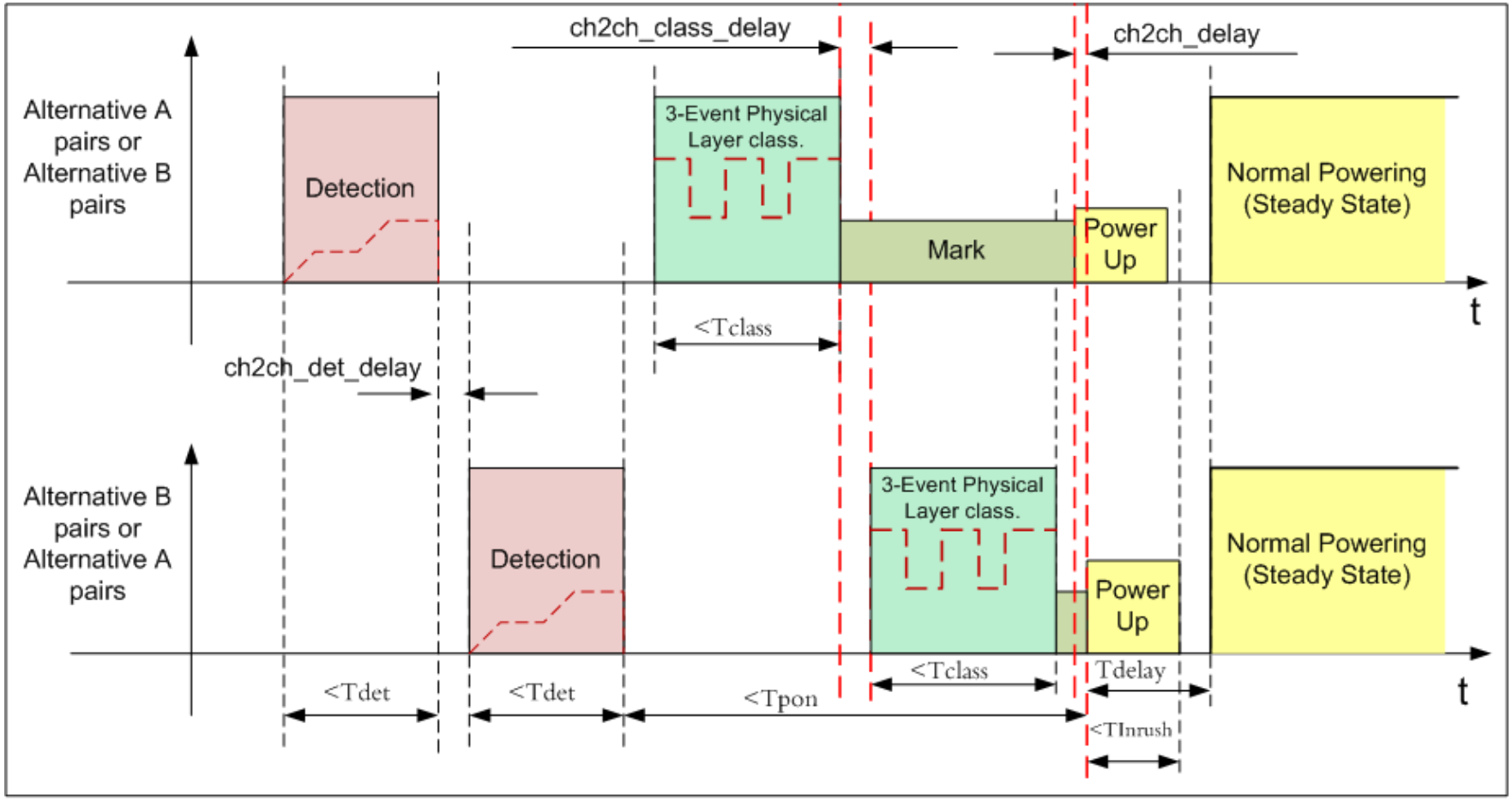
Preliminary Type 3 system timing Diagram



- Tpon of the system is measured from last detection
- This concept allows single PD chip and single PSE chip for any PSE/PD type including legacy devices.

Mutual Identification -4

Preliminary Type 4 system timing Diagram



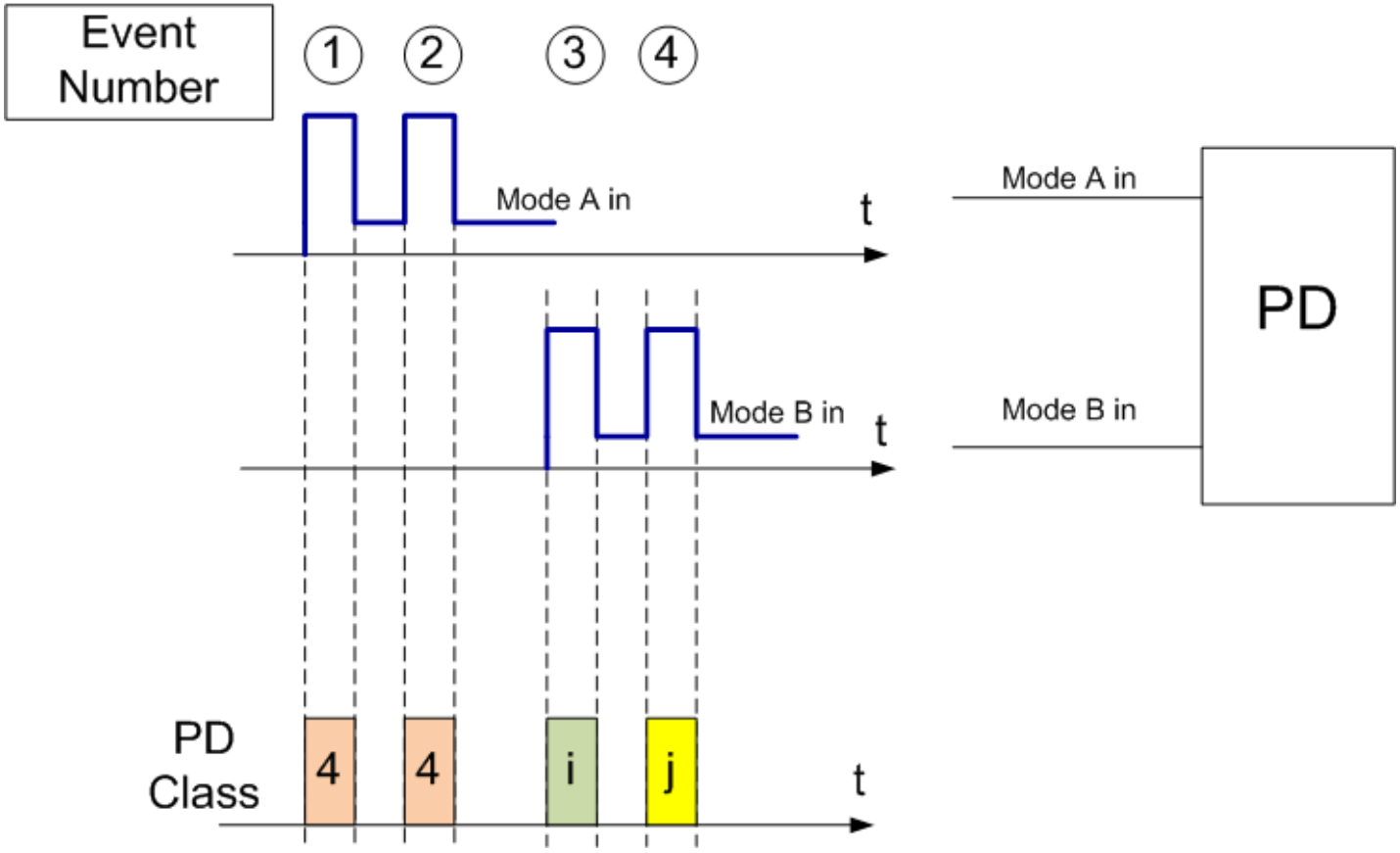
- Similar to Type 3 system with additional 3rd class event.
- Tpon of the system is measured from last detection
- This concept allows single PD chip and single PSE chip for any PSE/PD type including legacy devices.

PD Type "3"/"4" - Mutual Identification -5

For Type “3” and Type “4”:

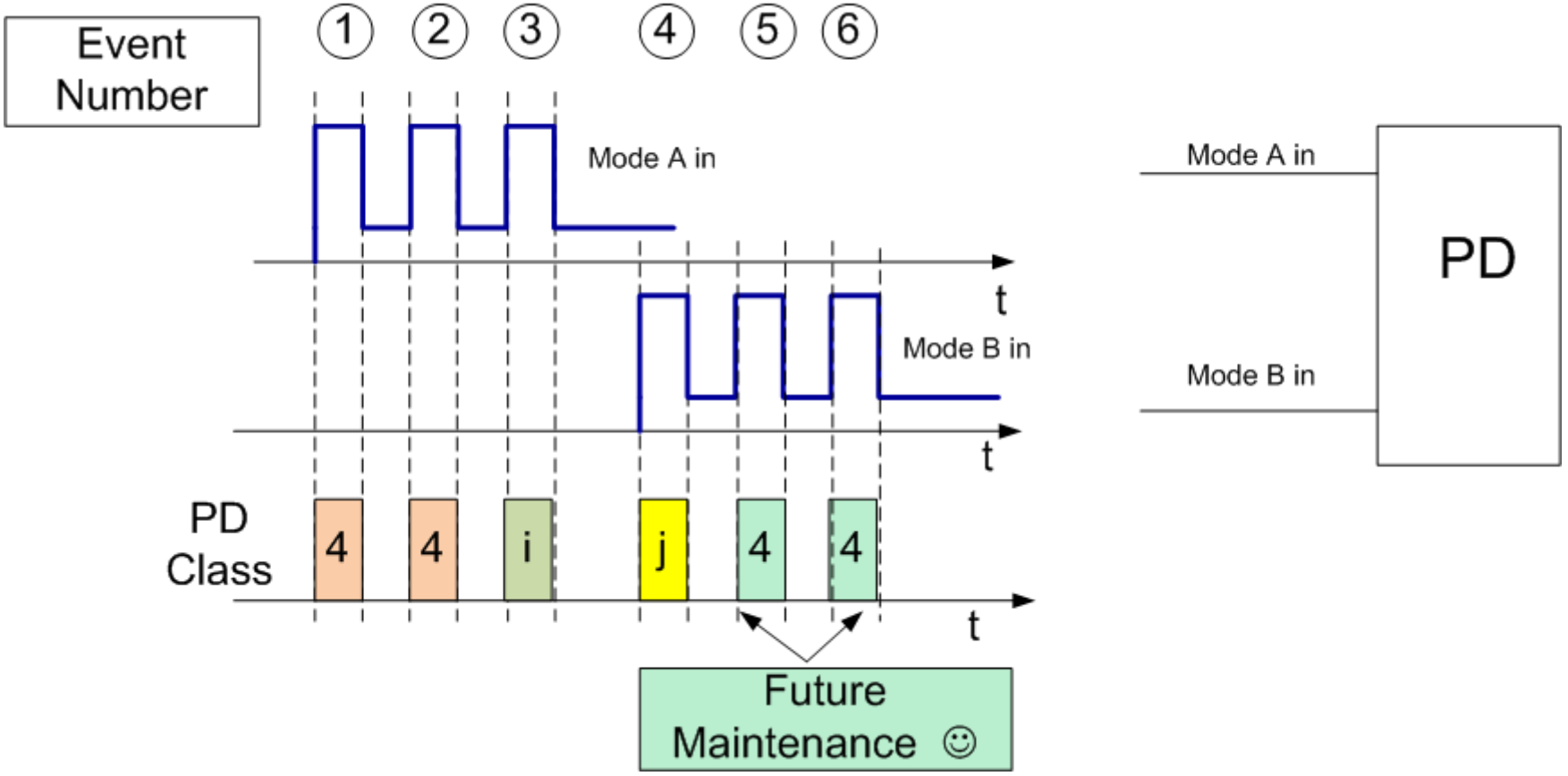
- The PD will present Class 4 for the 1st and 2nd class event received from PSE (This provides backward compatibility with Type 2 PSEs)
- PD will change its class for events 3 and 4, to produce a new code e.g. **44lJ**.
- For class “4”:
- PD will present class “4” for vents 5 and 6.
- The new code will look like **44lJ44.**
- At this point of time, Type 3 and Type 4 PDs have together 15 codes.
- This codes can be used for PD Types and PD power class.
- If we want more codes. We can use events 5 and 6 to expand the codes.
- If we want less codes, we can set the PD to present class 4 at the 3rd even as well, so we will have only 3 new codes.
- See next table for code allocation example.
  - To be discussed with group for preferences.
- At this point of the discussion the rest is implementation details and needs more study later.

PD Type 3 - Mutual Identification - 6



- **i** and **j** forms new classes i.e. 44 **ij** e.g. 4443, 4413
- i=j=4 is Type 2 PD.
- See next slide for initial work regarding codes interpretations.

PD Type 4 - Mutual Identification -7



- **i** and **j** forms new classes i.e. 44 **ij** 44 e.g. 44**4**344, 44**1**344
- i=j=4 is Type 2 PD.

New Type 3/4 PD classifications allocation example - 8

Class Event								
1	2	3	4	5	6			
		i	j			PD Type	Class ij part	Type/Power level TBD
4	4	1	1	-	-	3	11	Type 3 New class
4	4	1	2	-	-	3	12	Type 3 New class
4	4	1	3	-	-	3	13	Type 3 New class
4	4	1	4	-	-	3	14	Type 3 New class
4	4	2	1	-	-	4	21	Type 4 New class
4	4	2	2	4	4	4	22	Type 4 New class
4	4	2	3	4	4	4	23	Type 4 New class
4	4	2	4	4	4	4	24	Type 4 New class
4	4	3	1	4	4	4	31	Type 4 New class
4	4	3	2	-/4	-/4	spare	32	Type 3/4 New class
4	4	3	3	-/4	-/4	spare	33	Type 3/4 New class
4	4	3	4	-/4	-/4	spare	34	Type 3/4 New class
4	4	4	1	-/4	-/4	spare	41	Type 3/4 New class
4	4	4	2	-/4	-/4	spare	42	Type 3/4 New class
4	4	4	3	-/4	-/4	spare	43	Type 3/4 New class
4	4	4	4	-/4	-/4	2	44	Type 2 Class 4

PSE/PD all Types (1,2,”3”,”4”)-Mutual Identification -9

- To be discussed
  - How many classes codes we need?
  - How many classes codes lighting equipment will need?
  - More?

Summary - 2

- **Mutual Identification proposal**
  - It allows mutual identification with all PSE and PD types.
  - It is an extension of what we have
    - Concept is based on current physical classification attempts requirements and PD class definitions.
  - It allows more classes and PD type codes.
  - Number of codes can be easily reduced if we don't ned it
  - Backwards compatible with legacy devices
  - Interoperable with legacy devices
  - Simple implementation
  - More work is needed

Discussion

Thank You

- Backup Slides on various issues

Annex A

- IEEE802.3 clause 33.2.5 first line.

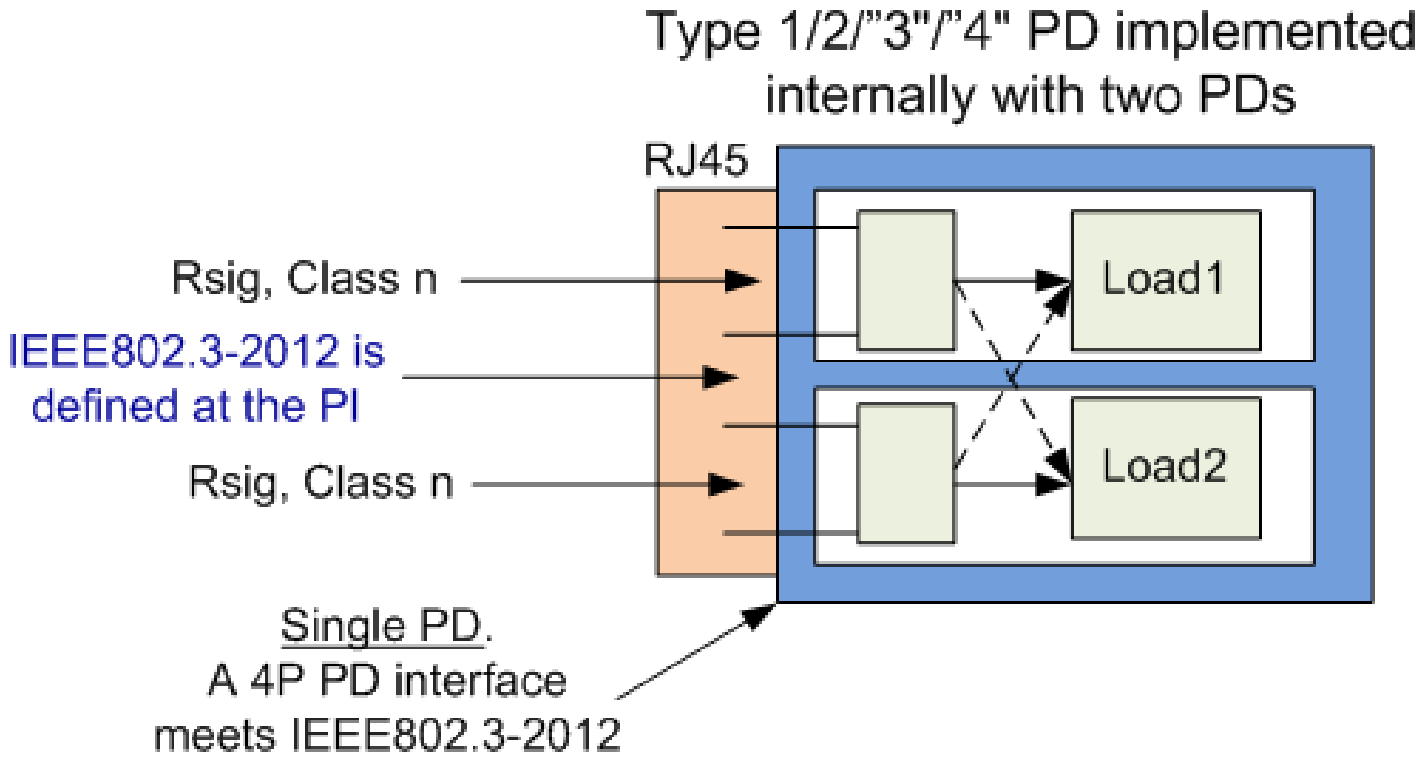
  In any operational state, the PSE shall not apply operating power to the PI until the PSE has successfully detected a PD requesting power.

- IEEE802.3 clause 33.2.5 last line.

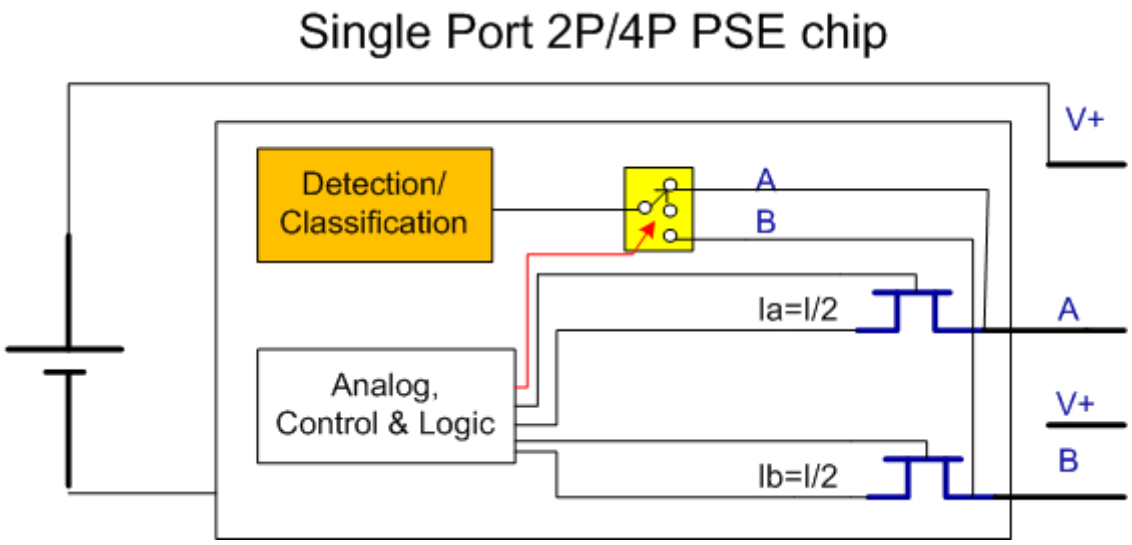
The PSE shall turn on power only on the same pairs as those used for detection.

Annex B

- PDs implemented with two internal PDs
- Any load can take power from any pair or from all pairs.
- PDs designed to work also with legacy power levels
- Compatible to IEEE802.3-2012 over 2P operation on ALT A or B



4P PSE single port – typical implementations



Cost per port is even better with multiport chip. Reuse of same chip resources.

- Chip resources are used for all pairs.
- Specifically, detection and classification functionality are multiplexed between all pairs.
- Each port can be configured as 2P or 4P.

Silicon Area of two MOSFETs

- MOSFETs takes significant chip silicon area.
- Rdson value is direct function of silicon area.
- The silicon area of a single MOSFET carrying I current is the same of 2 MOSFETS carrying I/2 current.
- Chip Level and System Level wise, the use of 2 MOSFETs, one per ALT A and ALT B pairs as traditionally done today, is significantly superior than other solutions. It is cost affective, allows design flexibility, reliability, compatibility and interoperability

Two Mosfets

$$P_A = Rd \cdot \left(\frac{I_A}{2}\right)^2 \quad P_B = Rd \cdot \left(\frac{I_B}{2}\right)^2$$

$$P2 = P_A + P_B = 2 \cdot Rd \cdot \left(\frac{I_B}{2}\right)^2 = 0.$$

Single Mosfet

$$P1 = Rdx \cdot I^2$$

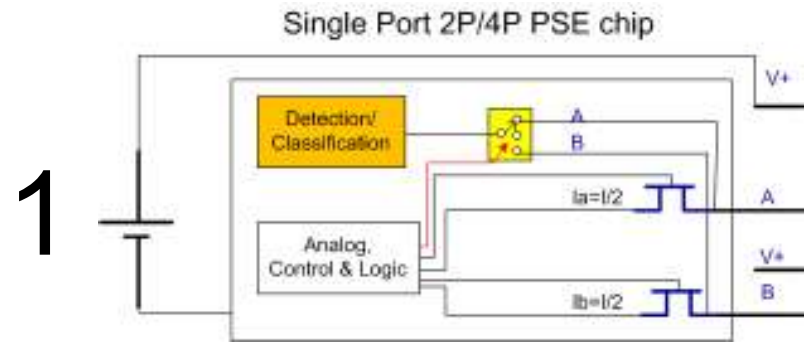
$$P1 = P2 \rightarrow Rdx = \frac{Rd}{2}$$

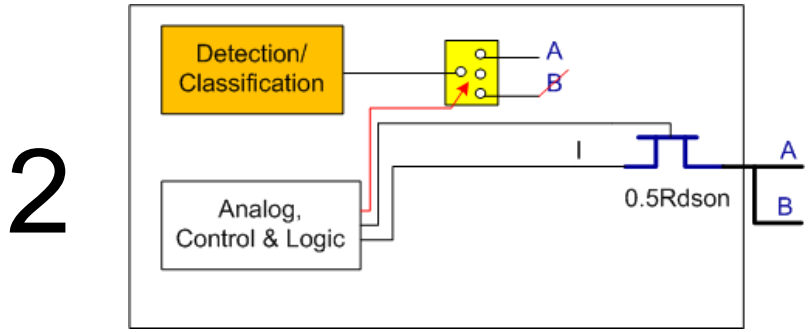
-Silicon area of MOSFET=k*Rdson.
-Single mosfet silicon area=two Mosfet silicon area
-Cost difference of other items ,negligible and cost effective.

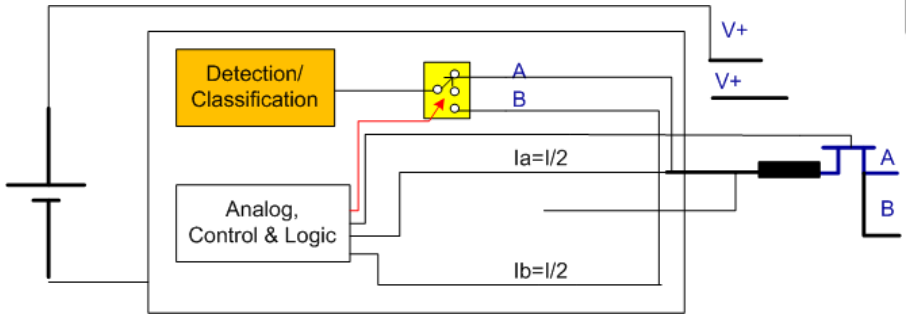
Cost - 1

- Case A :
- A chip with total output power of P, with Nx2P ports or (N/2)x4P ports cost the same.
  - It doesn't matter if it is implemented with 1 FET per 4P or 2 FETs per 4Pairs for getting the same power dissipation.
    - The "Rdson" equivalent amount = silicon area is the same.
- Case B:
  - If using external MOSFETs than 2 FETs cost more than 1 FET excluding the cost of the chip in both cases.
  - However system wise it may cost more due to quantities and pricing model.
  - It further will cost more at the BOX level.
  - Any how, It is implementation choice.
- Case A is the lowest cost chip and system wise

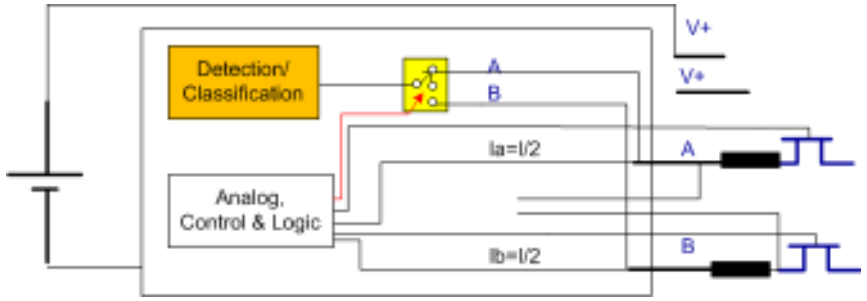
Cost - 2







Option	Cost	
Circuit	Chip+MOSFET	System
1	1	1
2	1	>>1
3	1.08	>>1
4	1.12	1.12



Y-cable Examples

- See slides 4,5 and 6 for Y connection examples at:

http://www.ieee802.org/3/bt/public/jan14/heath_04_0114.pdf

See slides 4 and 5 for Y connection example that has no risk due to separate MOSFETs and powering only after valid pairs at:
http://www.ieee802.org/3/bt/public/jan14/heath_04_0114.pdf

See damage and damage potential at slide 6 were single port with single MOSFET is connected to Y cable:
http://www.ieee802.org/3/bt/public/jan14/heath_04_0114.pdf

There is a long list of damage and safety issues with Y cables that will be mentioned if needed.