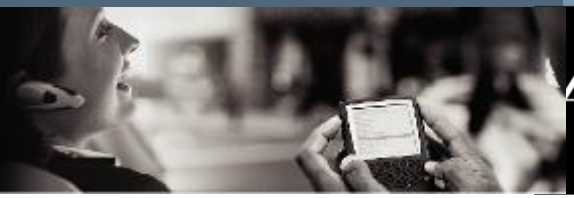
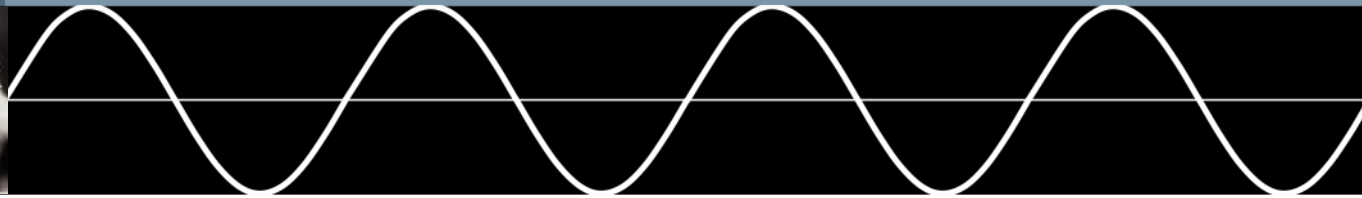
IEEE802.3bt
4 Pair PoE Current Imbalance Data and Thoughts

January 2014

J. Heath – Linear Technology





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Supporters

- Bill Delveaux (Avaya)
- David Tremblay (HP)
- Christian BEIA (ST Micro)
- Phil Brownlee (Coilcraft)

Goal of this Presentation

- Present preliminary lab data on diode mismatch
- Consider implications of not creating a specification for PD/PSE current mismatch
- Suggest the concept of specifying a current mismatch for PSEs and PDs
- Suggest a specification for:
  - PD current mismatch

What is New About 4 Pair Current Imbalance?

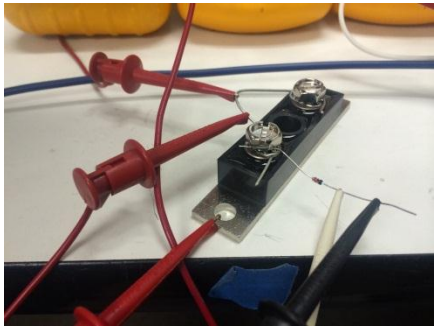
- The need to understand pair to pair current imbalance
- 2 pair common mode imbalance was not an issue because there were only 1 pair in each direction
- Differential mode imbalance was handled by a solid ‘educated guess’ on parasitics for
  - Transformers
  - Connectors
  - Cables
  - PCB Traces
  - Etc.

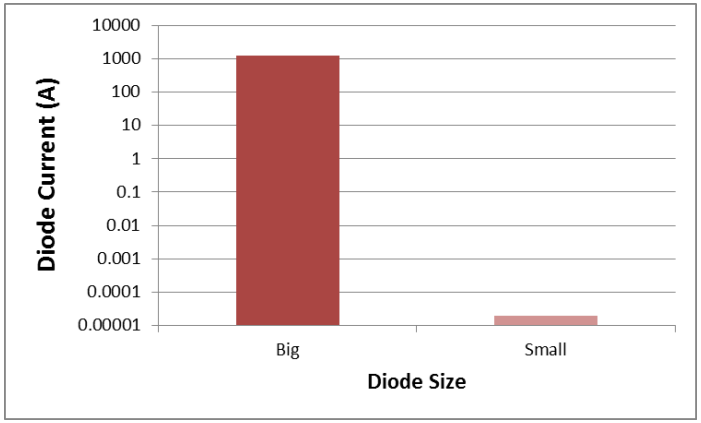
Why Do We Care?

- The health and happiness of transformers
  - Offset current causing loss of inductance and saturate cores
  - Heating causes loss of OCL
- There are other secondary issues but if one fixes the transformer problems the rest will be ok
  - Short of having huge transformers $$

What Could Happen if We Put No Specification on Current Balance in PSEs and PDs?

- Without a specification on the DC characteristics of both the PSE and PD, there would be no limit on what a customer is allowed to do
  - We could therefore not guarantee interoperability
  - Or have only ‘at’ power
- BTW, I agree this example is extreme but still useful to prove a point.





PD Components That Can Cause Imbalance

- DC Rectifiers – Thought to be the largest contributor when cables are short.
  - Diode bridges or MOSFET bridges
  - Diode bridges should be accommodated if possible for cost reasons
  - MOSFET bridges are available from multiple vendors
- Other magnetics (e.g. common mode chokes)
- Connectors
- Layout
- (Hot Swap MOSFETs for N-by-2 solutions)

PSE Components That Can Cause Imbalance

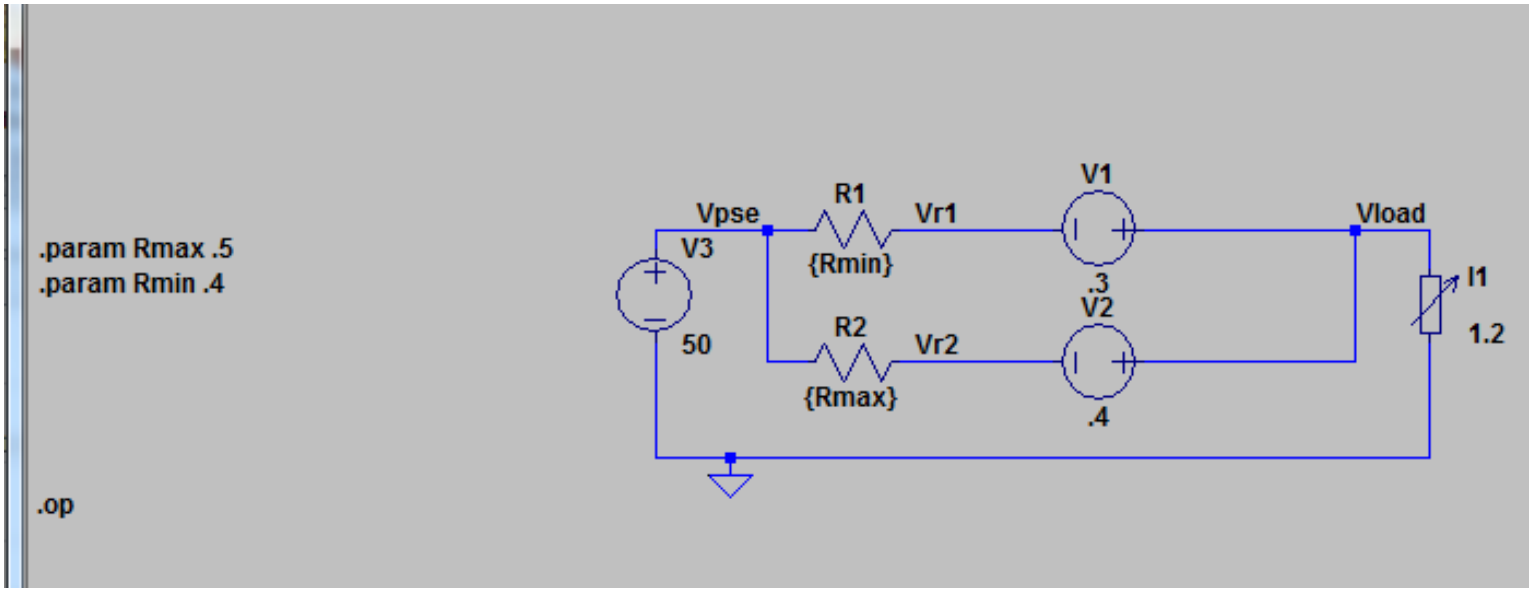
- Magnetics
- Connectors
- Layout
- (Hot Swap MOSFETs for 2-by-N PSE solutions)

PD – Diode Rectifier Data

- Previous imbalance presentations are based on a mathematical model
  - (Diodes (B1100 linearized model @0.6A): 0.3V+0.4Ohm*Id; 0.4V+0.5Ohm*id)
- My goal is to cross check these assumptions two ways
  - LTspice simulation data
  - Laboratory measurements

Simplified Diode Model LTspice Results Using Original Assumptions

- I(I1): 1.2 A (load)
- I(R2): 0.644 A
- I(R1): 0.555 A



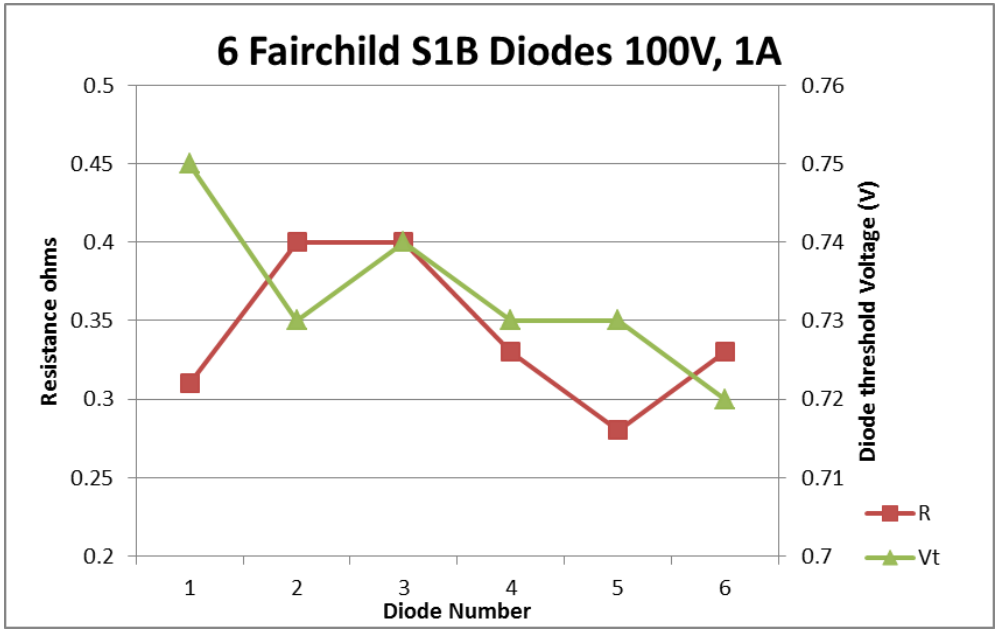
6 diode measurement results from MFG 1:

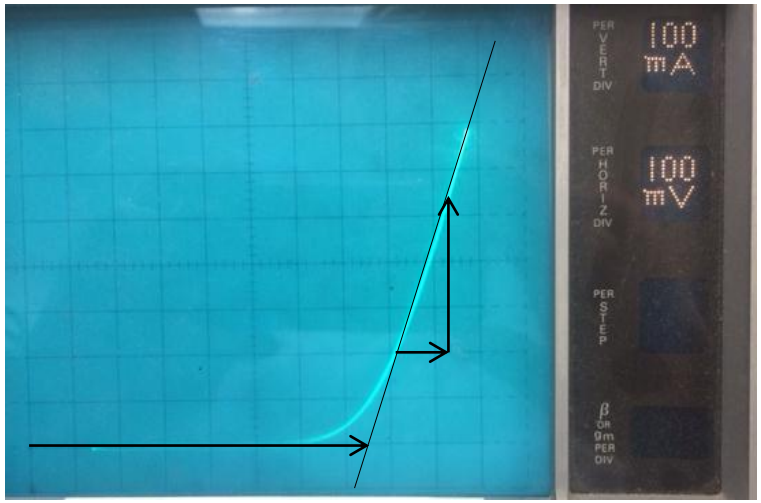
Vt Delta 0.03V R delta 0.12 ohms

Compared to simplified model analysis

Vt Delta 0.1V R delta 0.1 ohms

Diode	R	Vt
1	0.31	0.75
2	0.4	0.73
3	0.4	0.74
4	0.33	0.73
5	0.28	0.73
6	0.33	0.72
Mean	0.342	0.733
Min	0.280	0.720
Max	0.400	0.750
Delta	0.120	0.030





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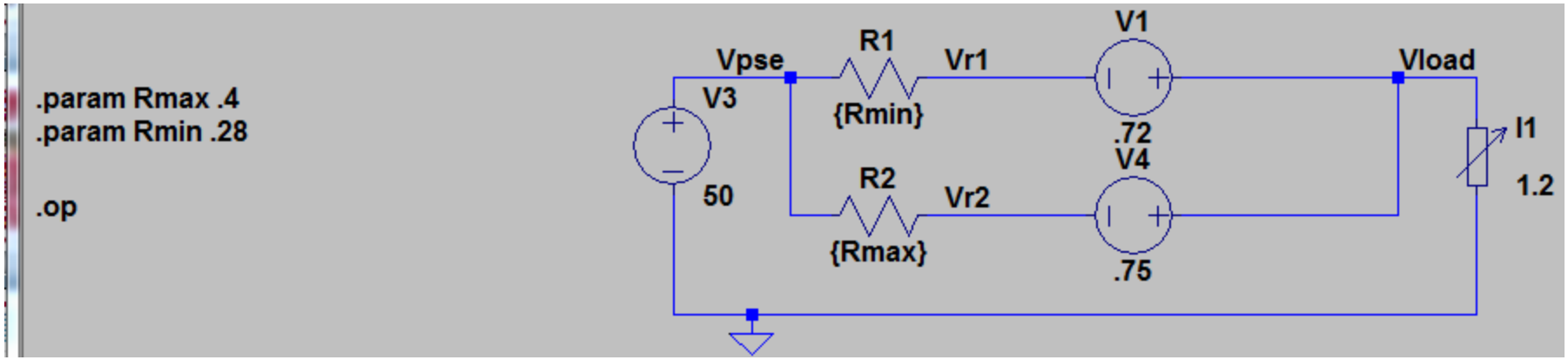
Simplified Diode Model LTspice Results Using Lab Data from 6 Diodes

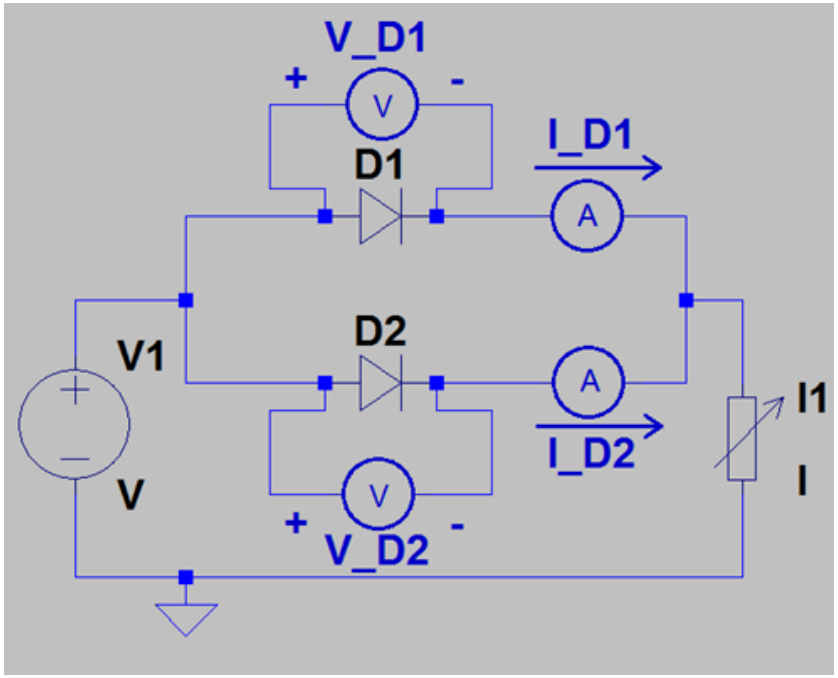
- I(I1): 1.2 device_current
- I(R2): 0.661 vs .644 (from above)
- I(R1): 0.538 vs .556 (from above)

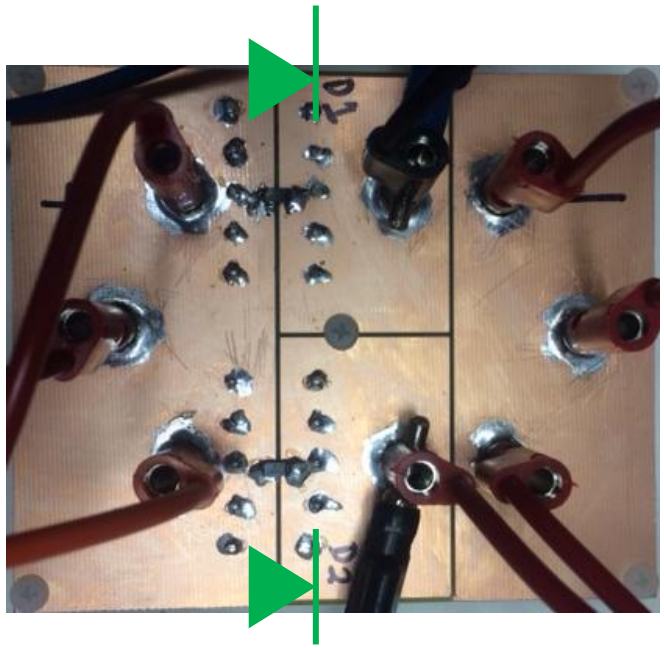
Original Estimates of imbalance due to diodes may be too low



Current Imbalance Lab Measurements

- Setup
  - Test schematic, test board

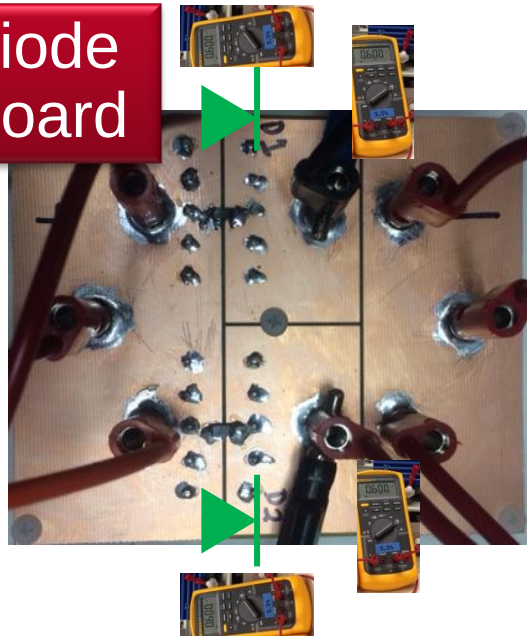




Lab Setup

- Isolate diode contribution to imbalance
- Worst case diode sharing
- Parasitic series resistance << than real system

Two Diode DUT Board



Current Meters ~0.05 Ohms

600mA check < 1mA or 0.2%

Full Bridge Sharing Setup

SMA Packages Using Multiple Manufacturers

- Imbalance for SMA package w/ multiple MFGs is quite large

Reference	Mfg.	Part #	Package
M1	Fairchild S	S1B	SMA
M2	Micro Com	GS1B-LTP	SMA
M3	Vishay	RS1B-E3/6	SMA
M4	Vishay	ES1B-E3/5	SMA
M5	Fairchild S	RS1B	SMA

CURRENTS										
Diode 1 (D1)	Diode 2 (D2)									
	M1		M2		M3		M4		M5	
	I_D1 (mA)	I_D2 (mA)	I_D1 (mA)	I_D2 (mA)	I_D1 (mA)	I_D2 (mA)	I_D1 (mA)	I_D2 (mA)	I_D1 (mA)	I_D2 (mA)
M1	656	547	497	705	777	426	242	962	766	437
M2	700	503	578	625	806	397	232	971	754	449
M3	487	717	380	823	609	594	202	1001	621	581
M4	962	241	851	351	993	209	526	676	939	264
M5	453	750	374	829	592	611	183	1020	678	526

Abs (deltas) mA	M1	M2	M3	M4	M5
M1	109	208	351	720	329
M2	197	47	409	739	305
M3	230	443	15	799	40
M4	721	500	784	150	675
M5	297	455	19	837	152
Max Imbalance Delta	721	500	784	837	675
% imbalance	60%	42%	65%	70%	56%

How Likely is the Multiple Vendor Scenario?

- Quite likely
  - Multiple vendors are typically qualified for manufacturing to avoid line down situations when a single vendor cannot produce parts
- With an imbalance specification in the 4 pair bt standard, OEMS can specify, test, and qualify DC rectifiers
- In the case of non-interoperating bt PSEs and PDs the offending device can be clearly and easily identified

SMA Packages Using a Single Manufacturer

S1B Comparison to within One Manufacturer (1.2A Load)				
Diode 1 (D1)	Diode 2 (D2)			
	M1_1			
	CURRENT		VOLTAGE	
	I_D1 (mA)	I_D2 (mA)	V_D1 (mV)	V_D2 (mV)
M1_2	653	549	879	877
M1_3	617	585	875	871
M1_4	599	604	875	868
M1_5	631	572	878	876
M1 x 2	*471*	*732*	*873*	*855*
Imbalance				
M1_2	104		2	
M1_3	32		4	
M1_4	5		7	
M1_5	59		2	
M1 x 2	*261*		*18*	
Max 'Single' mA	104			
% imbalance	9%			

Reference	Mfg.	Part #	Package
M1	Fairchild S	S1B	SMA
M2	Micro Com	GS1B-LTP	SMA
M3	Vishay	RS1B-E3/6	SMA
M4	Vishay	ES1B-E3/5	SMA
M5	Fairchild S	RS1B	SMA

- This is considerably better than multiple vendors
- *But, this is a very small sample*

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Comparison of Lab Measurements vs Two LTspice Predictions

- This data strongly suggests that we need a current imbalance specification for 4 pair 'bt' PDs
- Interoperability with Type 1 and Type 2 PDs is assured by default ok because even with 100% imbalance

		(A)	
	D1	**D2**	***Delta***
Simplified Model Original	**0.644**	**0.556**	**0.088**
Simplified Model with Measured Diodes	**0.661**	**0.538**	**0.123**
Single Vendor Lab Measurements Max	**0.653**	**0.549**	**0.104**
Multiple Vendor Lab Measurements Max	**0.183**	**1.020**	**0.837**

We are going to need a current imbalance spec

- With a small amount of lab data is quite clear we need a current imbalance specification on PDs and likely PSEs

Suggest Language for a bt PD Current Mismatch Standard

- The PD shall have a current imbalance when operating at any power level of less than xx mA between any 2 pairs that are passing current in the same direction as measured at the RJ45 connector.
  - This needs work!

Straw Polls

- Is there a technical need for an imbalance specification.
- Y: 21
- N: 0
- A: 7