Deadlock in Alt State Machines

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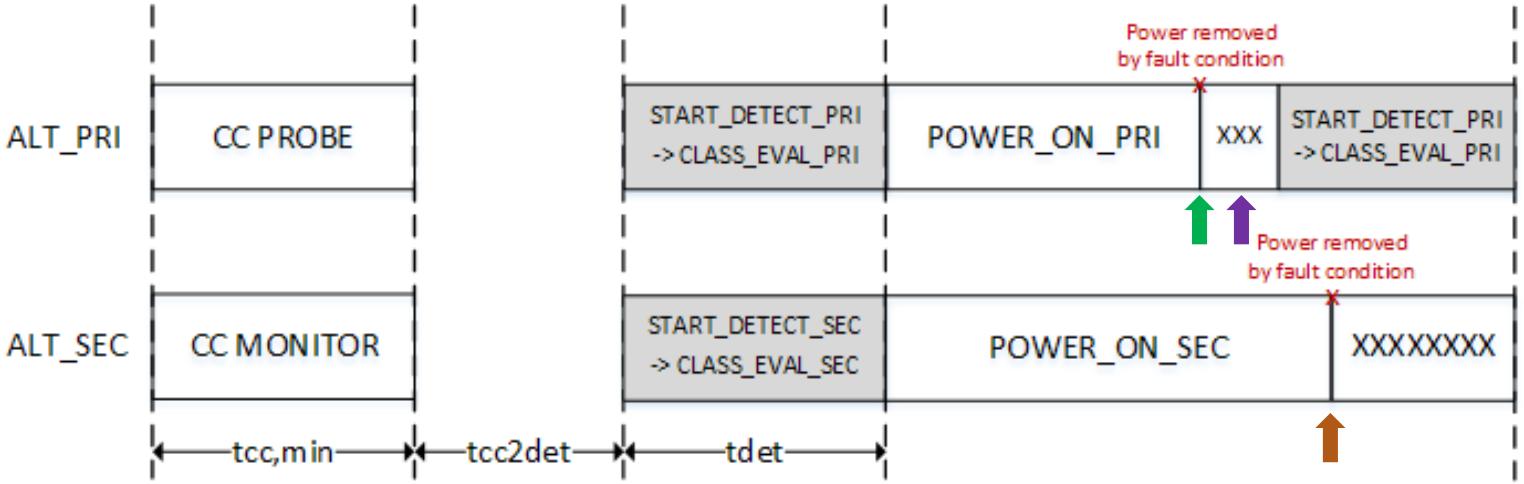
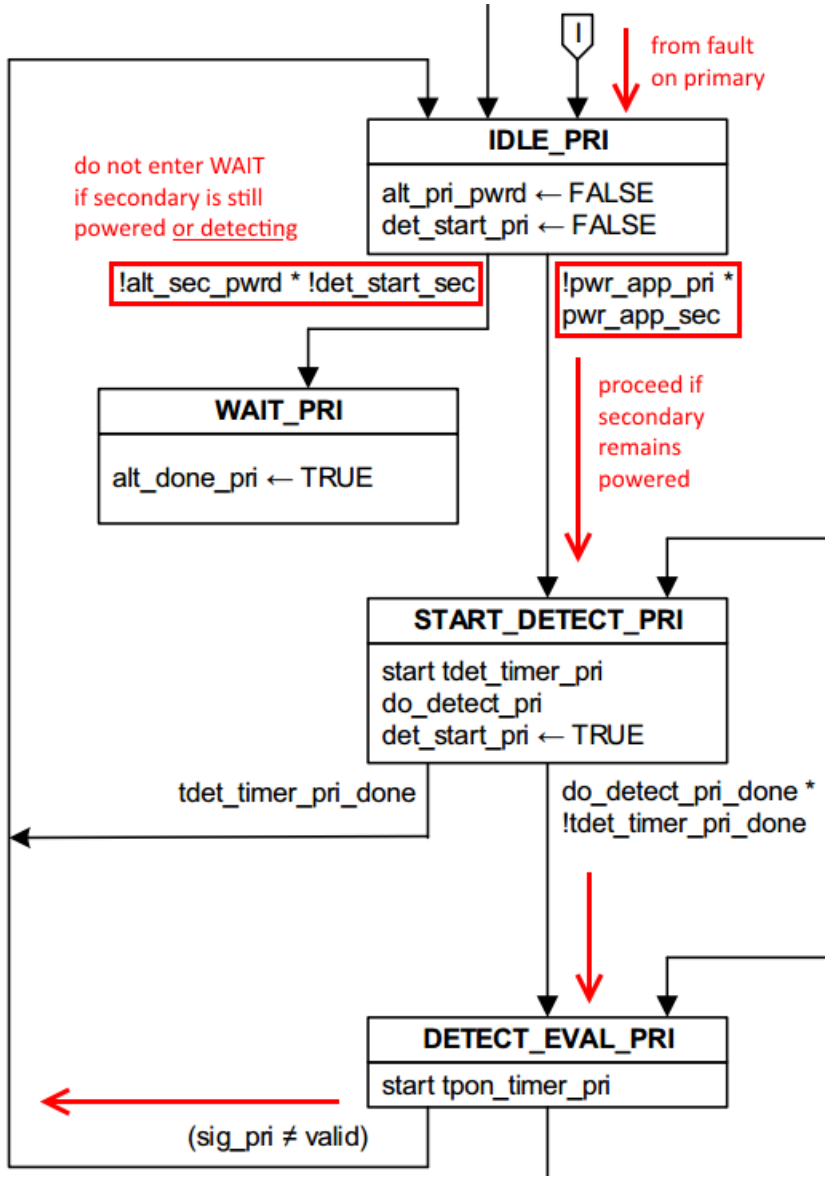
Problem Statement

- Scenarios exist where the primary and secondary Alt state machines can thrash out of phase perpetually
  - Any symmetric and out-of-phase DETECT, POWER_ON loops prevent Alt state machines from returning to global IDLE state
  - Applies to all dual signature PDs
    - Problem is not confined to any particular CC_DET_SEQ
  - Current behavior violates the Connection Check requirements in 33.2.5.0a

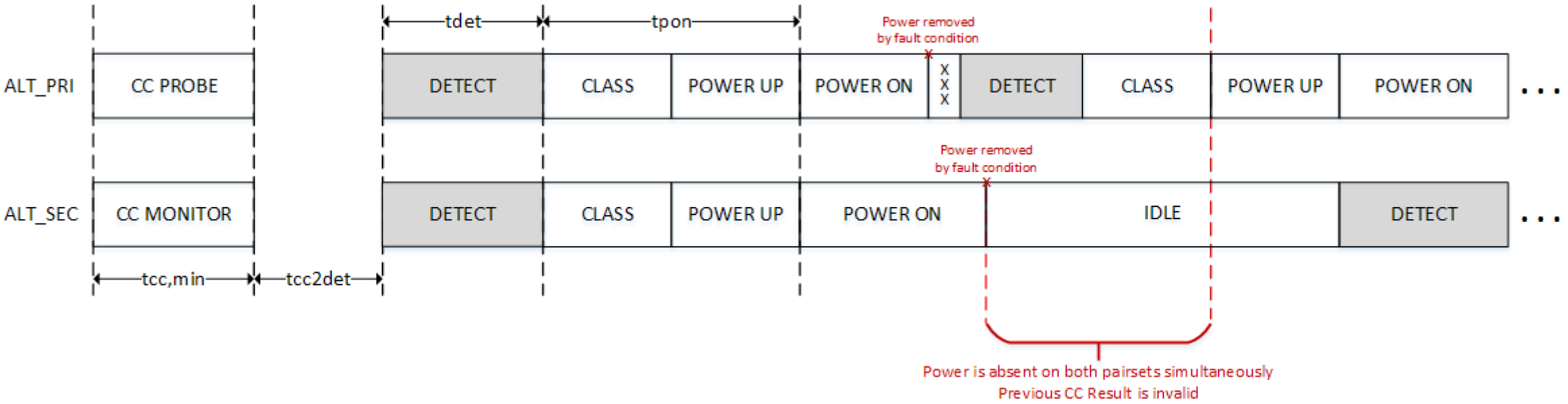
Example Case



- Consider a PD in fault condition
  - When power is removed from any Alt, that Alt shall perform another DETECT if power is being applied to the other Alt
  - As long as power is applied to the other Alt, the Alt may repeatedly cycle through (invalid) detections
  - Once a valid detection begins on an Alt, the other Alt may fault off and cycle through detections in the same manner
    - A fault on one Alt won't affect the other Alt's decision to apply power after successful detection, classification
    - Both sides of the link are unpowered and detecting at this time

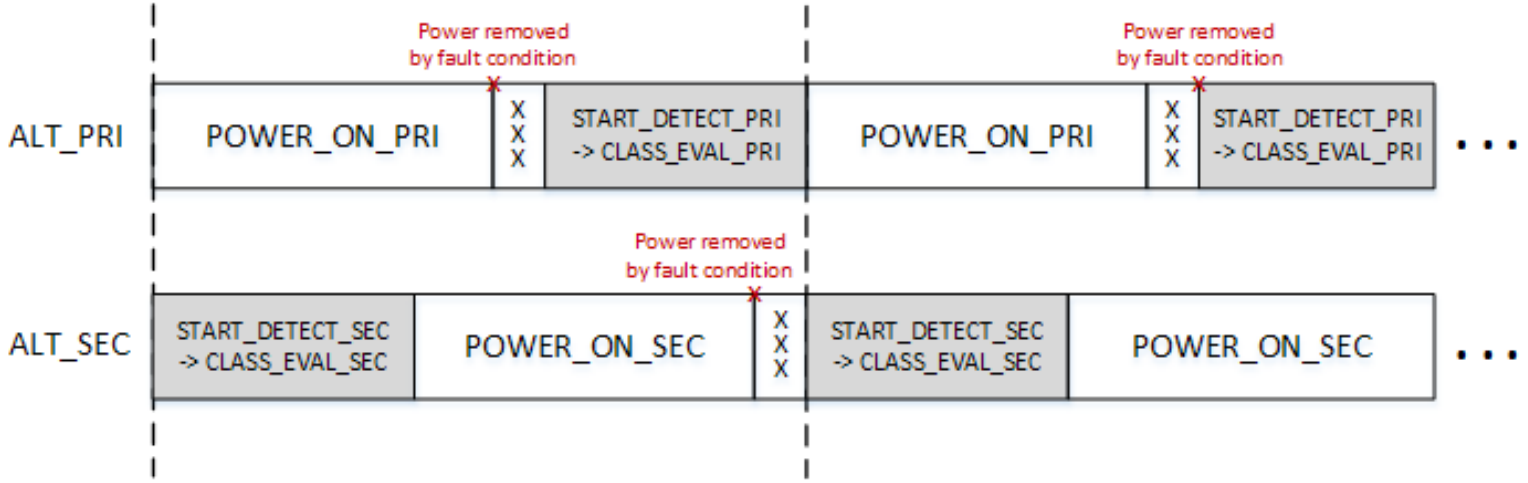


Example Case, continued



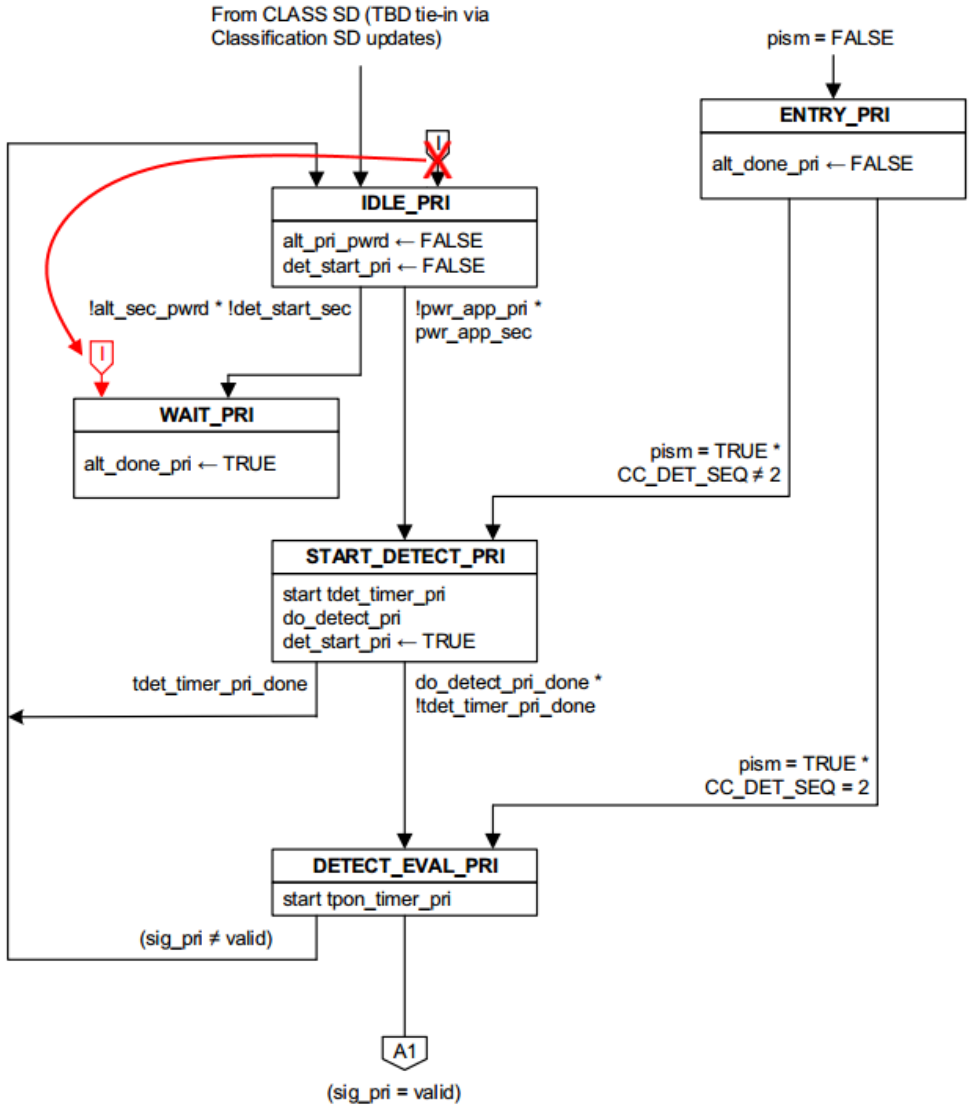
- 33.2.5.0a: "***The connection check is rerun before applying power if*** *power up fails to meet the timing requirements in both Table 33–3a and 33.2.7.13 or* ***power is absent on both pairsets simultaneously*** *or if the state machine reaches the IDLE state.*"

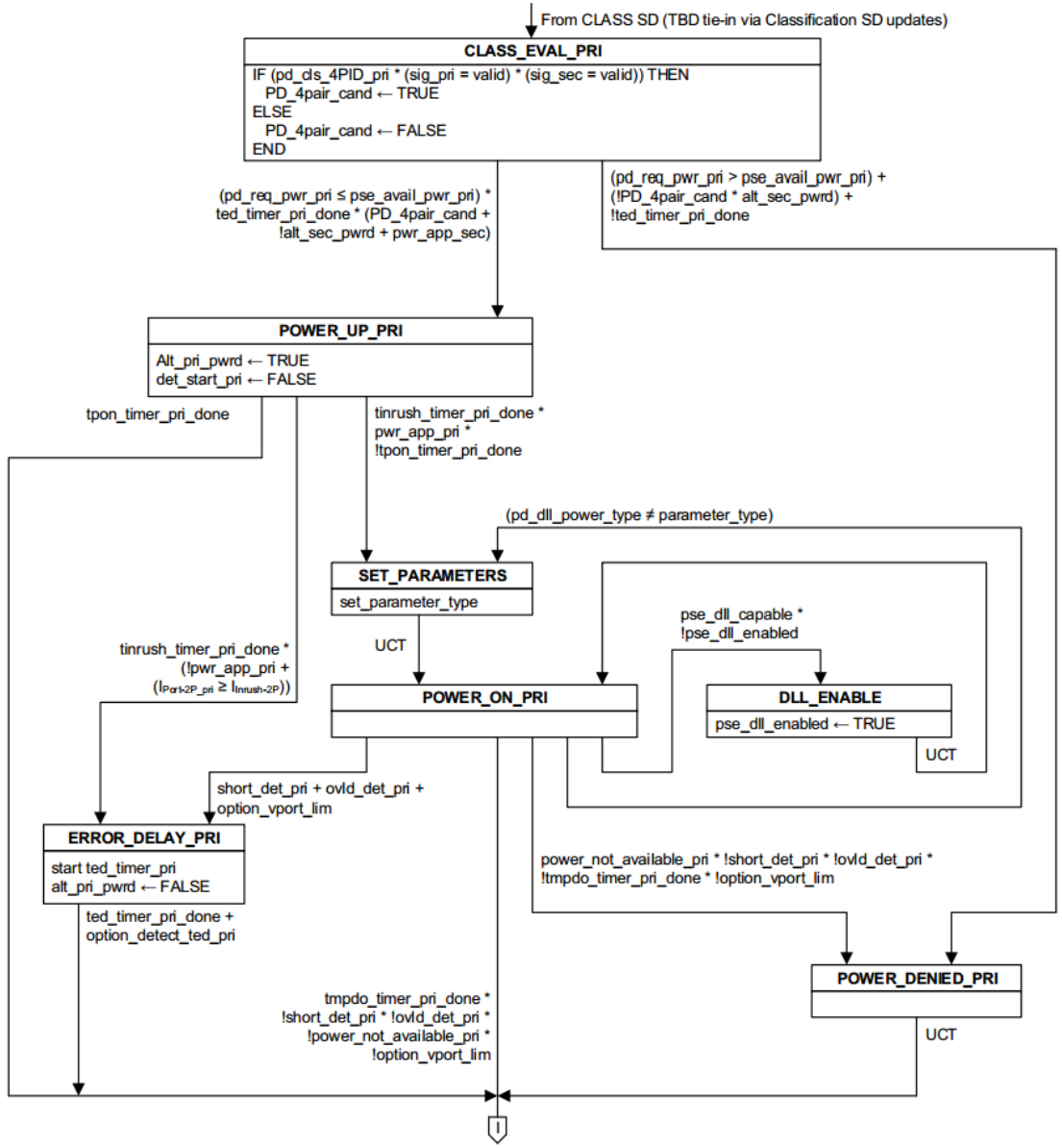
Example Case, continued



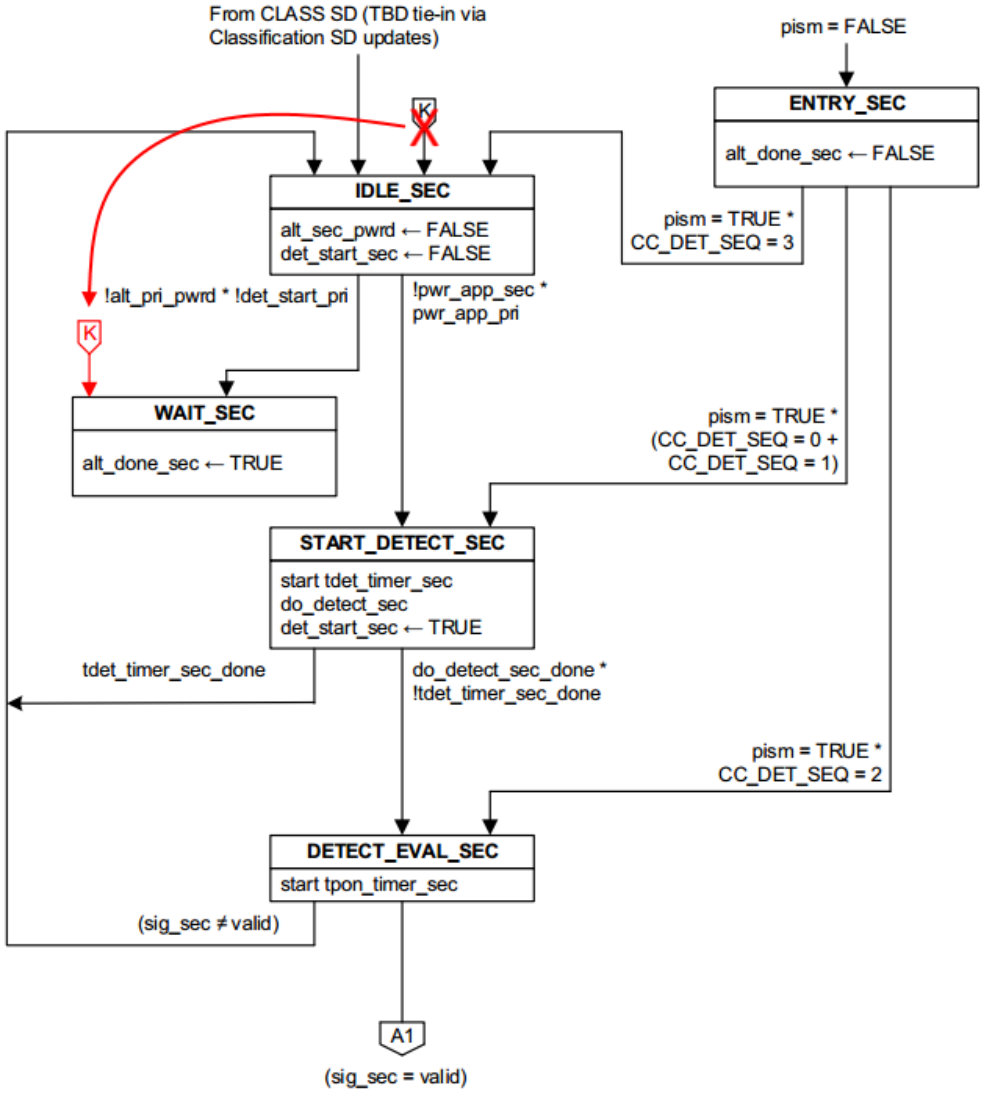
- The Alt state machines, now out-of-phase, will cycle through DETECT/POWER_ON and fault without ever returning to global IDLE **for as long as the PD remains connected**

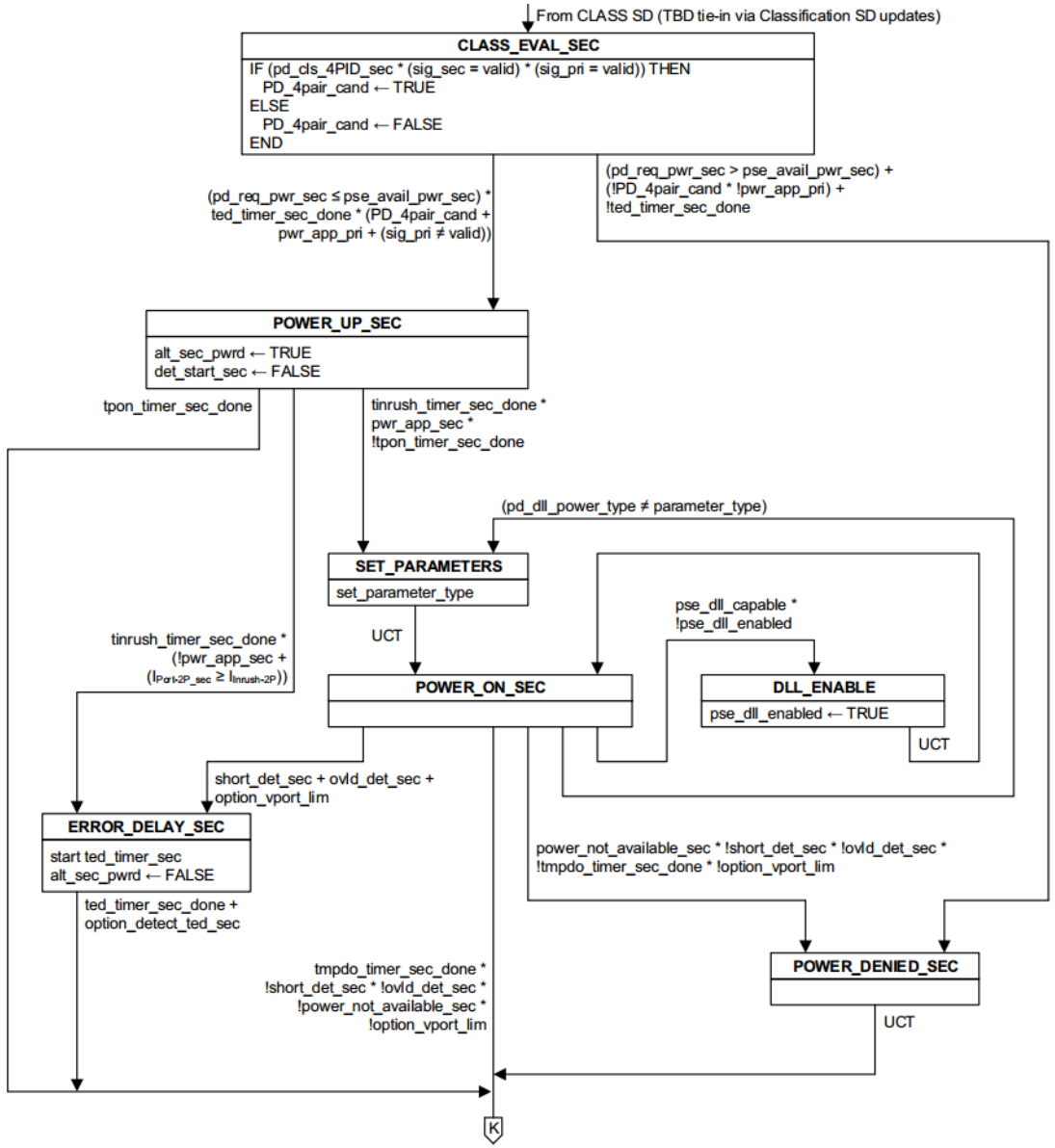
Proposed Solution



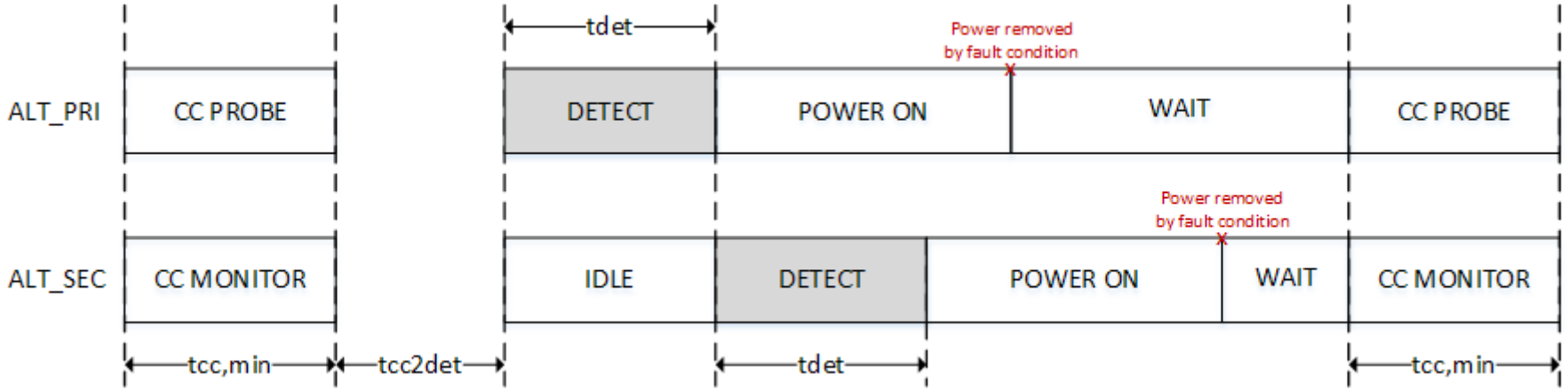


Proposed Solution, continued





Example Case with Proposed Solution



- Deadlock is resolved
- PSE is obliged to perform a new Connection Check prior to performing additional detections on either pairset