# MPS detection when MPS per pairset is not synchronized.

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Objectives

- To allow asynchronous PSEs to successfully detect the pair with maximum current when short MPS pulse (7msec) of single-signature PDs is used under unbalance conditions.

- To present simple solution(s).

- To guarantee Type 3 / 4 PSEs reasonable cost of MPS functionality for short MPS support.
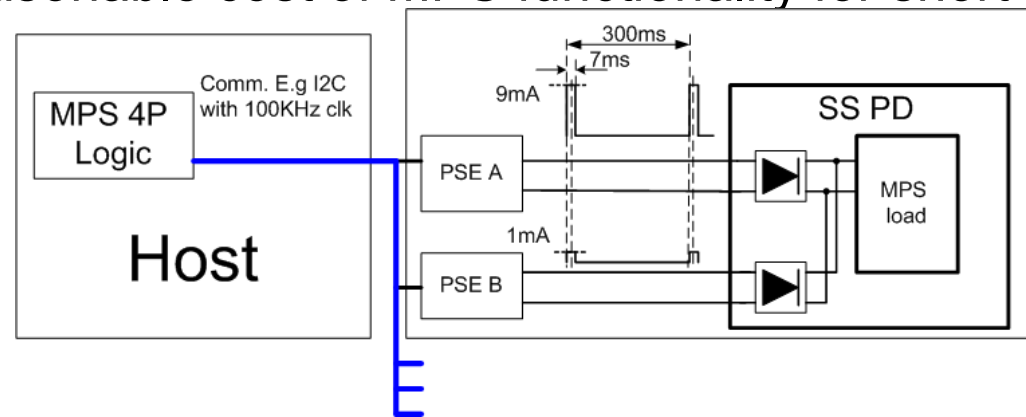
33.2.9.1.2 PSE DC MPS component requirements

....

A Type 3 or Type 4 PSE, when connected to a single-signature PD, shall monitor either the sum of Iport-2P of both pairs of the same polarity or the pairset with the highest IPort-2P current value and use the appropriate IHold level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than TMPDO.

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Proposed Baseline Text – Option 1

Change the following text in clause 33.3.5.2 page 132 lines 48-52 as follows.

Type 3 and Type 4 PDs may determine if the PSE they are connected to supports low MPS by measuring the length of the first class event. The default value for short_mps is FALSE. If it chooses to implement low MPS, a PD may set short_mps to TRUE if the first class finger is longer than TLCF_PD min and shall set short_mps to TRUE if the first class finger is longer than TLCF_PD max. A transition of short_mps from FALSE to TRUE shall occur at least 40/500/TBD ms after PD state MDI_POWER1.

500msec is the preferred number however 40msec can be used too if it helps to PDs.

Proposed Solution – Option 2

- TBD – Under discussions.

Use case details

- PSE Type 3 / 4 is constructed from two asynchronous 2P PSEs and connected to single signature PD Type 3 / 4.

- PD load is the minimum MPS current modulated with 7msec pulse over TMPDO and appears immediately after POWER_UP. i.e. there is no large DC load > MPS minimum value after POWER_UP.

- PSE current measurement of each pairset is not synchronized to each other.

- The function we need to implement according to **33.2.9.1.2**

  – To find if the current of pair A>B or B>A

  – Monitor the pair with maximum current and follow Ihold rules for this pair.

  – ***To do all of these <u>before</u> A or B will be disconnected due to no MPS signal caused by unbalance.***

Typical Implementation:
Finding which pair has the maximum current.

- sample pair A

- average pair A

- host need to read the sample (D1).

- sample pair B

- average pair B

- host need to read the sample (D2).

- Host to compare if A>B and follow MPS rules if to disconnect or not.

  - There are other possible implementations.

> The functions:
> 1. Finding the pair with maximum current:
> Must be done before the 1st MPS cycle.
> Otherwise the port may be disconnected.
>
> 2. Finding if current <> or than Ihold-2P need to be done on every TMPS+TNPDO cycle.
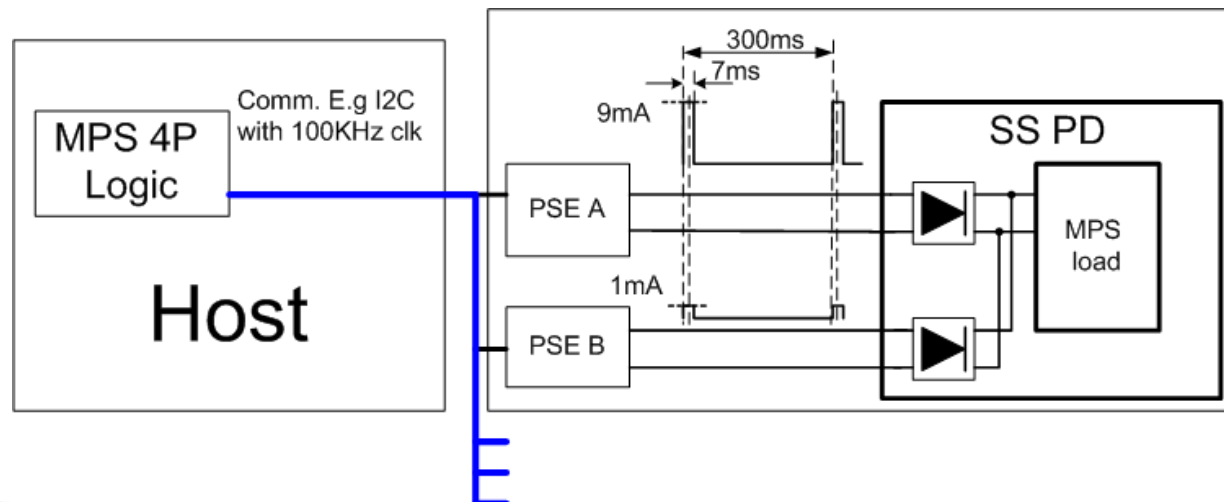
What are the potential problems?

- The MCU may miss the data pulses due to the fact that the sampling action is not synchronized in both the host and the PSE chip i.e. there is a time shift between generating the data on pairs A and B and between the acquisition of the data by the host for pairs A and B. *The problem became more apparent when the samples are actual real time current measurements (when samples need to be often refreshed) and not just 1/0 status. In order to resolve it, the MCU need to increase its sample rate to handle 7msec pulse width instead of 75msec.*

- The MCU sample rate need to be increased by a factor of 10 (from Type 1 support to Type 3 support) just for knowing if A>B which is needed just for the 1st TMPS+TMPDO cycle while it is not needed for the rest of the MPS timing. This is no cost effective solution.

- The above example can result with missing the pulses on A or B or both and result with failure to detect if A>B

Why there is a potential problem?
Missing detection of Type 3, 4 short pulse
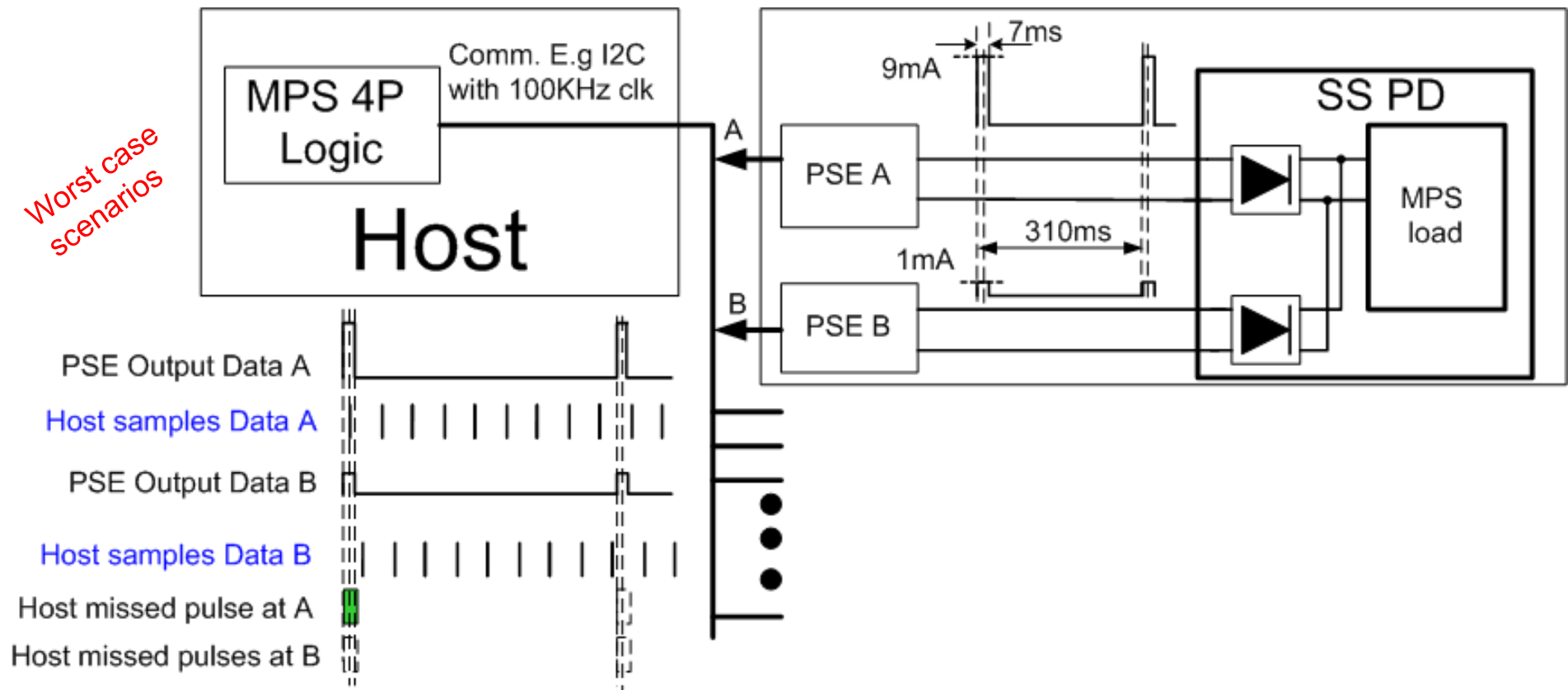
- In the example above, pulse data may be missed at Host. The condition for not missing the pulses:

- At the host $Ts<0.5*TMPS / (N*2*Number\_of\_ports)=0.5*7/(2*48)=0.036$msec. (no latch)

-     $Ts<0.5*T_{MPDO} / (N*2*Number\_of\_ports)=0.5*310/(2*48)=1.6$msec. (if latch)

- The objective is to allow implementations with latching time width much lower than TMPDO to allow real time current measurements. N>1 for filtering function. Results are for N=1.
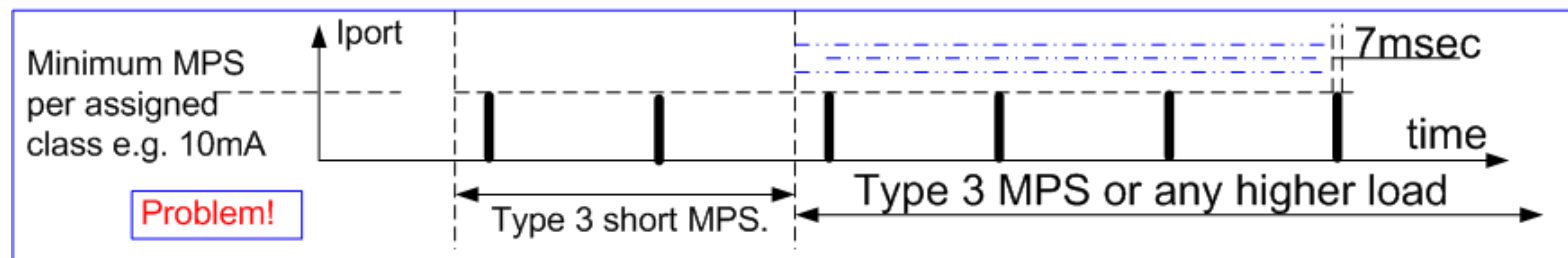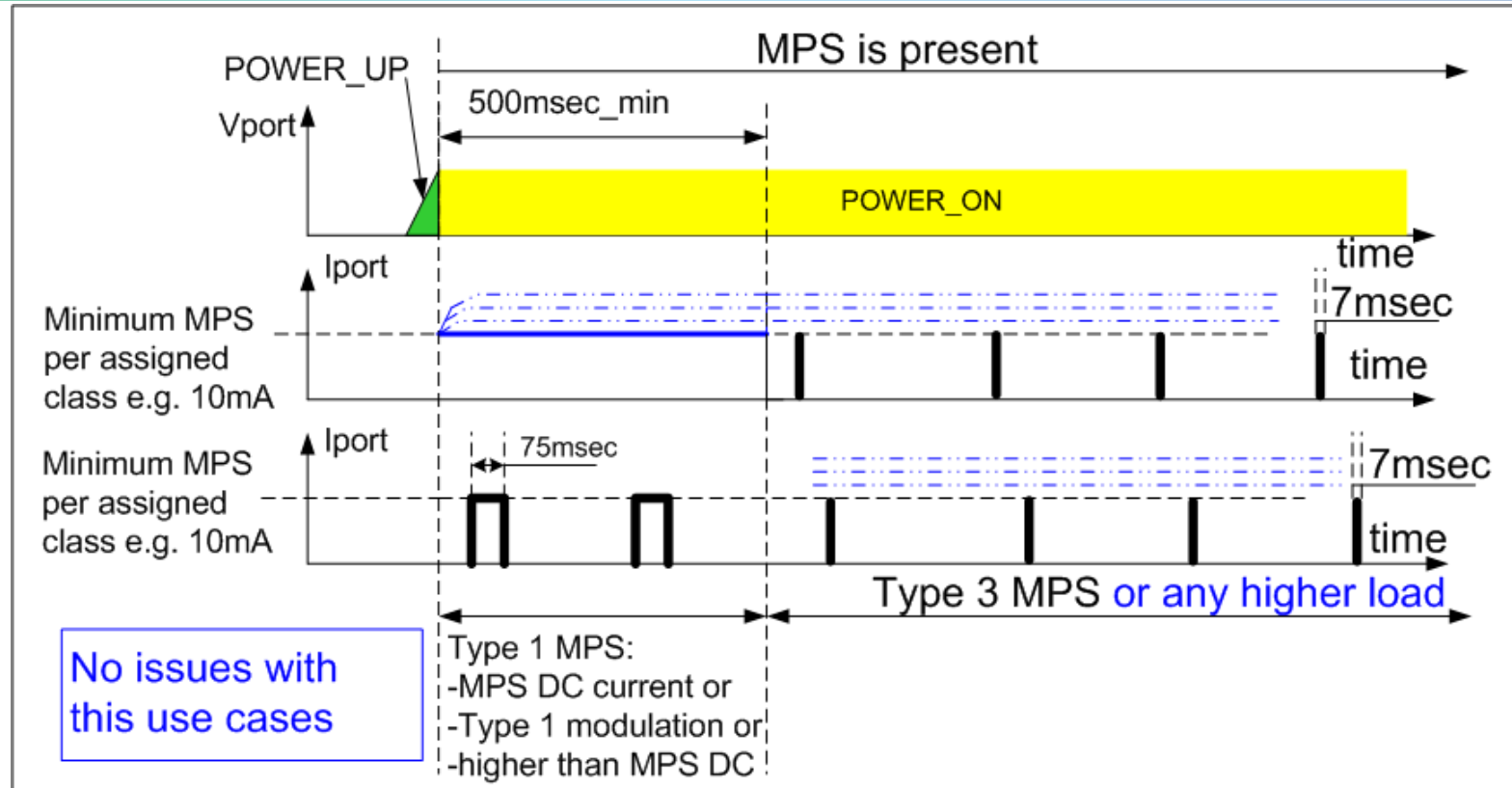
When there is no issues?
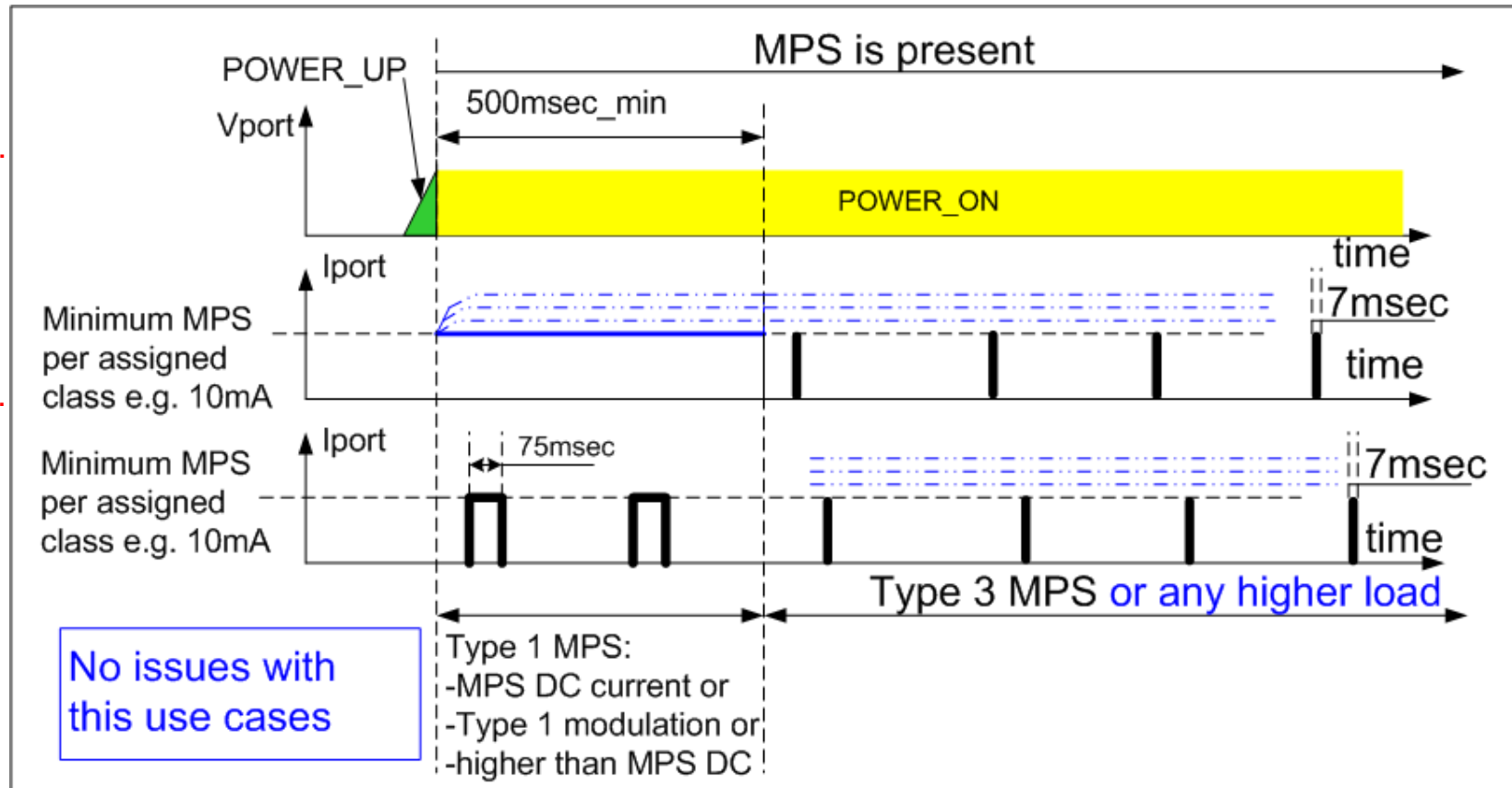
- During the 1st TMPS+TMPDO time, the PSE detects what is the pair with the maximum current and if MPS is valid or not valid.

- There is no issue if at the 1st 500msec after startup the lowest MPS appears for at least TMPS=75msec for every TMPDO+TMPS and afterwards, no changes in requirements.

- 500msec is derived from at least one TMPDO+TMPS cycle + margin.

When there is a potential issues?   -1

Note:
The drawings show PD Iport. The current is divided between the pairsets according to the unbalance. The current is measured per pairset.

■ Potential problem if short pulses appears right after startup so PSE may fail to find A>B.
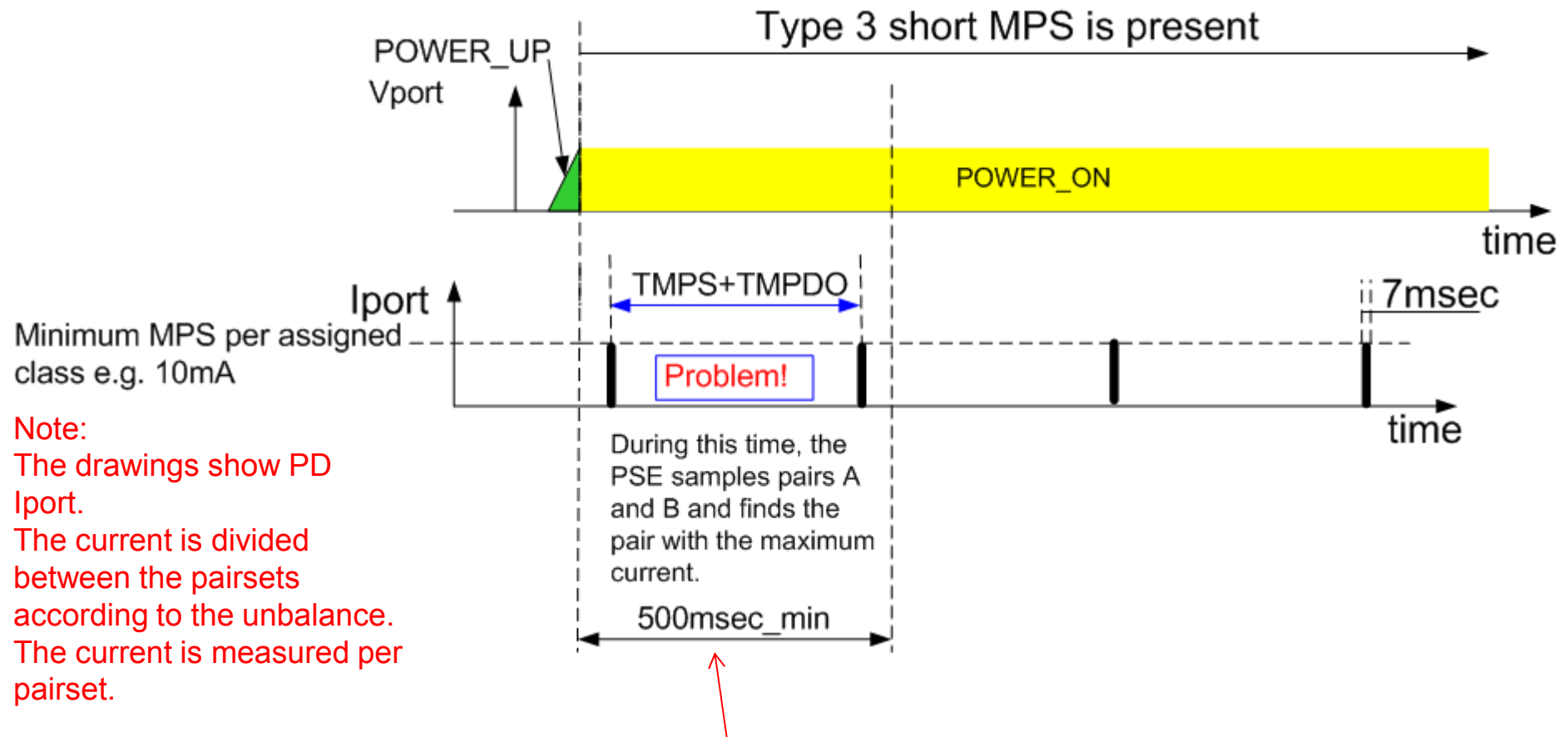
When there is a potential issues?   -2

Note:
The drawings show PD Iport.
The current is divided between the pairsets according to the unbalance.
The current is measured per pairset.

- During the 1st TMPS+TMPDO cycle, PSE determines what is the pair with the maximum current i.e. if A>B. according to the answer it applies the Ihold rules in **33.2.9.1.2.**

Possible solutions - 1

- Increasing the sample rate of PSE analog driver to be < 7msec/(2xN).
  - Issues: Possible. May not be so cost effective If the need is to use shared resources e.g. A/D for several ports instead of A/D for each port in heavily populated multiport systems. The host communication with PSE chips looks more limiting issue.

- Increasing the sample rate of host in addition to (1) to be < 7msec/(2*Nx(2*Number_of_Ports)) or 310msec/(2*Nx(2*Number_of_Ports)) pending the implementation if using latch or no at the host.
  - Issues: In either case of the calculations above, it looks impossible with the current low cost communication used between the host and to the PSE chips e.g. 100khz which generate about >>7msec sample rate between PSE chip samples in multiport system (and this is just for MPS while there are many functions that the host do..)

Possible solutions - 2

- To use comparators and filters to sample the peak and store the data in memory to be ready for the host.
  - Issues: If the need is to read absolute values of currents anyway so it is cost effective to use single A/D + digital filters for many ports and not to add comparators etc. in addition to each port.

- Require a PD to support at least Type-1 MPS values for 500msec/TBD after POWER_UP.
  - Issues: PDs will need to use Type 1 and Type-3 MPS values. However, a Type-3 PD already needs to be able support both MPS values to interoperate with all PSEs.
  - So far this one looks like the preferred solution.

- There are on going discussions to find solutions at PSE side as well.

Conclusions

The preferred solution (so far):

Type 3,4 PD that support short MPS, will enter short MPS mode in two steps:

Step1: after POWER_UP legacy MPS is used for at least 40msec/500msec/TBD

Step2: then low MPS may be used.

See proposed baseline on page 3 .

Summary-the advantages of the proposed solution

- **The proposed solution uses functions that are already required to be supported by PD Type 3, 4.**
  - PD is required to changes its MPS per the PSE assigned class.
    - PD type 3 will have the functionality of Type 1 and 2 as well

- **It doesn't add new requirements to PSE.**

- **It doesn't add additional burden on PD.**

- **It will guarantee high reliability of MPS detection at the PSE**

- **It will allow flexible design of PSEs**

- **Allow low cost circuitry for MPS detection in multiport PSEs systems**

Thank You

Annex

Probability to reliable measurements of current pulses are function of pulse width and current amplitude

- With Type 1 and 2 PDs implementing 75msec pulse current width, PSE measurements of the two channels with time shifting to determine the pair with maximum current is possible to guarantee (=cost effective) with Ts<<75mse.

2	PD Maintain Power Signature Time	T_{MPS_PD}	ms	75		1, 2	
						3, 4	short_mps = FALSE

- With Type 3 and 4 PDs implementing 7msec pulse current width, PSE measurements of the two channels with time shifting to determine the pair with maximum current is difficult to guarantee (not cost effective). Ts is required to be <<7msec including averaging to cancel noise at low current levels.

2	PD Maintain Power Signature Time	T_{MPS_PD}	ms	75		1, 2	
						3, 4	short_mps = FALSE
				7		3, 4	short_mps = TRUE

- Ts=sampling time

FAQ-1

- Q: Even unsynchronized PSE ICs could report if they see a current above a preset value.

- A:

- It depends on if they measure current value or report only logic state i.e. >value or <value and this value is not changed.

- Even if unsynchronized PSE ICs could report a value, the host will know it only after this pairset is sampled. And if the sample rate is too low it will be missed since the report from the PSE chip need to be updated.

- Only if the PSE chip sampling rate is <u>much better</u> than 7msec/2, and also the host sampling rate that need to be even much faster…they can do it. If it is not, it is impossible.

- To have sampling rate of <7msec/2 is not cost effective in multiport systems especially when you want to average the signal to cancel noise so the sample rate must be even faster i.e. Tsample = 7.5msec/(2*n), n>1.

FAQ-2 – Alternative solutions pro's/con's

- Q: Can PSE create a filtered peak detector to catch the peak MPS value.
- A: It can but it is not cost effective.
  - In most PSE chips the efficient way to do measurements (all measurements) is by using A/D that samples the port voltage/currents and then process it digitally.
  - Using comparators/Analog circuitry is minimized and there is no point to use both since in any case we need to measure and know absolute values and not just HIGH/LOW of many parameters.
  - In addition from signal processing point of view it is easier to use A/D and then process it digitally including filtering etc.

FAQ-3

- Q: What if I have separate A/D for each pairset?
- A:
- It will help with the PSE chip side.

- It will not help with the host with limited PSE chip information sampling rate.

- The problem is more relevant to PSEs that want to use shared A/D for many ports to reduce costs. Especially for multiport systems i.e. 24, 48 ports etc.

FAQ-4

- Does requiring that "The default value for short_mps is FALSE" for 500msec or 40msec add cost to PD?

- Regarding Timing functionalities, the PD is required to do the following:
  - A) Generating Type 1 MPS 75msec/300msec and Type 3/4 MPS 7msec/ 310msec.
  - B) Measure first class event (long or short)
  - C) To generate Tdelay=80msec for class 2 and above.

- So PD is already need to use timing circuitry and can reuse it to generate the a delay that will be cost effective for it.

Microsemi

FAQ-5

- If I detect the pair with the maximum current at the lowest MPS conditions i.e. at <u>low current</u>, and the PSE remembers it once it knows it e.g. at the first cycle of TMPS+TMPDO or at any time the current is at MPS levels, does the pair with maximum current can change polarity at high current?

- The polarity is important only at low current since the decision to maintain power or disconnect is done around Ihold range.

- At high current:
  - The unbalance is reduced dramatically.
  - The current per pair is much higher then Ihold.
  - The PSE must maintain power on each pairset.
  - There is no pulse sampling issues nor question about who is the pair with the maximum current….

- So why we care what is the polarity of unbalance at high current?