Comment

(TDL #162 from D2.1)

Adresses D2.2 comments: 88, 288, 280, 349, 237

1. Some updates are required for D2.2 for moving some of the normative requirements in Annex B to the standard body into 33.2.8.5.1 as requested by TDL #162.
2. As a result from (1), Annex 33B was updated accordingly and became informative

In addition the following updates were made:

3. Completing the missing numbers for long cable case in Table 33-1 due to the changes made to satisfy comment #162 from D2.1.
4. Additional updates due to moving from 71W to 71.3W, updating channel model at 100m per the changes made in D2.1 (striking the note in 33A.4)
5. Some text clarifications.
6. Updating values of Icon-2P_unb in Table 33-18 item item 5 for class 7 and 8.

Suggested Remedy:

Baseline starts here

Modify the text per the proposed baseline:

This is not part of the base line
The following is a proposal to move some of the important shall's from Annex B to to 33.2.8.5.1 as required by the TDL above. The title was updated with "effective" to sync it with all the spec where it used. See lines 25-26.

33.2.8.5.1 PSE PI pair-to-pair effective resistance and current unbalance

Type 3 and Type 4 PSEs that operate over 4 pairs are subject to unbalance requirements~~This section describes unbalance requirements for Type 3 and Type 4 PSEs that operate over 4 pair.~~ The contribution of PSE PI pair-to-pair effective resistance unbalance to the ~~effective~~ system end to end effective resistance unbalance, is specified by PSE maximum (RPSE_max) and minimum (RPSE_min) common mode effective resistance in the powered pairs of same polarity. See Figure 33-X1. Effective resistances of RPSE_min and RPSE_max include the effects of VPort_PSE_diff as specified in Table 33-18 and the PSE PI resistive elements. See definition and measurements in Annex 33B.

The PSE PI pair-to-pair effective resistance unbalance determined by RPSE_max and RPSE_min ensures that along with any other parts of the system, i.e. channel (cables and connectors) and the PD, the pairset with the highest ~~maximum pair~~ current including unbalance does not exceed ICon-2P-unb as defined in Table 33–18 during normal operating conditions. ICon-2P-unb is the current in the pairset with the highest current in the case of maximum unbalance and will be higher than ICon/2. ICon-2P-unb applies for total channel common mode pair resistance from 0.2 Ω to R_{Ch}. R_{Ch} is specified in 33.1.3.

RPSE_max and RPSE_min are specified and measured under maximum PClass_PD load ~~sourcing~~ conditions measured at the PD PI and over the V_{Port_PSE-2P} operating range.

The values of RPSE_max as a function of RPSE_min account for channel pair to pair unbalance and PD PI pair to pair unbalance at worst case unbalance conditions.

RPSE_min and RPSE_max for positive pairs are not necessarily the same values as for negative rail.

PSEs that comply with Equation 33-15 intrinsically meet unbalance requirements.

-Updates constants in Equation 33-15 as follows:
-Change in Equation 33-15 from "RPSE_max=" to "0<RPSE_max ≤…"

$$0 < R_{PSE\_max} \le \begin{Bmatrix} 2.182 \times R_{PSE\_min} - 0.040 & for & Class & 5 \\ 1.999 \times R_{PSE\_min} - 0.040 & for & Class & 6 \\ 1.904 \times R_{PSE\_min} - 0.030 & for & Class & 7 \\ 1.832 \times R_{PSE\_min} - 0.030 & for & Class & 8 \end{Bmatrix} \quad (33\text{-}15)$$

where

RPSE_max is, given RPSE_min, the highest allowable common mode effective resistance in the powered pairs of the same polarity.

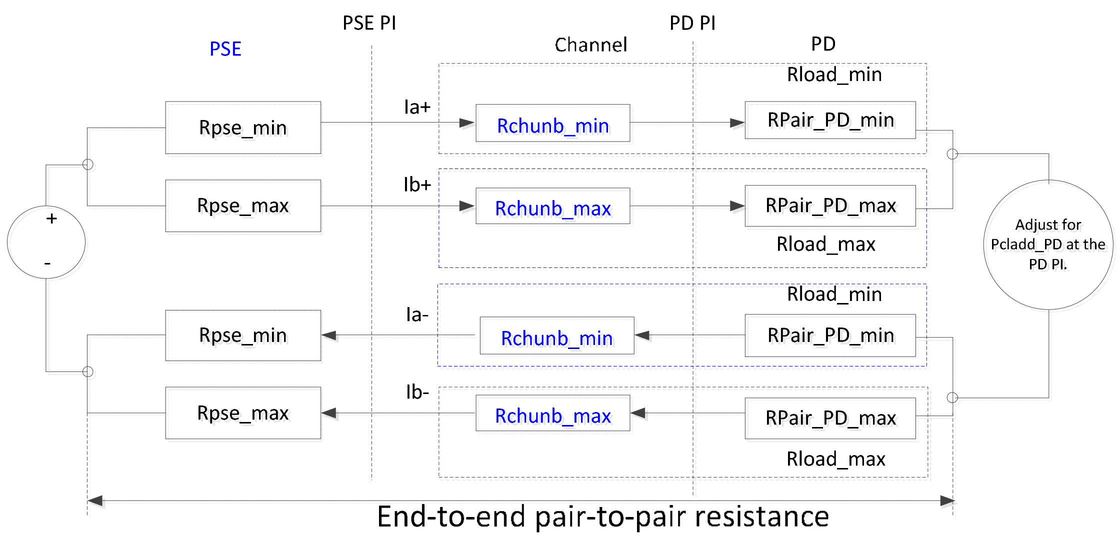
RPSE_min is the lower PSE common mode effective resistance in the powered pairs of the same polarity.

Common mode effective resistance is the resistance of the two wires and their components in a pair of the same polarity connected in parallel.

Figure 33-X1 illustrates the relationship between RPSE_max and RPSE_min effective resistances at the PSE PI as specified by Equation 33-15 and the rest of the end to end pair to pair effective resistance components.

A PSE shall not source more than Icon-2P_unb min on any pair when connected to a load as shown in Figure 33-X1, using values of Rload_min and Rload_max as specified in Table 33-X1.

Figure 33-X1~~B-1~~—PSE PI unbalance specification and E2EP2PRunb



The sum of Rchunb_min and Rchunb_max is Rchan-2P as described in Figure 33-X1 and as defined by the Pair-to-pair channel resistance unbalance requirement for 4-pair operation in 33A.4.

~~RPSE_max, RPSE_min and ICon-2P_unb shall be measured according to the tests **described in the normative Annex 33B.**~~

~~The following method may be used RPSE_min if the internal PSE circuits are not accessible or if the PSE is using active or passive current balancing circuitry that results in a variable effective resistance to control current unbalance. The current unbalance requirement shall be met for any pairs of the same polarity and with the load resistances per Table 33B–1~~. ~~A PSE which uses current balancing methods which effectively using lower R_{PSE_max} than required by Equation 33-15 and meets Icon-2P_unb requirements, by definition also meets Equation (33–15).~~

Figure 33B–4 shows a verification~~test~~ circuit for the current unbalance requirements measurement. Other methods for measuring RPSE_min and RPSE_max are described in Annex B.

Icon_2P_unb ~~max~~ and Equation 33-15 are specified for total channel common mode pair resistance Rchan-2P from 0.2Ω to 12.5Ω and worst case unbalance contribution by a PD as specified by 33A.5. ~~When the~~ PSEs optionally supporting ~~is tested for~~ channel common mode resistance less than 0.2 Ω (or if RChan is less than 0.1 Ω, See Figure 33A-X1, Figure 33-X1 and Figure 33-X2), i.e. 0 Ω < Rchan-2P < 0.2 Ω, the PSE should meet Icon_2P_unb requirements ~~shall be tested with~~when connected to (Rload_min – 0.5x Rchan-2P) and (Rload_max – 0.5x Rchan-2P) ~~to meet Icon_2P_unb requirements and~~ .The above can be met by using lower RPSE_max and/or higher RPSE_min than required by Equation (33–15).
Lower RPSE_max than required by Equation (33–15) is obtained by using smaller constants α and/or higher R_{PSE_min} ~~larger constant β~~ in the equation $R_{PSE\_max} = \alpha \times R_{PSE\_min} + \beta$ (See Equation 33-15).

Move Figure 33B-4 to this location with the following marked updates.

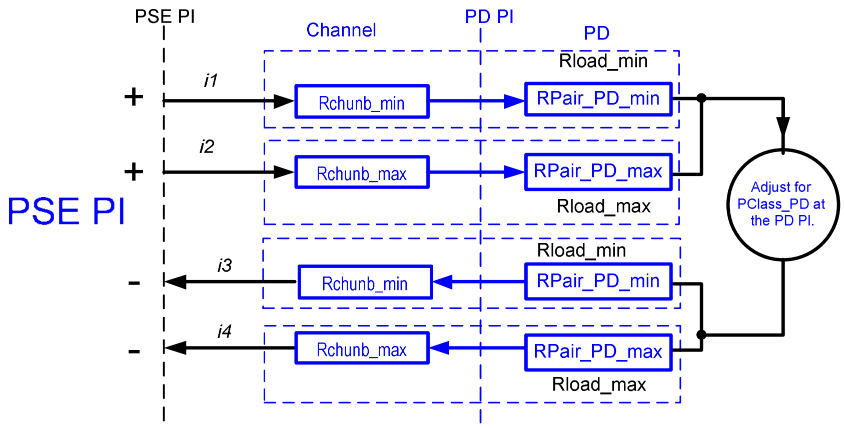


Figure 33-X2~~B–4~~—Current unbalance ~~test~~ verification circuit

The current unbalance ~~test~~ verification circuit is shown in Figure 33–X2. The evaluation method is described below:

1) Use Rload_min and Rload_max from Table 33-X1~~B-1~~ for Rload at low channel resistance conditions.
2) With the PSE powered on, adjust the load to Pclass_PD.
3) Measure I1, I2, I3 and I4.
4) Swap Rload_max, Rload_min, repeat steps ~~1~~ 2 and ~~2~~3.
~~5) Repeat for I3, I4.~~
~~6~~5) Verify that the current in any pair ~~each case~~ does not exceed Icon-2P_unb minimum in Table 33–18.
~~7~~6) Repeat steps ~~1~~2-5 ~~-6~~ for Rload_min and Rload_max from Table 33-X1~~B-1~~ for Rload at high channel resistance conditions.

-Add to Yair TDL to specify value tolerance and final significant digits of the resistance values since Table 33-X1 values are actual resistors in the test model and the objective is to set Icon-2P_unb accuracy to +/-5mA/TBD with the final significant bits.

Table 33B-~~1~~X1—Rload_max and Rload_min requirements

PSE Class	Rchunb~~CH~~_min, [Ω]	Rchunb~~CH~~_max, [Ω]	RPair_PD_min, [Ω]	RPair_PD_max, [Ω]	Rload_min, [Ω]	Rload_max, [Ω]	Additional Information
5	0.087	~~0.1~~ 0.101	0.641~~0.636~~	1.524~~1.528~~	0.728~~0.723~~	1.624~~1.628~~	Rload is at low channel resistance conditions. All resistances within ±1% range.
6			0.541~~0.536~~	1.187~~1.189~~	0.628~~0.623~~	1.288~~1.289~~	
7			0.486~~0.503~~	1.020~~0.99~~	0.573~~0.59~~	1.121~~1.09~~	
8			0.441~~0.457~~	0.896~~0.875~~	0.529~~0.544~~	0.996~~0.975~~	
5	5.405	6.250	0.708	1.031	6.113~~5.92~~	7.281~~7.19~~	Rload is at high channel resistance conditions. All resistances within ±1% range.
6			0.567	0.826	5.972~~5.78~~	7.076~~7~~	
7			0.494	0.720	5.898~~5.71~~	6.970~~6.87~~	
8			0.432	0.630	5.837~~5.65~~	6.882~~6.79~~	

Table 33-X1 specify the values of Rload_min and Rload_max components according to Equations 33-15B and Equation 33-15C. The values of RPair_PD_min and RPair_PD_max are given to allow calculations and measurement of PClass_PD at the PD PI.

Rload_min = RPair_ PD_min+Rchunb_min (33-15B)

Rload_max = RPair_PD_max+Rchunb_mx (33-15C)

Where

Rload_min is the minimum common mode effective load resistance in the powered pairs of the same polarity. Rload_min is composed from the minimal common mode channel resistance Rchunb_min and the minimum common mode effective PD PI resistance PD Rpair_PD_min.

Rload_max is the maximum common mode effective load resistance in the powered pairs of the same polarity. Rload_max is composed from the maximum common mode channel resistance Rchunb_max and the maximum common mode effective PD PI resistance Rpair_PD_max

RPair_ PD_min is the minimum common mode effective PD PI resistance that accounts for the effective resistance of resitive elements combined with PD pair to pair voltage difference and the effect of system end to end pair to pair resistance unbalance. See 33A-5.

RPair_PD_max is the maximum common mode effective PD PI resistance that accounts for the effective resistance of resitive elements combined with PD pair to pair voltage difference and the effect of system end to end pair to pair resistance unbalance. See 33A-5.

Rchunb_min is the minimum common mode channel resistance in the powered pairs of the same polarity from PSE PI to PD PI per the model described in Figure 33B-4. See 33A-4.

Rchunb_max is the maximum common mode channel resistance in the powered pairs of the same polarity from PSE PI per the model described in Figure 33B-4. See 33A-4.

33A.3 Intra pair resistance unbalance

Make the following changes:

Operation for all PSE and PD Types requires that the resistance unbalance be 3% or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33A–1):

$$\left\{\frac{(R\max - R\min)}{(R\max + R\min)}\times 100\right\}_{\%} \qquad (33A\text{–}1)$$

where

Rmax is the resistance of the pair conductor with the highest resistance

Rmin is the resistance of the pair conductor with the lowest resistance. ~~Common mode resistance is the resistance of the two wires in a pair (including connectors), connected in parallel.~~

33A.4 Pair-to-pair channel resistance unbalance requirement for 4-pair operation

Make the following changes:

Operation using 4-pair requires the specification of resistance unbalance between each two pairs of the channel, not greater than 100 milliohm or resistance unbalance of 7% whichever is a greater unbalance. Resistance unbalance between the channel pairs is a measure of the difference of resistance of the common mode pairs of conductors used for power delivery. Channel pair-to-pair resistance unbalance is defined by Equation (33A–2).

The resistance of the common mode pairs of conductors and connectors ~~RCH_min~~ Rchunb_min and ~~RCH_max~~ Rchunb_max are described by Figure 33A-XX.

Not part of the baseline
Figure 33A-XX was added to differentiate between R_{ch} term used from PSE PI to PD PI and back and the channel resistance of pair of wires and their connectors from PSE PI to PD PI (one way) when they are unbalanced are used in this Annex and all related P2Punb clauses.

Add Figure 33A-X1

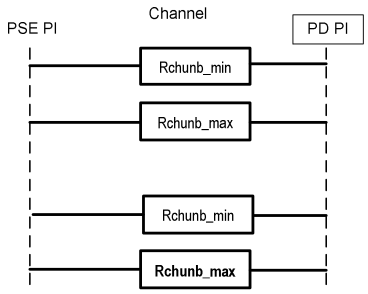


Figure 33A-X1 – Common mode Pair-to-pair channel resistance unbalance

Replace Rch_max and Rch_min with Rchunb_min and Rchunb_max as follows.

$$\left\{\frac{(Rchunb\_\max - Rchunb\_\min)}{(Rchunb\_\max + Rchunb\_\min)}\times 100\right\}_{\%} \qquad (33A\text{-}2)$$

Channel pair-to-pair resistance difference is defined by Equation (33A–3):

$$\{Rchunb\_\max - Rchunb\_\min\} \qquad (33A\text{-}3)$$

where

~~*Rch_max*~~ Rchunb_max is the sum of channel pair ~~elements~~ components with highest common mode resistance from PSE PI to PD PI.

~~*Rch_min*~~ Rchunb_min is the sum of channel pair components ~~elements~~ with lowest common mode resistance from PSE PI to PD PI. ~~Common mode resistance is the resistance of the two wires in a pair (including connectors), connected in parallel.~~

Common mode resistance is the resistance of the two wires in a pair (including connectors), connected in parallel.

Annex 33B

This is not part of the baseline
The important shalls moved from Annex B to PSE PI unbalance section in 33.2.8.5.1 and Annex 33B was updated accordingly.

(~~normative~~Informative) ***Insert Annex 33B after Annex 33A as follows:***

PSE PI pair-to-pair resistance/current unbalance

33B.1 Introduction

End to end pair-to-pair resistance/current unbalance (E2EP2PRunb) refers to current differences in powered pairs of the same polarity. Current unbalance can occur in positive and negative powered pairs when a PSE uses all four pairs to deliver power to a PD.

Current unbalance requirements (RPSE_min, RPSE_max and Icon-2P_unb) of a PSE ~~shall be~~is met with Rload_max and Rload_min as specified ~~by~~ in Table 33B-1.

A compliant unbalanced load, Rload_min and Rload_max consists of the channel (cables and connectors), and PD effective resistances, including the effects *(or influence)* of PSE PI effective resistance as a function of the system end-to-end unbalance.

This is not part of the baseline
The following part was moved to 33.2.8.5.1

~~Icon_2P_unb max and Equation 33-15 are specified for total channel common mode pair resistance~~ ~~$R_{Ch\text{-}2P}$~~ ~~from 0.2Ω to 12.5Ω and worst case unbalance contribution by a PD as specified by 33A.5. When the PSE is tested for channel common mode resistance less than 0.2 Ω, i.e. 0 Ω < Rchan-2P < 0.2 Ω, the PSE shall be tested with (Rload_min – 0.5xRchan-2P) and (Rload_max – 0.5xRchan-2P) to meet Icon_2P_unb requirements and using lower Rpse_max than required by Equation (33–15).~~
~~Lower Rpse_max than required by Equation (33–15) is obtained by using smaller constants α and larger constant β in the equation~~ ~~$R_{PSE\_max} = \alpha \times R_{PSE\_min} + \beta$~~.

Equation (33–15) is described in 33.2.8.5.1, specified for the PSE, assures that E2EP2PRunb will be met in the presence of all compliant, unbalanced loads (Rload_min and Rload_max) attached to the PSE PI.

Figure 33-X1~~B-1~~ illustrates the relationship between effective resistances at the PSE PI as specified by Equation (33–15) and Rload_min and Rload_max as specified in Table 33B-1.

There are ~~three~~ two alternate verification ~~test~~ methods for RPSE_max and RPSE_min and determining conformance to Equation (33–15) and to Icon-2P_unb.

Measurement methods to determine RPSE_max and RPSE_min and Icon-2P_unb are defined in 33B.1~~,~~ and 33B.2.~~, and 33B.3.~~

Delete Figure 33B-1. It was updated and moved to 33.2.8.5.1

Delete Table 33B-1. It was updated and moved to 33.2.8.5.1

~~**Figure 33B-1—PSE PI unbalance specification and E2EP2PRunb**~~

~~Table 33B-1—Rload_max and Rload_min requirements~~

~~PSE Class~~	~~RCH_min, [Ω]~~	~~RCH_max, [Ω]~~	~~RPair_PD_min, [Ω]~~	~~RPair_PD_max, [Ω]~~	~~Rload_min, [Ω]~~	~~Rload_max, [Ω]~~	~~Additional Information~~
~~5~~	~~0.087~~	~~0.1~~	~~0.636~~	~~1.528~~	~~0.723~~	~~1.628~~	~~Rload is at low channel resistance conditions~~
~~6~~	~~0.087~~	~~0.1~~	~~0.536~~	~~1.189~~	~~0.623~~	~~1.289~~	
~~7~~	~~0.087~~	~~0.1~~	~~0.503~~	~~0.99~~	~~0.59~~	~~1.09~~	
~~8~~	~~0.087~~	~~0.1~~	~~0.457~~	~~0.875~~	~~0.544~~	~~0.975~~	
~~5~~					~~5.92~~	~~7.19~~	~~Rload is at high channel resistance conditions~~
~~6~~					~~5.78~~	~~7~~	
~~7~~					~~5.71~~	~~6.87~~	
~~8~~					~~5.65~~	~~6.79~~	

33B.2 Direct RPSE measurement

If there is access to internal circuits, effective resistance may be determined by sourcing current in each path corresponding to maximum PClass operation, and measuring the voltage across all components that contribute to the effective resistance, including circuit board traces and all components passing current to the PSE PI output connection. The effective resistance is the measured voltage Veff, divided by the current through the path e.g. the effective value of R_{PSE_min} for i1 is $R_{PSE\_min} = V_{eff1}/i_1$ as shown in Figure33B-2.

Update Figure 33B-2 as follows:

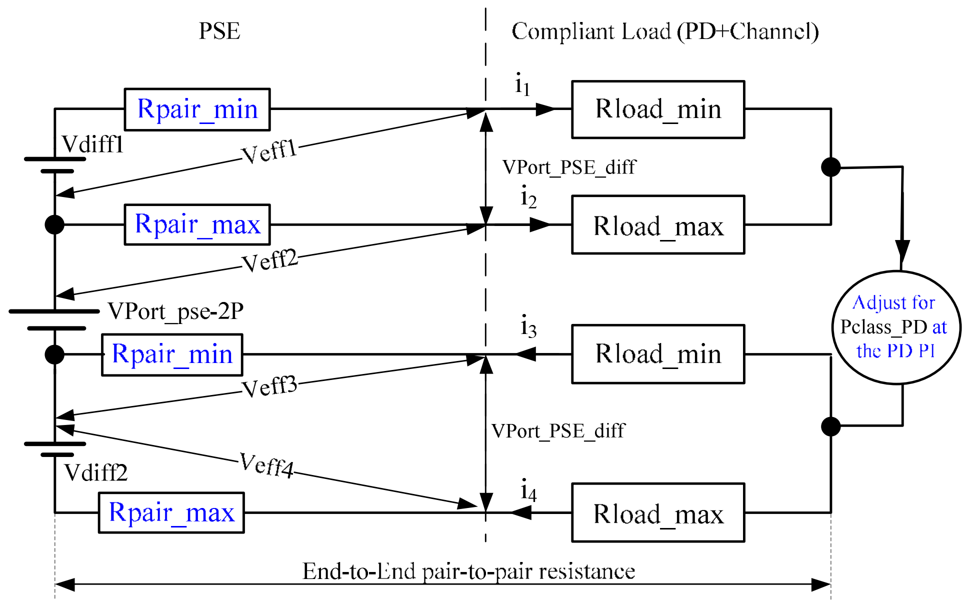


Figure 33B–2—Direct measurements of effective RPSE_max and RPSE_min

33B.3 Effective resistance Rpse measurement

Add to TDL: Ken to verify that the following verificationmodel works in simulations

Figure 33B-3 shows a possible ~~test~~verification circuit for effective resistance measurements on a PSE port for evaluating conformance to Equation (33–15) if the internal circuits are not accessible. In Figure 33B-3, the positive pairs of the same polarity are shown as an example. The same concept applies to the negative pairs.

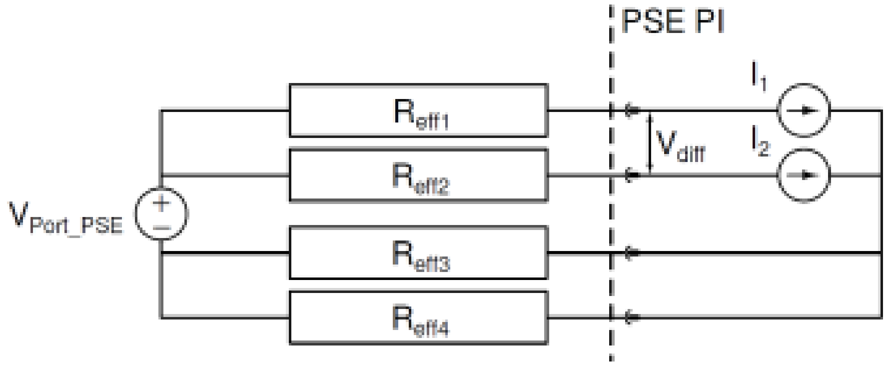


Figure 33B-3 – Effective resistance ~~test~~verification circuit

The Effective Resistance verification~~Test~~ Procedure is described below:

1) With the PSE powered on, set the following current values
   a. 10 mA < I_2 < 50 mA
   b. $I_1 = 0.5 \times (P_{max}/V_{port}) - I_2$
2) Measure V_{diff}.
3) Reduce I_1 by 20% (=I_1'). Ensure I_2 remains unchanged.
4) Measure V_{diff}' in the same mannar as V_{diff}..
5) Calculate R_{eff1}: $R_{eff1} = [(V_{diff}) - (V_{diff}')] / (I_1 - I_1')$
7) Repeat procedure for R_{eff2}, with I_1, I_2 values swapped.
8) Repeat procedure for R_{eff3}, R_{eff4}.
9) Evaluate compliance of $R_{eff1}$and R_{eff2} with Equation (33–15). Evaluate compliance of R_{eff3} and R_{eff4} with Equation (33–15).

The effective resistance verification ~~test~~ method applies to the general case. If pair-to-pair balance is actively controlled in a manner that changes effective resistance to achieve balance, then the current unbalance measurement method described in **33.2.8.5.1** ~~33B.4 shall be~~ is used.

33B.4 was moved to 33.2.8.5.1 per the TDL

Update Table 33-18 item 5, Icon-2P_unb page 118 lines 50 and 51:

Class 7: Change from 777mA to 781mA

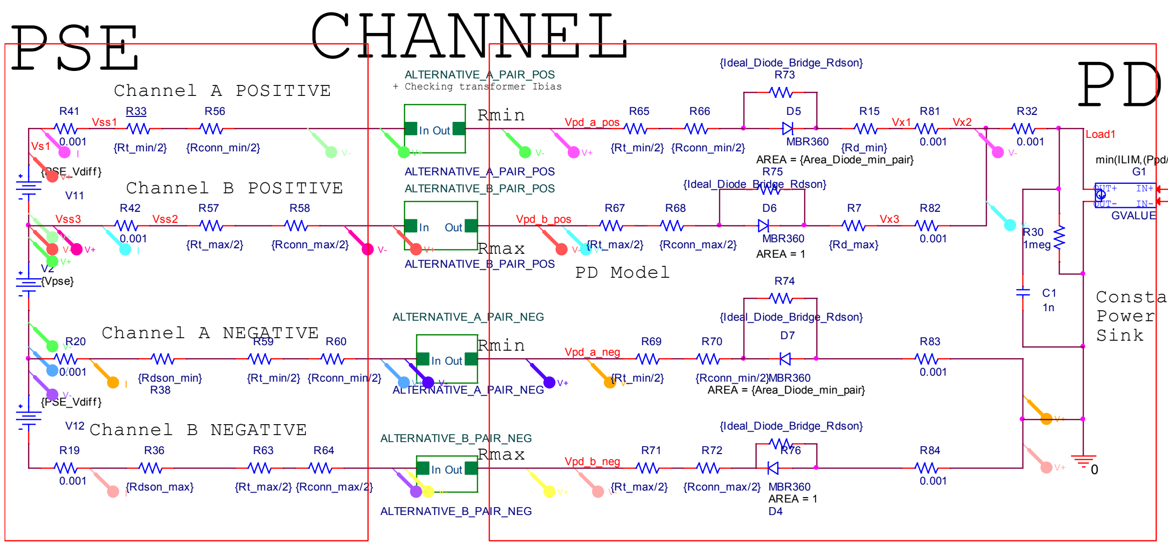
Class 8: Change from 925mA to 932mA

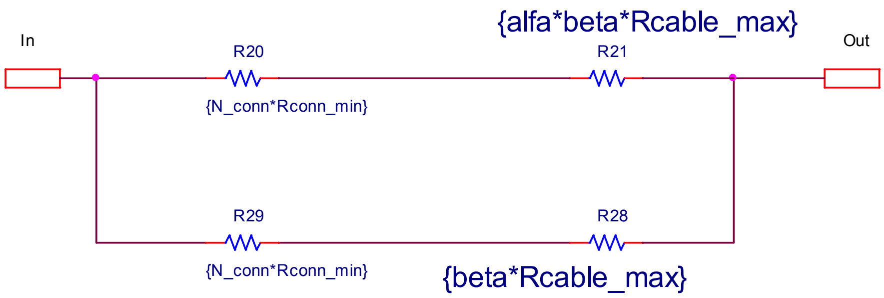
END OF BASELINE

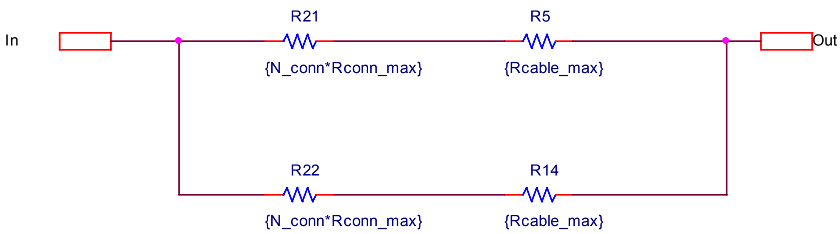
Annex A: 4-pairs spice simulation model parameters used to specify IEEE802.3bt D2.2 requirements.

The following values of the 4-pair model where used to set the specification requirements of the PSE PI and the PD PI unbalance requiremenrs as a function of the total system end to end pair to pair effective resistance/current unbalance.

#	Parameter	Units	Class 5-6		Class 7-8		Notes
			Min	Max	Min	Max	
1	Vpse	Vdc	50.31	----	52.31	----	PSE voltage source, no load voltage
2	Ppd	W	40, 51	----		----	PD input power measured at the PD PI
3	Ppd extended power	W	59.7	----	89.4	----	PD input power measured at the PD PI
4	Lcable	m	2.65	100	2.65	100	Cable and cordage legth.
5	Diode AREA2	-	10		10		Diode simulation parameter. Set the PD Vdiff compare to the diode in the pair with minimum resistance that is set to AREA=1. As a result, PD Vdiff is set to Vdiff=(n*K*T/q)*LN(Is2/Is1) while Is2=Is1 (same diodes only AREA parameter is changed) . As a result, AREA2/AREA1 sets PD Vdiff. For AREA2=10 we will get PD Vdiff =60mV measured at IF=10mA (PD Vdiff is the pair to pair PD voltage difference casued by the forward voltage difference between two diodes on pairs of the same polarity. PD Vdiff is determined at low current (few mA range). When current increase the effect of PD Vdiff on the PD contribution to its PI unbalance and to the total system unbalance is reduced. The use of diodes with higher Vdiff, will increase the PD unbalance at high currents. Therefore a limit of 60mV for PD Vdiff was set at 10mA.
	Diode AREA1	-	1	----	1		Diode simulation parameter set to AREA 1. This diode is located at the pair with maximum resistance.
	Cordage Resistivity	Ω/m	0.0926	----	0.0926	----	Used for short channel length with Lacble =2.65m simulations
	Cable resistivity	Ω/m	0.074	----	0.074	----	Used for short channel length with Lacble =2.65m simulations
	Nuber of connectors	-	0	----	0	----	Used for short channel length with Lacble =2.65m simulations
	Cordage Resistivity	Ω/m	0.123	Ω	0.123	----	Used for long channel length with Lacble =100m simulations
	Cable resistivity	Ω/m	0.123	Ω	0.123	----	Used for long channel length with Lacble =100m simulations
	Nuber of connectors	-	4	----	4	----	Used for long channel length with Lacble =100m simulations
	Minimum Channel Resistance wire 1	Ω	=α*β*Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity)+N*Rconn_min				1st wire of the pair withminimum resistance α=(1-pair_Runb)/(1+pair_Runb)=0.96. Pair_Runb=0.02. β=(1-pair2p_Runb)/(1+pair2p_Runb)=0.9. Pair2p_Runb=0.05 for IEEE802.3bt D2.1 and was changed to β=(1-pair2p_Runb)/(1+pair2p_Runb)=0.8867. Pair2p_Runb=0.06 to ensure total channel pair to pair resistance unbalance of 7% per Annex 33A.4. Wire length is measured from PSE PI to PD PI (not round loop). Each pair of the same polarity has two wires (wire 1 and wire 2) are connected in parallel and form common mode resistance of that pair. In the positive pairs, we have two pairs with the same voltage polarity, the 1st pair is set to minum resistance and the 2nd pair is set to maximum resistance. The same applies to the negative pairs.
	Minimum Channel Resistance wire 2	Ω	=β*Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity))+N*Rconn_min				
	Maximum Channel Resistance wire 1 and wire 2		Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity)				
	PSE Vdiff	mV	10	----	10	----	
	Rt	Ω	0.12	0.13	0.12	0.13	Transformer winding resistance
	Rconn	Ω	0.03	0.05	0.03	0.05	Connector resistance
	Rdson	Ω	0.07	0.1	0.07	0.1	
	Rsense	Ω	0.0225	0.25	0.0225	0.25	







Simulation results on the positive pairs Done for IEEE802.3bt D2.2 for reference.

Cable Length (m)	2.65m	100m	Spec in D2.2	Notes
Cable max wire resistance (Ω)	0.2	12.5		
Number of connectors	0	4		
PSE Vdiff (mV)	10	10		
PD Vdiff (mV)	60	60		
Pair with maximum current (mA) on (I(R41))	Imax,	Imax,	Imax=Icont_2P_unb	Positive pairs
Class 5	547.07	483.86	550(*)	Maximum current is at short cable length.
Class 6	678.65	638.83	682(*)	Maximum current is at short cable length.
Class 7	780.85	764.43	781(**)	Maximum current is at short cable length.Different from D2.1 results (maximum current was at long cable) due to different model parameters values that was updated at D2.1 meeting.
Class 8	911.62	911.61(*)	931(***)	Maximum current is at long cable length.

(*) Spec was not changed in D2.2 for class 5 and 6 in order to finish first the significant digits issues.
(**) (Spec was changed in D2.2 for class 7 to update per the updated sim results.
(**) Spec was changed in D2.2 for class 8 to allow PD margin for Extended Class 8 use case. D2.1 spec was 925mA.

Annex B – Calculating RPSE_min from Equation 33-15

RPSE_max is a function of RPSE_min according to Equation 33-15 structure RPSE_max =α * RPSE_min +β.

In addition we need to ensure that RPSE_max> RPSE_min and Rpse_max>0.

$R_{PSE\_\max} \le \alpha \cdot RPSE\_\min + \beta$ Equation 33-15 in IEEE802.3bt D2.2

Change Equation 33-15 in D2.3 to:

$$0 < R_{PSE\_\max} \le \alpha \cdot RPSE\_\min + \beta$$