PSE PI P2PIunb Infrastructure requirements completion

Comment:

The following completes the infrastructure work needed for PSE PI P2PRUNB.

1. In previous drafts we add the equations needed for designing Rpair_max/min relationship in order to guarantee compliance with system E2EP2PIunb/Runb objectives.

As we already know, E2EP2P_Iunb is function of power level and we care only for the worst case condition at maximum system power level. E2EP2P_Iunb is decreased when load power is increased.

So far we have supplied the requirements for Type 3 and Type 4 maximum power i.e. class 6 and 8 and we need to complete it for class 5 and 7 as well. This part will be addressed by expanding equation 33-4b to include requirements for class 5 and 7 and adding to Table 33-11 item 4a the Icont-2P-unb values for class 5 and 7.

2. In order to check for compliance, we need test setup that will include Channel and PD effective resistance to ensure that the PSE under test meets the requirements. This part will be cover by Annex B which is a normative Annex.

See next suggested Remedy.

<u>Suggested Remedy:</u>

1. Replace the TBD in 33.2.7.4b (Test setup and test conditions for RPair_max and RPair_min)
With: See Annex B.

2. Replace equation 33-4b with the missing parts required for each PSE power class as follows:

$$R_{Pair\_max} = \begin{cases} k1 \text{ x } R_{Pair\_min} + a1 & \text{for class 5} \\ 1.894 \text{ x } R_{Pair\_min} - 0.053 & \text{for class 6} \\ k2 \text{ x } R_{Pair\_min} + a2 & \text{for class 7} \\ 1.760 \text{ x } R_{Pair\_min} - 0.042 & \text{for class 8} \end{cases}$$

Note: meeting equation 33-4b for class N (N=6,7 and 8) covers all classes below N.

[Editor Note (to be removed prior to publication): k1,k2,a1 and a2 parameters will be specified in the next draft.]

3. Add to Table 33-11 item 5a parameter Icont-2P-unb additional rows for class 5 and 7. This completes the maximum Icont-2Punb values for all classes for PSE and PD PI compliance tests

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
4a	Pair set current due to E2ERunb within E2ERunb range for Class 5	$I_{Con\text{-}2P\text{-}unb}$	A		TBD	3	See 33.2.7.4a
	Pair set current due to E2ERunb within E2ERunb range for Class 6				0.668[1]	3	
	Pair set current due to E2ERunb within E2ERunb range for Class 7				TBD	4	
	Pair set current due to E2ERunb within E2ERunb range for Class 8				0.931[1]	4	

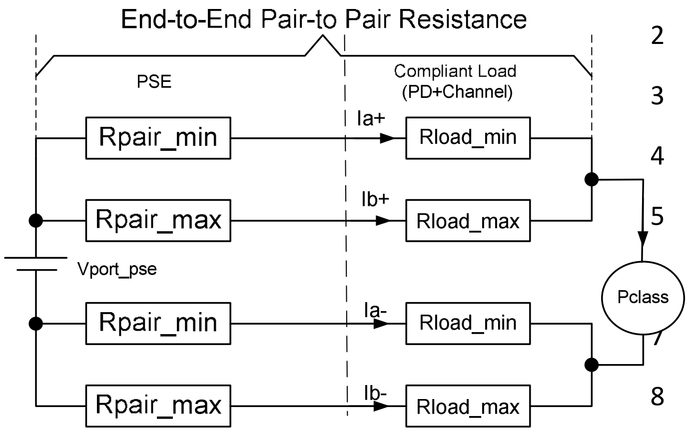
4. Insert Normative Annex 33B to the Annex section.
5. Insert Informative Annex 33F to the Annex section

ANNEX 33B [Normative] PSE PI Pair-to-Pair Resistance/Current Unbalance

Pair-to-pair current unbalance refers to current differences in powered pairs of the same polarity. Current unbalance can occur in positive powered pairs, negative powered pairs, or both when a system uses all four pairs to 4-pair power when both PSE Alternatives provide power to both PD Modes.

Current unbalance of a PSE shall be met with Rload_max and Rload_min as specified by table Yuval_1. The details for derivation of Rload_max and Rload_min can be found in Annex 33F.
A compliant unbalanced load consists of the channel (cables and connectors) and the PD effective resistances.

Equation 33-4b is described in 33.2.7.4a, specified for the PSE, assures that E2EP2PRunb will be met in a compliant 4-pair powered system. Fig. 33B-1 illustrates the relationship between PSE PI equation 33-4b and E2EP2PRunb.



$$R_{pair\_max} \le R_{pair\_min} \times U + K_{pse} \quad \textit{(33-4)}$$

U=(1+E2EP2P_Runb)/(1+E2EP2P_Runb)

Fig. 33B-1 PSE PI Unbalance specification and E2EP2PRunb

PSE Class	Rload_min, [Ω]	Rload_max, [Ω]
5	TBD	TBD
6	0.632	1.250
7	TBD	TBD
8	0.530	0.975

Table Yuval_1: Rload_max and Rload_min requirements.

Equation 33-4b specifies the PSE effective resistances required to meet E2EP2PRunb in the presence of all compliant, unbalanced loads attached to the PSE PI. There are 3 alternate test methods for Rpse_max and Rpse_min and determining conformance to equation 33-4b

33B.1 direct measurements of Rpse_max and Rpse_min

If there is access to internal circuits, effective resistance may be determined by sourcing current in each path corresponding to maximum Pclass operation, and measuring the voltage across all components that contribute to the effective resistance, including circuit board traces and all components passing current to the PSE PI output connection. The effective resistance is the measured voltage Veff, divided by the current through the path e.g. the effective value of Rpair_min =Veff1/*i1* as shown in Fig. 33-B2.

The two sections that follow, 33B.2 and 33B.3 illustrate two other possible measurements of PSE effective resistances for Rpse_max and Rpse_min equation 33-8 verification, if the internal circuits are not accessible.

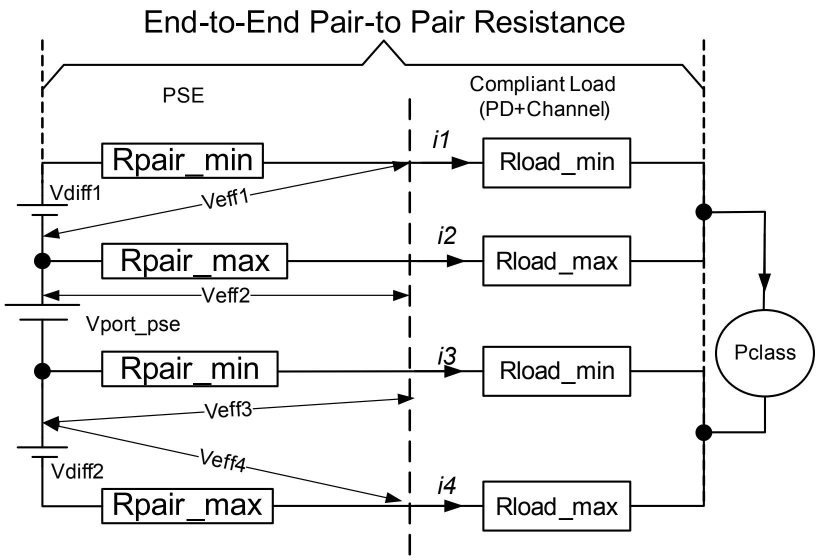


Fig. 33B-2 direct measurements of effective Rpse_max and Rpse_min

33B.2 Effective Resistance Measurement Method by measurement of current unbalance under worst case pair-to-pair load conditions

Figure 33-B3 shows a possible test circuit for effective resistance measurements on a PSE port for evaluating conformance to Equation 33-4b.

The Effective Resistance Test Procedure is described below:

1) With the PSE powered on, set the following current values
   a. $10mA < I_2 < 50mA$
   b. $I_1 = 0.5*(Pclass_{max}/Vport) - I_2$.
2) Measure Vdiff across V_1, V_2.
3) Reduce I_1 by 20% ($=I_1$'). Ensure I_2 remains unchanged.
4) Measure Vdiff' across V_1, V_2.
5) Calculate R_{eff1}:
6) $R_{eff1} = [(Vdiff) – (Vdiff')] / (I_1 – I_1')$
7) Repeat procedure for R_{eff2}, with I_1, I_2 values swapped.
8) Repeat procedure for R_{eff3}, R_{eff4}.
9) Evaluate compliance with Equation 33-4b.

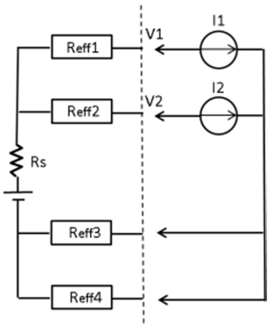


Fig. 33B-3 Effective resistance Test Circuit

The Effective resistance test method applies to the general case; if pair-to-pair balance is actively controlled in a manner that changes effective resistance to achieve balance, then the Current Unbalance Measurement Method described in 33B3.3 should be used.

33B.3 Current Unbalance Measurement Method

Unbalanced load resistances must be selected per Table Yuval_1 . Current unbalance must be met for any pair-to-pair resistances meeting the equation; selected resistance values which provide adequate verification are dependent upon PSE circuit implementation and as such are left to the designer.

Fig. 33B-4 shows a test circuit for the current unbalance measurement.

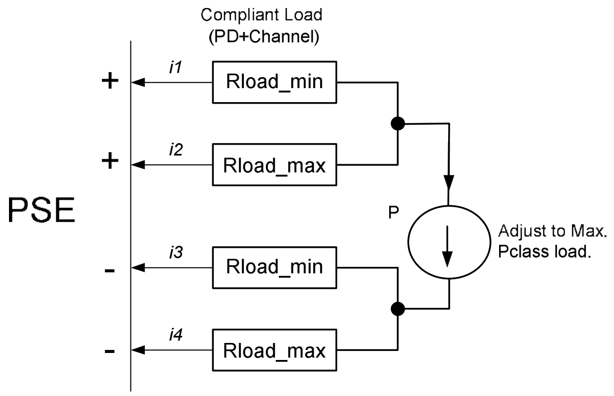


Fig. 33B-4 Current Unbalance Test Circuit

The current unbalance test method is described below:

1) Use Rload_min and max from Table Yuval_1
2) With the PSE powered on, adjust the load for Max. Pclass power at the PSE
3) Measure i_1, i_2
4) Swap R_max, R_min, repeat steps 1 and 2.
5) Repeat for i_3, i_4
6) Verify that the current unbalance in each case does not exceed Icont-2P_unb limit in table 33-11 item 4a.

Verification of Icont-2P_unb in step 6 confirms PSE conformance to Equation 334-b.

33B.4 Channel resistance with less than 0.1Ω

Icont_2P_unb_max was specified for total channel common mode pair resistance from 0.1Ω to 12.5Ω and worst case unbalance contribution by a PD.
When PSE is needed to be tested for channel common mode resistance less than 0.1 Ω, i.e. 0 Ω <Rch_x <0.1 Ω , the PSE should be tested with (Rload_min - Rch_x) and , (Rload_max - Rch_x)

Annex F (Informative) - Derivation of Rload_max and Rload_min

Editor Note (to be removed prior to publication): To consider the value of adding informative Annex F to present Rload_max and Rload_min equation derivation and values.

---------------------- END OF REMEDY PART --

This part is not part of the Comment and Suggested Remedy. It is given here for explaining the derivation of the procedure in 33B.2.

Equation Derivation

$V_{diff} = V_2 - V_1 = V_{R1} - V_{R2} = I_1{*}R_1 - I_2{*}R_2$ *(Note: $V_2 > V_1$ because $I_1 >> I_2$)*

$V_{diff}' = V_2' - V_1' = V_{R1}' - V_{R2}' = I_1'{*}R_1 - I_2{*}R_2$

$V_{diff} - V_{diff}' = (V_2 - V_1) - (V_2' - V_1') = (I_1{*}R_1 - I_2{*}R_2) - (I_1'{*}R_1 - I_2{*}R_2) = I_1{*}R_1 - I_1'{*}R_1$

$(I_2{*}R_2)$ in the above equation cancels because I_2 is held to a constant value;

$(V_2 - V_1) - (V_2' - V_1') = I_1{*}R_1 - I_1'{*}R_1$

$(V_2 - V_1) - (V_2' - V_1') = (I_1 - I_1')\, R_1$

And;

$$\frac{(V_2 - V_1) - (V_2' - V_1')}{(I_1 - I_1')} = R_1$$

Example: $R_{eff1} = 0.5$ Ohms, $R_{eff2} = 0.45$ Ohms, $I_1 = 300mA$, $I_1' = 240mA$, $I_2 = 10mA$

$V_{diff} = 300mA{*}0.5 - 10mA{*}0.45 = 145.5mV$

$V_{diff}' = 240mA{*}0.5 - 10mA{*}0.45 = 115.5mV$

$(V_{diff} - V_{diff}')/(I_1 - I_1') = (.1455-.1155)/(0.3-0.24) = 0.030/0.060 = 0.5 = R_{eff1}$

Assumption: 20% difference between I_1 and I_1' yields negligible change in Reff1 at high currents: the difference could be reduced to 10% or even less.