Analysis of:

Table 33-18 item 9, Cpd_min value for Type 3 and 4 PDs

(D1.1 comment cycle)

Yair Darshan, July 2015

Supporters:
Lennart Yseboodt / Philips
Matthias Wendt / Philips
Fred Schindler / Seen Simply.
Pavlik Rimboim / MSCC

Comment

In Draft D1.1 we require 5uF minimum for Type 2 PD (25.5W) and the same value for Type 3 PD (51W) and for Type 4 PD with (71W to 90W).
This is impossible if we want to meet the same transient requirements.
Increasing the load must end with increasing input capacitance accordingly.
It is not clear from the text if the capacitance seen from the PSE PI is 5uF total over all 4P or it is 10uF over all 4P.
Using the PI in the text added to 33.3.7.6 in draft D1.0 also not clarify it for SS PDs.
It is clear that for SS PD, the total Cport_min that is seen by PSE when operated with 4P need to be as follows:

Type/Class	Cport_min	Iload	Vmax	Vmin	Ppd_max	t	Notes
-	uF	A	V	V	W	us	
Type 1, 2. Type 3 class 0-4.	5	0.6	57	50	25.5	73.43	Our reference case
Type 3 class 5, 6	10	1.2	57	50	51	73.43	For SS PD as seen by PSE over all 4P. When we measure with 2P, we will see 10uF for Type 3 and 19.13uF for Type 4 as well.
Type 4 class 7, 8	19.13	1.73	57	52	71	73.43	

For Type 2 which is our reference point, Maximum transient time, t addressed by Cport_min=5uF is:
t=0.5*Cport_min*(Vmax^2-Vmin^2)/Pclass_PD =
To keep the same behavior for higher power and different PSE voltage, we need higher total Cport_min seen by the PSE when all 4P are conducting and delivering power.

Suggested Remedy – See next slide

Suggested Remedy

1. To update Table 33-18 item 9 as follows:

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
9	Pair set capacitance during MDI_POWER states	CPort	uF	5		1, 2	See 33.3.7.6, 33.3.7.3.
9a				10		3	
9b				20		4	

Modify 33.3.7.6 lines 27 – 36 as follows:

33.3.7.6 PD behavior during transients at the PSE PI

Change text in section 33.3.7.6 as follows:

Type 1, Type 2~~,~~ ~~and~~ single-signature PD and Type 3 single signature PDs with classes 0 to 4 ~~and Type 4 PDs~~ shall meet the requirement for Cport as defined in Table 33–18 item 9.

Type 3 single-signature PDs with class 5 to 6 shall meet the requirement for Cport as defined in Table 33–18 item 9a.

Type 4 single-signature PDs with class 7 and 8 shall meet the requirement for Cport as defined in Table 33–18 item 9b.

Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9 for each pair set.

Type 3 dual-signature PDs with class 5 shall meet the requirement for Cport as defined in Table 33–18 item 9a for each pair set.

~~and Type 4 dual-signature PDs shall meet the requirement for Cport as defined in Table 33–18 for each pair set.~~

Modify 33.3.7.3 lines 39 – 47 as follows:

Input inrush current at startup is limited by the PSE if CPort per pair set < 180 µF, as specified in Table 33– 11. If CPort per pair set ≥180 µF, input inrush current shall be limited by the PD so that IInrush_PD per pair set max is satisfied.

[Editor Note (to be removed prior publication): To consider using global parameter and use Cport_max in Table 33-18 per PD Type instead of numbers e.g. 180uF in the text. In addition, Cport_max need to be defined for Type 3 and 4 since currently it is not clear what it is]

Insert a note at the end of section 33.3.7.3 as follows:

NOTE— Cport per pair set is the Cport seen by an attached PSE on two twisted pairs

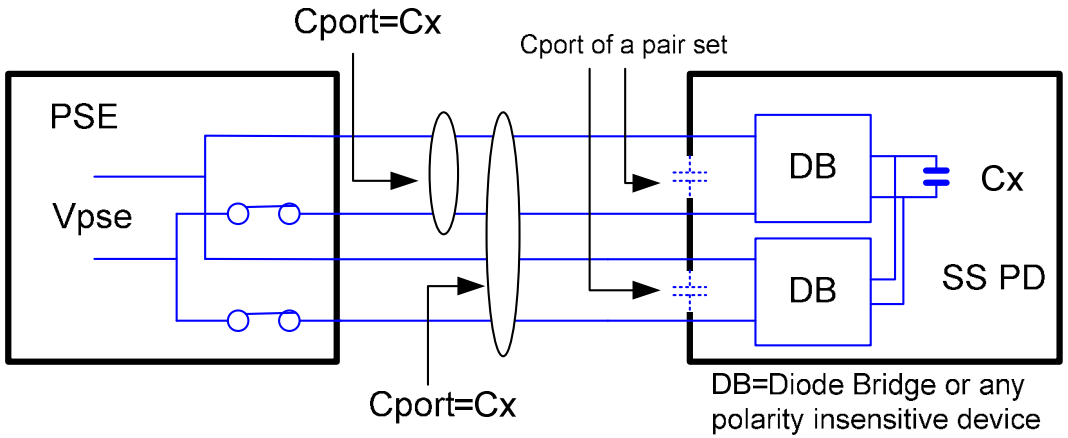
Note: Cport in Table 33-18 is the total PD input capacitance during POWERUP and POWER ON states that any PSE sees when connected to any single signature PD over a pair set or both pair sets.

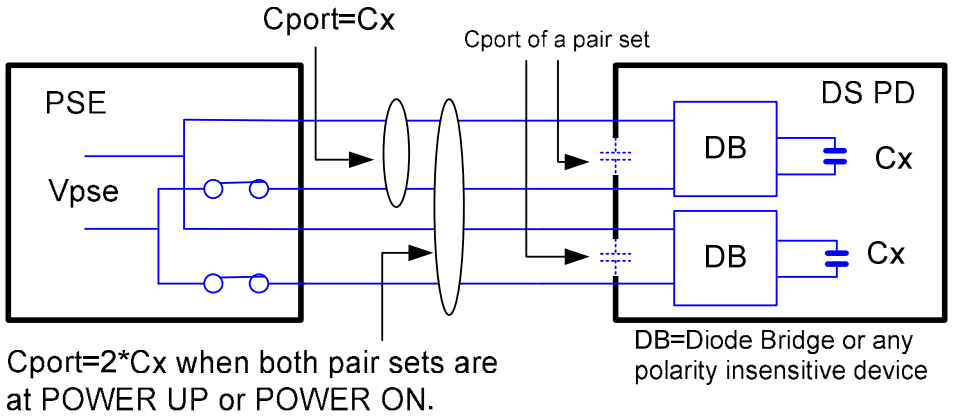
When PSE is connected to Dual Signature PDs, Cport value requirements are specified in 33.2.7.6.

See PSE-PD simplified Cport interpretation model in Annex TBD-A.

Annex TBD-A – Simplified model for Cport interpretation in SS PD per pair set during POWER UP and POWER ON states

SS PD = Single Signature PD





Note: Cpd_d per Table 33-19 and input capacitance during detection per Table 33-14 are not shown in the model due to the fact that they are significantly smaller than <<Cport_min requirement per Table 33-18