Is 180uF Enough?

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Topics

- 180uF: History
- 180uF: Technical details with 100W supply
- 180uF: Market trends
- Conclusions

History Behind 180uF

- Chosen during AF to ensure no inadvertent Tcut errors due to PSE backplane voltage steps:
  - 400mA min Ilim current
  - 350ma max PD current continuous (from AF spec)
  - 50ms Tcut min
  - 44V to 57V input step
- C = I*dt/dv = (400-350)mA*50ms/13V = 192uF
  - Rounded down to 180uF

180uF – More History

- Larger cap values may be used in the PD, but they must be after an internal current limiter so they don't appear at the PD input during inrush or PSE voltage transients (33.3.7.3)
- 180uF in turn sets the SOA required for inrush in most AF PSE designs
- AF inrush specs were preserved in AT to keep SOA requirements the same

Input Cap Functions

- The input capacitor does more than one thing:
  - Attenuates ripple at the PD input
  - Absorbs inrush current at turnon
  - Filters voltage input during backplane steps
    - Positive steps look like inrush to the PSE
    - Negative steps look like disconnect as input diodes reverse-bias
      - In this case, small Cpd is desirable (less time with diode bridge reverse-biased)

Ripple Attenuation

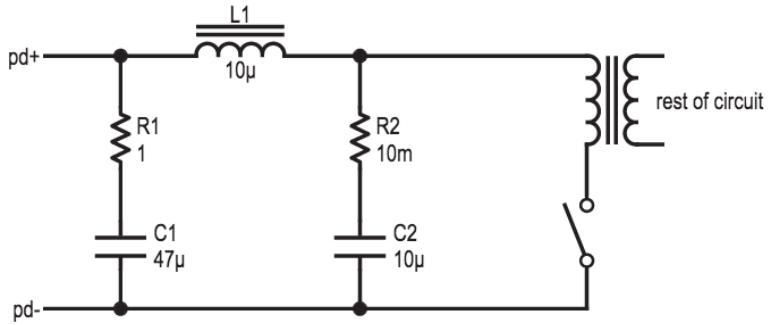
- 802.3-2012 defines ripple specs at the input of the PD:

Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
10	Ripple and noise, < 500 Hz		V_{PP}		0.500	1, 2	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
	a) PD Power supply turn on						

PD Supply Model: Ripple Voltage

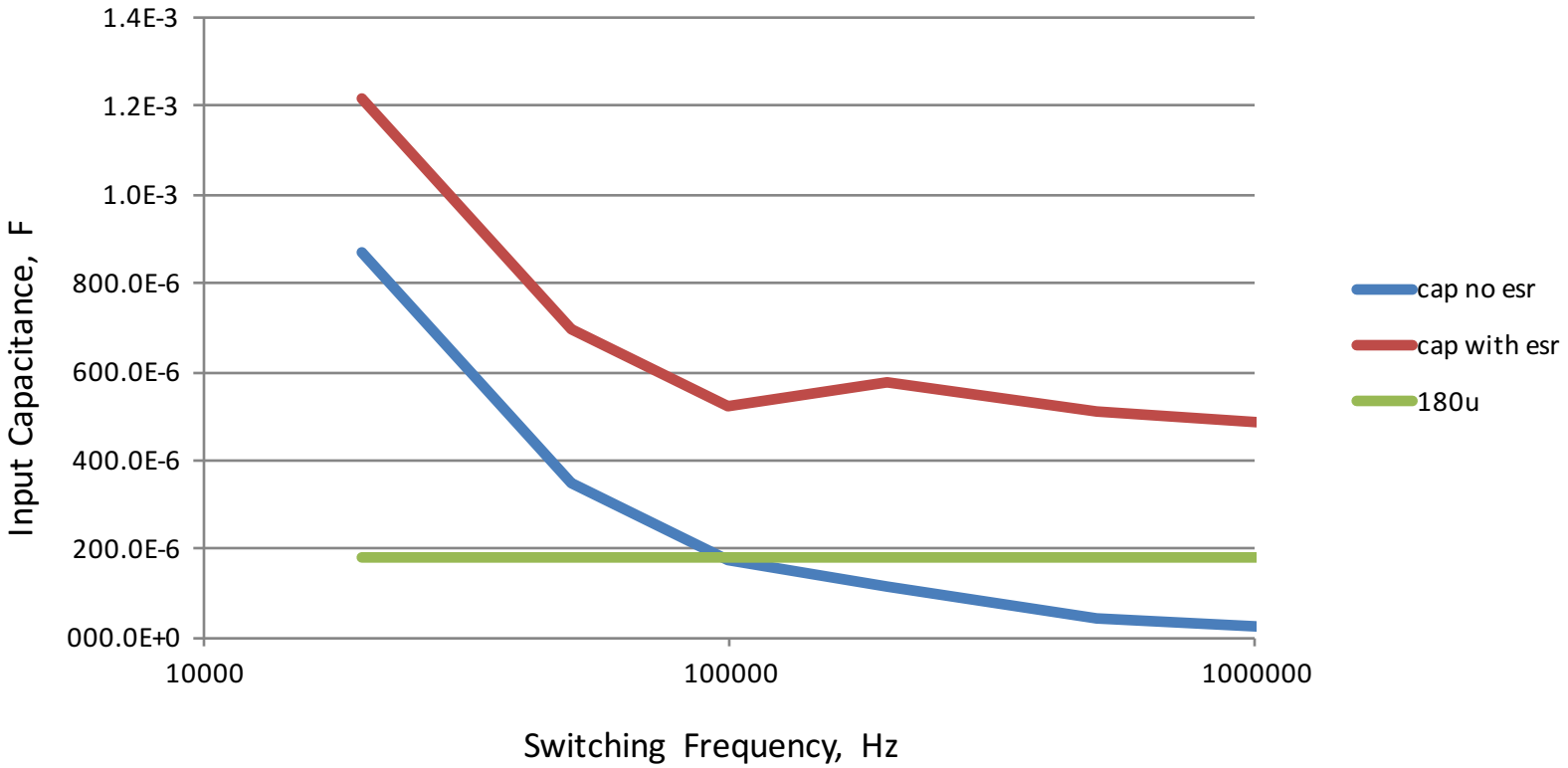
- PD supplies are typically flyback or forward converters with discontinuous input currents
  - Switch in series with the input causes square-wave current flow
- Ripple voltage comes from two effects:
  - Peak current flowing in and out of C2
  - Peak current flowing in capacitor ESR (R2)
- Both effects are attenuated by input pi filter if included (L1, R1, C1)



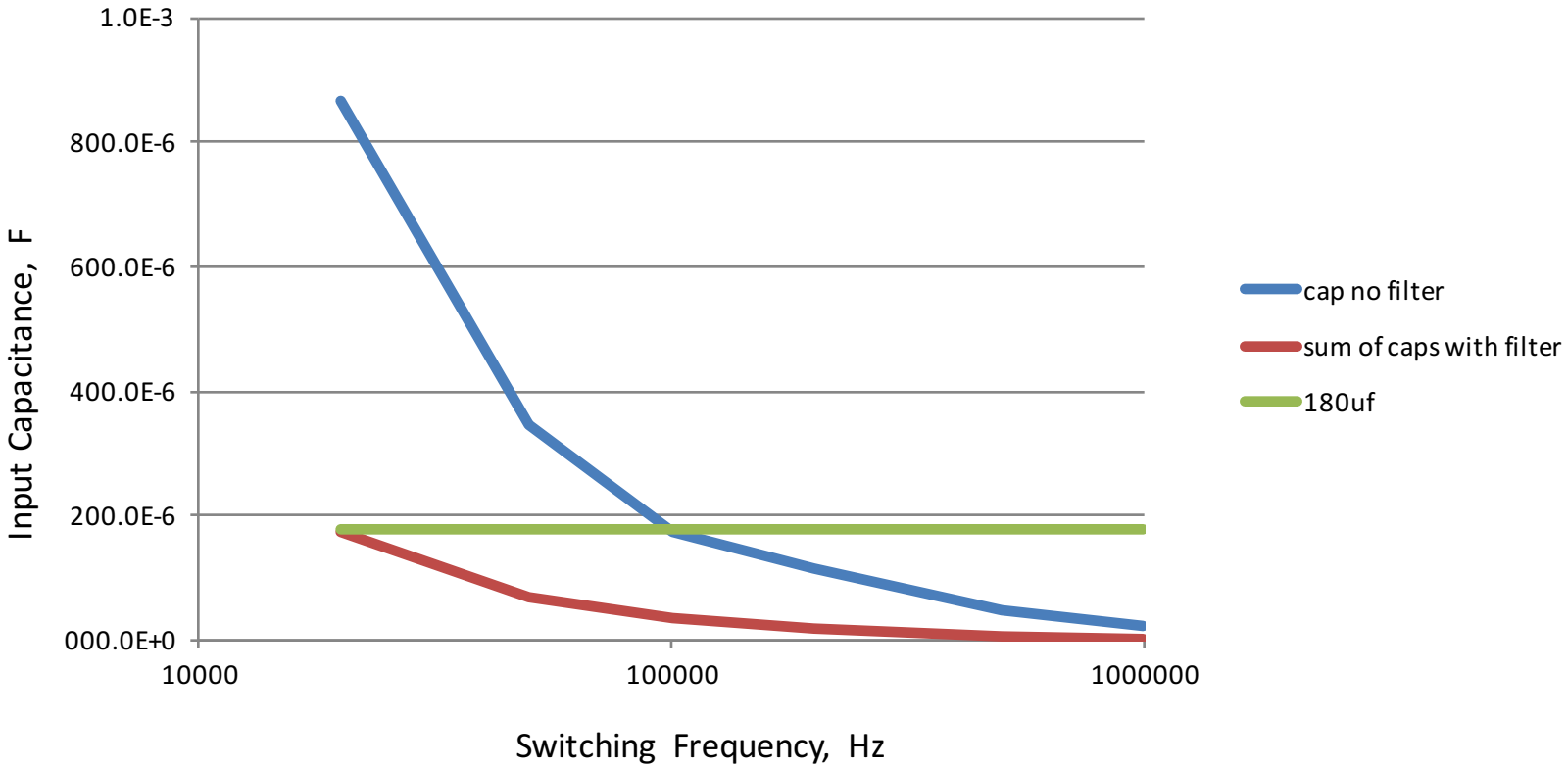
PD Ripple Calculation Assumptions

- Vpd = 36V (Table 33-18 item 3 min)
- 50% ripple current (aggressive)
- 200mV max ripple spec (Table 33-18 item 10)
  - 150mV max above 150kHz
- Preliminary calculations in Excel file (see me) – final analysis to be presented next time

Cap Required to Meet Spec: No Pi Filter



Cap Required to Meet Spec: With Pi Filter



Inrush and Backplane Steps

- Inrush at Turn-on: spec is not perfect
  - Current spec requires 400mA/pair minimum, allows 50ms for Tinrush
  - PD must act as Type 1 for Tdelay = 80mS (13W max) = 350mA current
    - 433mA at 30V (min Von) – this can get stuck!
  - PD load at 350mA: PSE can only inrush **48uF** in 50ms!
  - Most PDs limit power during Tdelay to <<13W – **but this is a hole in the spec**
  - If PD draws zero load during Tdelay: PSE can inrush 380uF
  - **A compliant PSE may fail to turn on a compliant PD**
- Backplane step bad for Type 2, OK for other Types
  - Type 1 OK – 180uF was calculated from Type 1 specs
  - Types 3/4 OK due to higher Ipse: can handle >600uF
  - **Type 2 is broken: can only handle 120uF PD in this case (due to short Tlim)!**

Cpd Market Trends

- Most PD data sheet circuits and demo boards use caps <<180uF behind PD inrush limiter
- Typical bulk values are 15uF, 22uF, or 47uF for 25W supplies
- Caps scale with power, so 4x = 60uF to 188uF
- Virtually all demo systems use Pi filters and place caps after an inrush-limiting PD chip
- 180uF max at 100W doesn't seem limiting in most applications
- 90uF max per pair for DS applications (50W/pair) is similarly not limiting

Conclusion: 180uF is Enough

- 180uF total for Cpse (without PD current limiting) seems reasonable for all PD configurations – SS and DS
- No technical or economic need for 180uF/pair for DS PDs
- Keeping 180uF total limits SOA requirements for all PSE designs
  - Compatible with existing PSE silicon
  - Room for optimization for future PSE silicon
- We should fix existing spec problems with AT spec