Connection Check: Timing Requirements Baseline Text

David Abramson

Texas Instruments

IEEE802.3bt Task Force

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Presentation Information

- This presentation is a repeat of what was presented in Pittsburgh (5/15) with the exception of the new baseline text slides at the end.

History of the “Connection Check”

- The connection check was originally introduced as a method for PSEs to determine if they were connected to a single signature PD or a dual signature PD.
- Multiple methods for implementing the connection check have been presented. See:
  - http://www.ieee802.org/3/bt/public/nov14/Lukacs_01_1114.pdf
  - http://www.ieee802.org/3/bt/public/nov14/darshan_10_0914.pdf
  - http://www.ieee802.org/3/bt/public/sep14/dwelley_01_0914.pdf
- Baseline text for the electrical specifications of the connection check were adopted in March 2015. See:
  - http://www.ieee802.org/3/bt/public/mar15/abramson_01_0315.pdf
- The purpose of this presentation is to present baseline text for the timing requirements of the connection check.
- **This presentation specifically does not address 4-Pair ID and whether connection check is sufficient to apply 4-pair power.**

Adopted Connection Check Baseline Text

33.2.5.X Connection Check Requirements

Type 3 and Type 4 PSEs that operate over both pair sets shall complete a connection check prior to the classification of a PD as specified in clause 33.2.6. The purpose of the connection check is to determine the architecture of the PD connected to the PSE PI, specifically the PSE shall determine if it is connected to a single PD interface or a dual PD interface. See Annex 33TBD for more information about the connection check.

Editor's Note: Definitions of single PD interface and dual PD interface need to be added or text needs to be cleaned up when final terminology is decided.

While the exact method of the connection check is left to the implementer, the PSE shall meet the specifications for open circuit voltage and short circuit current in Table 33-4. In addition, only tests that result in a voltage at the PSE PI that is within the V_{valid} voltage range as specified in Table 33-4 shall be used to determine the architecture of the PD.

Timing requirements TBD.

Connection Check: Timing Requirements

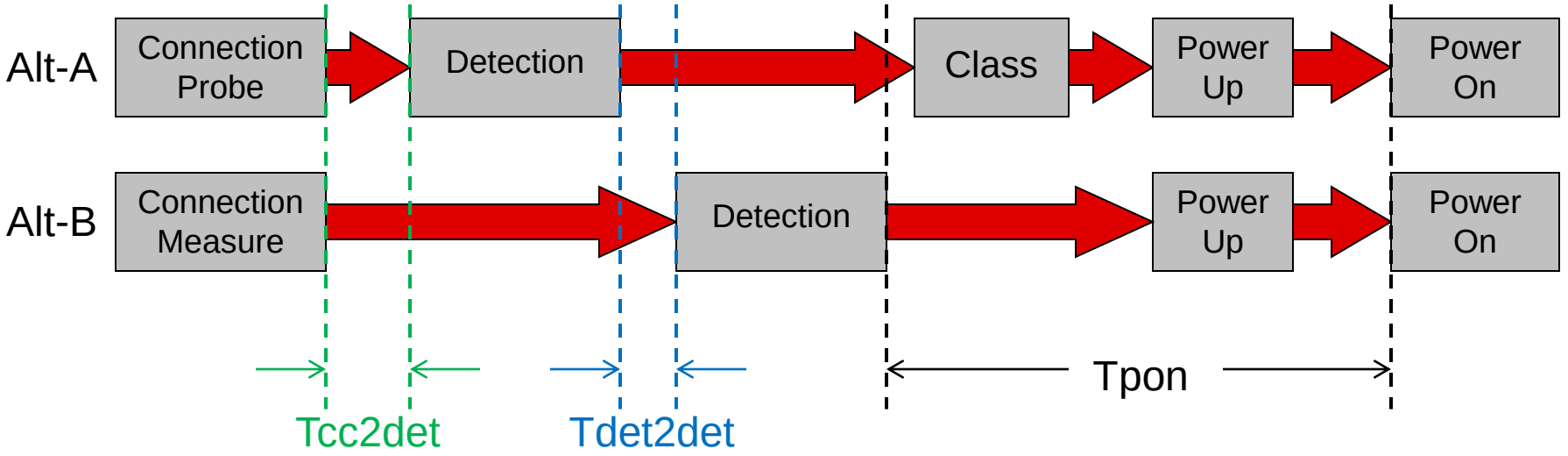
- The goal of the timing requirements for the connection check (and rest of the powering procedure) are to not allow gaps of greater than 400ms where a cable could be unplugged and another cable plugged in without the PSE recognizing it.
  - The Tpon requirement makes sure that a PD is powered within this 400ms limit from the end of detection.
  - There is now information gained during the connection check (as well as independent detections on each pair set) that must be “maintained” until the PD is powered.
    - “Maintained” means that we must ensure the load is not switched without the PSE restarting the connection check/detection/power up procedure.

More Timing/Transition Requirements

- If the connection check is performed after detection, it must be fast enough to squeeze into Tpon along with class and power up (inrush).
- If the connection check is performed as part of detection, it will be included in the Tdet timing requirements.
- If the connection check is preformed before detection, we will need to add a new timing requirement to ensure gaps of more than 400ms are not created.
- If the connection check is performed before (or during) detection, it must not result in the PD presenting an invalid signature.
  - If the connection check causes the PD voltage to raise into the class range and return to a lower voltage (in the Vvalid range), Type 2, Type 3, and Type 4 PDs will transition to mark and present invalid signatures.
  - If the voltage is brought below the reset threshold between the connection check and detection, this PD would reset and transition back into detection and present a valid signature.

Connection Check Timing: An Example

4PPoE PSE Connected to 4PPoE PD with Dual PD Interface



- Tpon: Ensures cable is not switched between end of detection and power on.
- Tcc2det: Ensures cable is not switched between end of connection check and beginning of detection.
  - Possible wording to allow flexibility: "The end of the connection check shall be no more than 400ms before the beginning of detection on at least one pair set."
- Tdet2det: Ensures cable is not switched between end of first detection and beginning of 2nd detection.
  - Possible wording to allow flexibility: "There shall be no more than 400ms from the end of the detection on the first pair-set to the beginning of detection on the other pair-set."

Dual Signature PDs

- Detection can be done simultaneously, or staggered.
  - Tpon must be met on each pair set.
  - This means that Tdet2det does not apply to dual signature PDs.
- If detection is staggered, the connection check result holds once one pair set is powered according to the Tcc2det and Tpon requirements.
  - The connection check result is reset (a new check is needed) if both pair sets are unpowered at the same time.

Single Signature vs. Dual Signature PDs

Parameter	Single Signature PD	Dual Signature PD
Tcc2det	Applies from connection check to first detection.	Applies from connection check to first detection.
Tdet2det	Applies from end of first detection to beginning of second detection.	Does not apply.
Tpon	Applies from end of second detection to power on state (power up sequence must be simultaneous).	Applies to each pair set individually from end of detection to power on state (power up sequence may be simultaneous or staggered).
Connection Check Reset Behavior	Connection check must be rerun if power up fails to meet timing requirements or anytime power is removed from the PI (from the power up or power on states).	Connection check must be rerun if power up fails to meet timing requirements or anytime both pair sets are unpowered at the same time.

Summary

- Two new timing parameters have been introduced for the startup sequence:
  - Tcc2det ensures the cable is not switched between end of connection check and beginning of detection for both single and dual signature PDs.
  - Tdet2det Ensures cable is not switched between end of first detection and beginning of 2nd detection for single signature PDs.
- How Tpon applies to single and dual signature PDs will need to be clarified. I propose:
  - Tpon applies from end of second detection to power on state (power up sequence must be simultaneous).
  - Tpon applies to each pair set individually from end of detection to power on state (power up sequence may be simultaneous or staggered).
- PD Reset behavior should be addressed.
  - The PSE must reset the PD (bring the voltage below the reset threshold) if the voltage has entered the class range during the connection check.
- Based on your feedback I will present baseline text for this at the next meeting.

Baseline Text

- Text to be added in place of “Timing Requirements TBD.” in section 33.2.5.0a:
  - The connection check shall be completed before classification.
  - The specification for Tcc2det, defined in Table 33-CC,1applies to the time between the end of the connection check and the beginning of detection on at least one pair set. If the connection check takes place after the beginning of detection, this specification does not apply.
  - The specification for Tdet2det, defined in Table 33-CC1, applies to the time between the end of the detection on the first pair set to the beginning of detection the other pair set when connected to a single-signature PD.

Table 33-CC1 Connection Check Timing Requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional Information
1	Connection check to detection time	Tcc2det	s		0.4	Applies only when connection check is performed before the start of detection
2	Detection to detection time	Tdet2det	s		0.4	Applies only when connected to a single-signature PD

  - Editor’s Note to be removed before publication: Table number needs to be updated once draft order is finalized.

Baseline Text

- Text to go in new paragraph at the end of section 33.2.5.0a:
  - The connection check shall be rerun if power up fails to meet the timing requirements or anytime power is removed from both pair sets at the same time after reaching the POWER_UP state.

  - If the voltage at the PI, on either pair set, rises above Vvalid max, defined in table 33-4, the PSE shall reset the PD by bringing the voltage at the PI below Voff max, defined in Table 33-7.

Baseline Text

- Text to replace the current 33.2.7.12 section:
  - The specification for Tpon in Table 33—11 applies to the PSE power up time for a PD after completion of detection.
  - For Type 3 and Type 4 PSEs, when connected to a single-signature PD, both pair sets must reach the POWER_ON state within Tpon after detection on the last pair set. When connected to a dual-signature PD, Tpon is applied from the completion of detection to the POWER_ON state for each pair set independently.
- Text to replace the second paragraph of 33.2.4.1
  - If power is to be applied, the PSE turns on power after a valid detection in less than Tpon as specified in Table 33–11. If the PSE cannot supply power within Tpon, it initiates and successfully completes a new detection cycle before applying power. See 33.2.7.12 for complete details.