Updated Table 3-18: Item 9 Cport-2P minimum value

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
9	Pair set capacitance during MDI_POWER states	CPort_2P	uF	5		1, 2, 3	See 33.3.7.6, 33.3.7.3. For Type 3 dual signatures PD. For Type 3 single signature PD during 4P operation, the total minimum PD input capacitance is 10uF when Mode A and Mode B pairs are tied together.
				9		4	See 33.3.7.6, 33.3.7.3. For Type 4 dual signatures PD. For Type 4 single signature PD during 4P operation, the total minimum PD input capacitance is 10uF when Mode A and Mode B pairs are tied together.

Derivation of CPort_2P minimum value for Type 3.

From energy storage consideration in order to meet transient requirements of type 2 power with Type 3 PDs, Type 3 single signature PD will have to use twice the minimum capacitance value due to the fact that it supports twice the power of Type 2 PD. Dual signature PD is considered as two independent power inputs hence 5uF is required per Mode A pair and Mode B pair.

Derivation of CPort_2P minimum value for Type 4.

From energy storage consideration in order to meet transient requirements of type 2 power with Type 4 PDs, Type 4 single signature PD will have to use higher capacitance value due to the fact that power can reach 90W instead of 51W. Ignoring the fact that type 4 use 52V minimum instead of 50V in Type 3, we can increase minimum capacitance for Type 4, proportionally to the power increase of Type 4 compared to Type 3 total power.

CPort_2P=5uF*(90/51) =8.82uF rounding up to 9uF.

Annex A_PD_Iinrush for clause 33.3.7.3 page 90 lines 28-31.

The comment addresses the following text in lines 28-40 but focused on lines 28-31):

33.3.7.3 Input inrush current

Inrush current per pair-set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33-18, and ending before TInrush-2P min per Table 33-11. After TInrush-2P min, the PD shall not exceed its per pair set current threshold corresponding to its class level.

From the current text, it is not clear that Iinrush is the response of applying voltage to a capacitor. After PD input capacitance is charged, the capacitor current is decaying to zero

It is also not clear that it is possible that during POWER UP, the input current to the PD contain a resistive load component that is limited for all PD types to 350mA during POWER UP time frame For Type2, 3 and 4 PDs it is limited to 350mA for at least 80msec from STARTUP begin.

As a result the PD input current is split to the PD resistive load and PD input capacitor, generating a charging current of: Icharging=Iinrush-2P_min -Type 1 maximum DC current=0.4A-0.35A=50mA which guarantees that maximum PD input capacitor=180uF is fully charged within 50.4msec for Type 1 systems and Type 1 maximum allowed DC load. Tinrush=Cpd_max*(Vpse_min-Voff)/ (Iunrush_min-Iport_cont) =180uF*(44V-30V)/ (0.4A-0.35A) =50.4msec. This is the reason why Tinrush max for the PD is 50msec.

In similar way for Type 2: Tinrush =180uF*(50V-30V)/ (0.4A-15.4W/50V)= 180uF*20V/ (0.4A-0.308A) =39.13msec <50msec which is OK.

As a result, Iinrush is observed almost immediately when PSE applies Voltage to PD (within few msec) and PD resistive load may follow it at any time during POWER UP time frame with maximum value of 350mA.
There are 2-3 main PD POWER UP profiles (1. short load, ramp, stable. 2. Flat, ramp, stable. 3. Vport, short load, ramp, stable). In all of them completion of Iinrush is possible to detect without waiting for the completion of Tinrush timer.