Proposed baseline for D3.0:

79.3.2.5 PD requested power value

Not part of the baseline
The content of PD requested power value (named Y field in the adhoc material) is function of 3 use cases: 1. Use Y when PSE is connected to single-signature PD or Type 1 and Type 2 PDs. 2. Use Y=0 when connected to dual-signature PD over 4-pirs and both modes are active. 3. Use Y= the value of the active mode X when connected to dual-signature PD over 2-pairs to interoperate with PSEs operating over 2-pairs.

The PD requested power value field shall contain the PD's requested power value defined in Table 79–5, for Type 1, Type 2, and single-signature Type 3 and Type 4 PDs. The fields for PD requested power value shall be set to 0 for Type 3 and Type 4 dual-signature PD operated over mode A and mode B. ~~to the sum of PD requested power value Mode A and PD requested power value Mode B in Table 79–6a, for Type 3 and Type 4 dual-signature PDs.~~

For Type 3 and Type 4 dual-signature PD operated over 2-pairs, the fields for PD requested power value shall be set to the value of PD requested power value Mode (X) where X is the active mode (A or B).

Table 79–5—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through ~~255~~999.

PD requested power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PD is requesting. "PD requested power value" is the power value at the PD PI.

79.3.2.6 PSE allocated power value

The PSE allocated power value field shall contain the PSE allocated power value defined in Table 79-6 for PSEs connected to single-signature PDs and Type 1 and Type 2 PDs.

The field for PSE allocated power value shall be set to 0 for Type 3 and Type 4 dual-signature PD operated over mode A and mode B.

The fields for PSE allocated power value shall be set to the value of the active Alternative A or active Alternative B when the PSE is connected to dual-signature PD over 2-pairs.

~~The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field, as defined in Table 79–6a, shall be provided in the PSE allocated power value field for Type 3 and Type 4 PSEs connected to a dual-signature PD. The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field may be provided in the PSE allocated power value field for Type 1 and Type 2 PSEs when connected to a dual-signature PD.~~

Table 79–6—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through ~~255~~999.

"PSE allocated power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the PD PI. The PSE uses this value to compute PClass defined in 33.2.7 and 145.2.7.

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

Not part of the baseline
We need to delete the red text to allow PSE to know what is the requested power on both modes when PD switches back from 2-pairs to 4-pars.

The "Dual-signature PD requested power value Mode A and Mode B" fields shall contain the PD requested power value defined in Table 79–6a for mode A and for mode B of a dual-signature PD.

~~If mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0.~~

Single-signature PDs shall set the PD requested power value Mode A and Mode B fields to 0.

Table 79–6a—Dual-signature PD requested power value field for Mode A and Mode B

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	Dual-signature PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

"Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

79.3.2.6b PSE allocated power value Alternative A and Alternative B

The PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field shall contain the values in Table 79–6b for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.

Table 79–6b—PSE allocated power value Alternative A and Alternative B field

Bit	Function	Value/meaning
15:0	PSE allocated power value Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	PSE allocated power value Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

"PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives. "PSE allocated power value Alternative A" and "PSE allocated power value Alter-native B" are the power levels at the dual-signature PD PI. The PSE uses this value to compute $P_{Class\text{-}2P}$ defined in 145.2.7. A PSE providing power to a dual-signature PD over 2-pairs, shall set 0 in the PSE allocated power value alternative A field and PSE allocated power value alternative B field.

A PSE providing power to a Type 1, Type 2, or single-signature Type 3 or Type 4 PD, places 0 in the "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields defined in Table 79–6b.

79.3.2.6e PSE maximum available power

Not part of the baseline
Power management for single signature and dual signature cares only for the total port power. Parts of the power management then use this power to allocate it per A and B fields. The following changes will allow us to get rid of the requirement of Y=A+B in D3.0 and set Y=0 instead, when Type 3 /4 PSE operating over 4-pairs is connected to dual signature.

The PSE maximum available power field shall contain the highest power the PSE can grant as defined in Table 79–6e to the port when supporting single-signature PD or dual-signature PD PD. The PSE shall set the value of this field taking available power budget and hardware capabilities into account.

Not part of the baseline
The following change is required to allow dual-signature PD when operating over 2-pairs to get power on the inactive pair later when the inactive pair became active. This is part of the solution to resolve comment #297.

pd_dll_ready_mode(X)

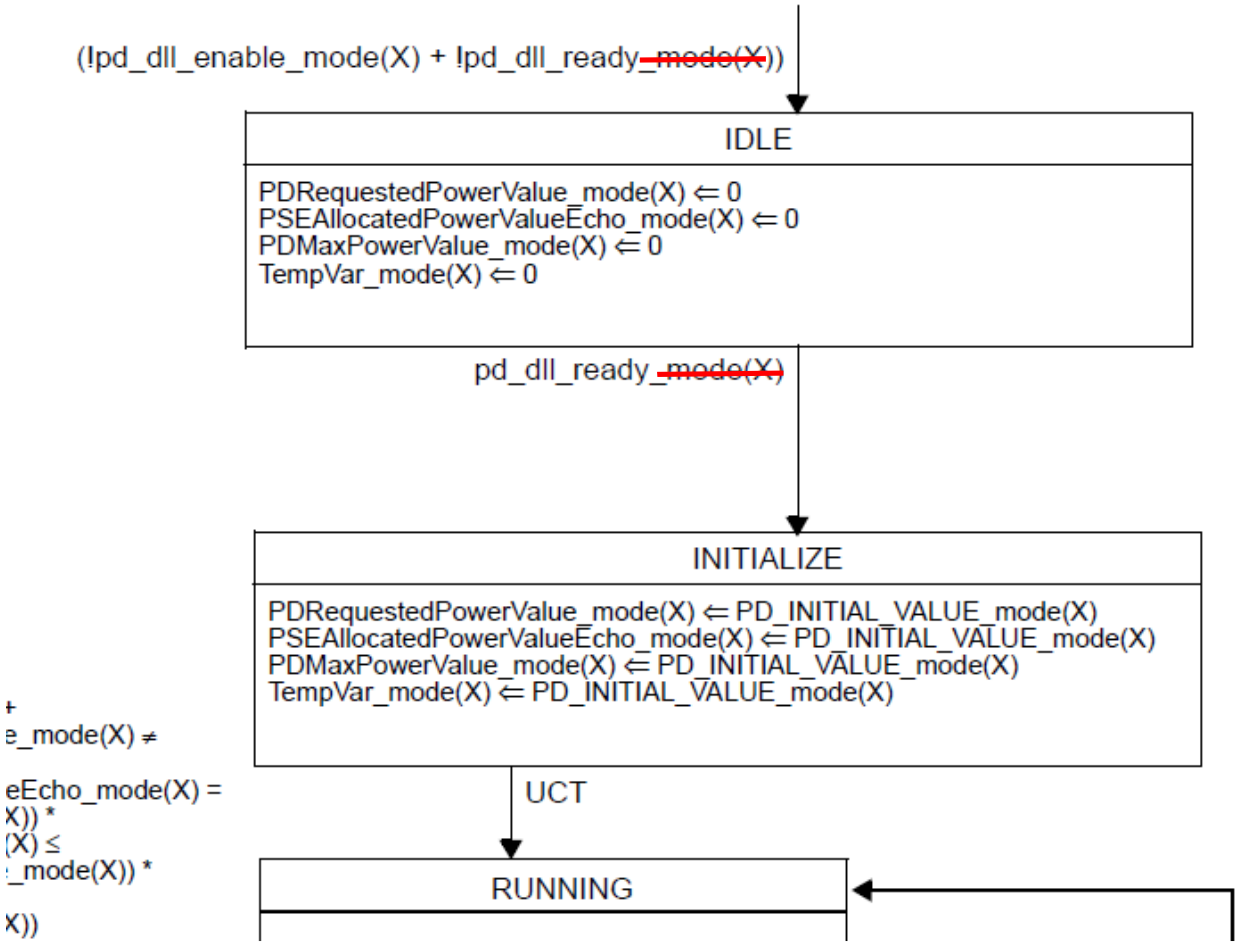
An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. ~~for Mode(X).~~ This variable maps into the aLldpXdot3LocReady ~~aLldpXdot3LocReadyA and aLldpXdot3LocReadyB~~ attribute (30.12.2.1.20 ~~30.12.2.1.18a and 30.12.2.1.18b~~).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

Change "!pd_dll_ready_mode(X)" to !pd_dll_ready in Figure 145-34



145.5.3.4 Single-signature PD power control state diagrams

Add the following text:

This subclause contains the variables and state diagrams the single-signature PD uses when connected to Type 3 or Type 4 PSE or when connected to a PSE that is providing power over 2 pairs.

145.5.3.6 PSE power control state diagrams (dual-signature)

Add the following text:

This subclause contains the variables and state diagrams the PSE uses when connected to a dual-signature PD, when it is providing power over 4 pairs.

145.5.3.7 Dual-signature PD power control state diagrams

Add the following text:

This subclause contains the variables and state diagrams the Dual Signature PD uses when connected to a PSE that is providing power over 4 pairs.

When a dual-signature PD transition from 4-pair operation to 2-pairs operation, the PD requested power value field shall contain the last value of the active PD requested power value mode X filed.

Lennart: To review and update the DLL state machine for dual-signature that comply with the concept we just have agreed.

John: To add text to explain how the PSE and PD get into **sync** when they transition from 2P to 4P and back.

Group: We OK with the concept table. Lennart to review and approve by Sunday.