Proposed baseline for D3.1:

Info (not part of baseline

Purpose
This is an overhaul for the LLDP specification in Clause 79, specifically addressing dual-signature operation. It aims to address the issues raised in comments D2.4 #130, #293, #294, #296, and #297.

All of the requirements we currently have in Clause 79 regarding which fields to set to which value depending on the PD Type and such really don't belong there. Clause 79 defines the format of the PoE TLV. How that TLV is to be used must be defined in Clause 33 and Clause 145. Therefore, this baseline scraps all of the requirements that were added to subclauses 79.3.2.5, 79.3.2.6, and it's dual-signature brethren.

Changelog
v100 First full proposal
v110 Moved DLL requirements to Clause 145 from Clause 79
v111 Comments Heath Stewart (editorial)
v120 4PID bit + restrict new fields to Type 3/4 devices only
v130 Back to using a single pd dll enable / pse dll enable variable for the dual-mode DLL diagrams + big renaming (single-mode and dual-mode DLL)
v131 Review Yair: ...
v132 Yair updates per adhoc meeting #8 proposals/decisions
-PSE single-signature state machine need to work with PD single-signature state machine. Same for dual-signature. After connection check PD doesn't change its hardware. It is still dual-signature PD. As a result, if it is 4P or 2P it stays in dual-signature state machine. This covers line 4 in the Concept table. As a result, in when dual-signature PD is connected to Type 3, 4 PSE, always to work on fields A and B over 4-pairs or A or B over 2-pairs whichever is active. The non-active field in the PSE will be set to 0. In the PD, the non-active field will get the required power (option 1 the current solution) or set to zero (option 2, to be discussed by the group).
-When dual-signature is connected to Legacy PSE, it will work with single-signature SM since PSE has no other choice. This covers line 5 in the Concept Table (No change).
-pse_dll_enable_alt(X) and pd_dll_enable_mode(X) where unified (There is only one instance running so we can unify dll_enable).
-pse_dll_ready stays separate for both PSE and PD (that it is not instantaneous mechanism it takes seconds until you get completion).

145.5.3 Power control state diagrams

Info (not part of baseline

Type 3/4 PSEs need to ~~always~~ 'run' both the single-signature and the dual-signature state diagrams. ~~These state diagram control the logic needed to set the values of the respective fields correctly.~~

Once single-signature or dual-signature operation was determined, the state machine stays there and doesn't flip if operating mode was changed from 4P to 2P when operating in dual-signature SM.

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively.

~~Data Link Layer classification of PSEs connected to a single-signature PD, shall provide the behavior in the state diagram defined in Figure 145–39 and Figure 145–40. Data Link Layer classification of PSEs connected to a dual-signature PD, shall provide the behavior in the state diagram defined in Figure 145–43.~~

Data Link Layer classification of PSEs shall provide the behavior in the state diagrams defined in Figure 145–39, Figure 145–40, and Figure 145–43.

Info (not part of baseline

The same applies to PDs, they need to follow the relevant state machine pending the result of the connection check and not flip between state machines even if dual-signature transitions from 4 pair to 2-pair and vice versa.

~~The same applies to PDs, they need to follow all of the state diagrams. For a single-signature, this means that the state diagrams for dual-signature will stay in the IDLE state, thereby setting the A and B fields to zero.~~

Single-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–41 ~~and~~ Figure 145–42, and Figure 145-44. Dual-signature PD Data Link Layer classification shall provide the behavior of the state diagram defined in Figure 145–44.

Insert new subclause 145.5.3a before 145.5.4 as follows:

145.5.3a Power requests and allocations

The variables PDRequestedPowerValue and PDRequestedPowerValue mode(X) allow a PD to request an amount of power from the PSE. The variables PSEAllocatedPowerValue and PSEAllocatedPowerValue alt(X) allow the PSE to allocate an amount of power to the PD.

PSEs shall use values in the range defined in Table 145–41 for PSEAllocatedPowerValue and PSEAllocatedPower-Value alt(X) where X can be A or B. PDs shall use the values in the range defined in Table 145–42 for Requested-Power Value and PDRequestedPowerValue mode(X) where X can be A or B.

Table 145–41—Permitted values for PSEAllocatedPowerValue and PSEAllocatedPowerValue alt(X)

PSE Type	Powering mode	PD configuration	PSEAllocatedPowerValue	PSEAllocatedPowerValue alt(X)
Type 1, 2	-----	1,2,3,4	1-255	0
Type 3, 4	4-pair	single-signature	1-999	0
Type 3, 4	2-pair	single-signature	1-499[a]	0
Type 3, 4	4-pair	Dual-signature	0	1-499
Type 3, 4	2-pair	Dual-signature	0	1-499[a] for the active mode. The non-active mode will be set to 0.

[a] NOTE—A PSE that has encountered a fault that requires to operate in 2-pair mode, may use values 1–499 for this variable.

Table 145–42—Permitted values for PDRequestedPowerValue and PDRequestedPowerValue mode(X)

PD Type	Powering mode	PD configuration	PDRequestedPowerValue	PDRequestedPowerValue mode(X)
Type 1, 2	-----	-----	1-255	0
Type 3, 4	4-pair	single-signature	1-999	0
Type 3, 4	2-pair	single-signature	1-499[a]	0
Type 3, 4	4-pair	Dual-signature	0	1-499
Type 3, 4	2-pair	Dual-signature	0	Option 1: 1-499[a] for the both the active and non-active mode. Option 2: 1-499[a] for the active mode. The non-active mode will be set to 0. GROUP TO DISCUSS

145.5.3.3 PSE power control state diagrams (single-signature)

~~This subclause contains the variables and state diagrams the PSE uses when connected to a single-signature PD, or when it is providing power over 2 pairs.~~

This state diagram controls the PSEAllocatedPowerValue variable, which is used to allocate power to a PD. It is applicable when the PD is a single-signature PD or when the PD is Type 1 or Type 2.~~, or when the PD is supplied in 2-pair mode.~~

145.5.3.4 Single-signature PD power control state diagram

Add the following text to this empty subclause:

This state diagram controls the PDRequestedPowerValue variable, which is used to request power from a PSE. It is applicable when the PD is a single-signature PD or Type 1 or Type 2 PD. ~~, PD, or when the PD is supplied in 2-pair mode.~~

145.5.3.6 PSE power control state diagrams (dual-signature)

Add the following text to this empty subclause:

This state diagram controls the PSEAllocatedPowerValue alt(X) variables, which are used to allocate power to the individual Modes of a dual-signature PD. ~~It is applicable when the PD is a dual-signature PD that is supplied in 4-pair mode.~~

145.5.3.7 Dual-signature PD power control state diagrams

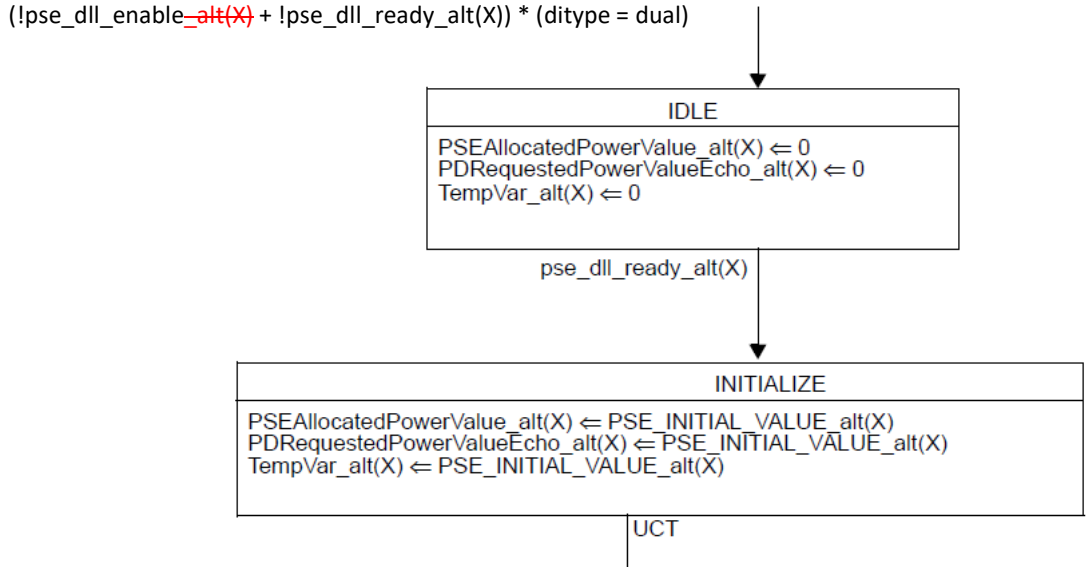
Add the following text to this empty subclause:

This state diagram controls the PDRequestedPowerValue mode(X) variables, which are used to allocate power to the individual Modes of a dual-signature PD. ~~It is applicable when the PD is a dual-signature PD that is supplied in 4-pair mode.~~

145.5.3.6.3 State diagrams

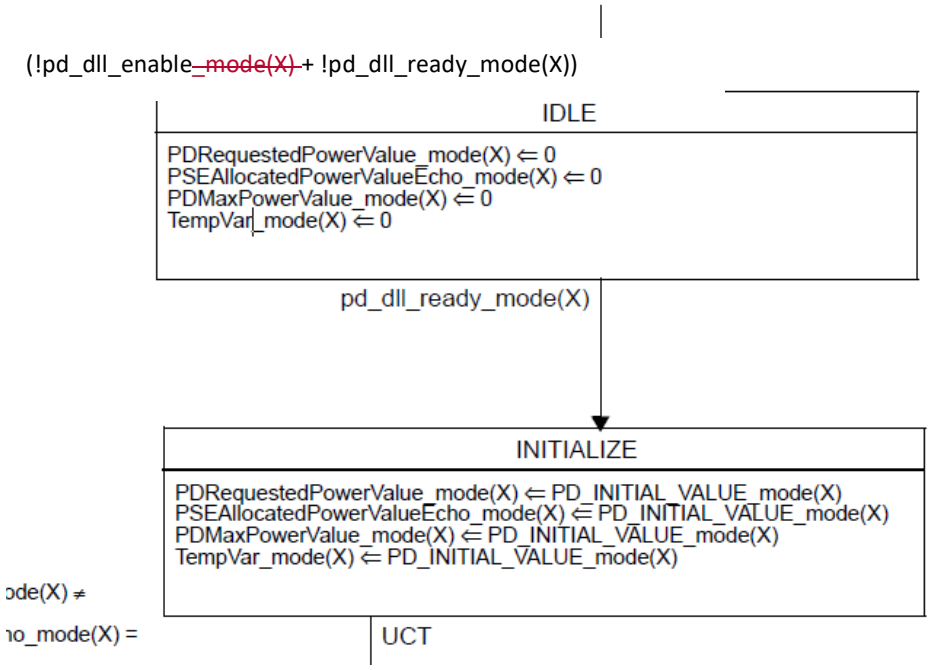
Info (not part of baseline
pse_dll_enable_alt(X) is unified to pse_dll_enable.

The general state change procedure for PSEs is shown in Figure 145–43.



145.5.3.7.4 State diagrams

The general state change procedure for PDs is shown in Figure 145–44.



79.3.2 Power via MDI TLV

The Power via MDI TLV shown in Figure 79–3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV only supported the first three fields of Figure 79–3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-201x to add a further nine fields, labeled Type 3 and Type 4 extension to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

~~Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension.~~

……..

Append the following paragraph as follows:

If a Type 1 or Type 2 power entity implements Data Link Layer classification, it shall support the Power Via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered. If a Type 3 or Type 4 power entity implements Data Link Layer classification, it shall support both the DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in transmitted LLDPDU's.

Info (not part of baseline)
Out of all the fields and bits in the "Type 3 and Type 4 extensions", there is one bit that is specifically intended for Type 1 and Type 2 PDs. The PD 4PID bit allows such a PD to assert that it is 4-pair capable. By having this bit in the "Type 3 and Type 4 extensions" fields, we open up Pandora's box of having the define ALL of the fields for Type 1 and Type 2 devices. The proposed solution is to move this bit into a reserved bit of the existing fields. That way, the "Type 3 and Type 4 extensions" can be restricted to Type 3 and Type 4 devices only.

79.3.2.4.1 Power type

Move the PD 4PID bit from Table 79–6d (System setup field) to bit position 2 in Table 79-4 (Power type/source/priority field) as follows:

Table 79–6d—System setup field

Bit	Function	Value/meaning
7:6	Reserved	Transmit as zero. Ignore on receive.
5:2	Power typex	5 4 3 2 1 1 1 1 = Type 4 dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Type 3 dual-signature PD 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Type 4 single-signature PD 1 0 0 0 = Type 4 PSE 0 1 1 1 = Type 3 single-signature PD 0 1 1 0 = Type 3 PSE 0 1 0 1 = Type 2 PD 0 1 0 0 = Type 2 PSE 0 0 1 1 = Type 1 PD 0 0 1 0 = Type 1 PSE 0 0 0 1 = Reserved/Ignore 0 0 0 0 = Reserved/Ignore
1	PD 4PID	1 = PD supports powering of both Modes simultaneously 0 = PD does not support powering of both Modes simultaneously
0	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.

Move PD 4PID

1

2

Table 79–4—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source Move 4PID to bit 2	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Transmit as zero, ignore on receive
1:0	power priority	1 0 1 1 = low priority PD 1 0 = high priority PD 0 1 = critical priority PD 0 0 = priority unknown (default)

Info (not part of baseline)
Restore sections on PD requested power and PSE allocated power. The new subclause in Clause 145 above will deal with what needs to be filled out in particular circumstances.

79.3.2.5 PD requested power value

The PD requested power value field shall contain the PD's requested power value defined in Table 79–5. ~~, for Type 1, Type 2, and single-signature Type 3 and Type 4 PDs. The fields for PD requested power value shall be set to the sum of PD requested power value Mode A and PD requested power value Mode B in Table 79–6a, for Type 3 and Type 4 dual-signature PDs.~~ PD requested power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PD is requesting. "PD requested power value" is the power value at the PD PI.

Table 79–5—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~1~~ 0 through ~~255~~999.

Info (not part of baseline
We have now changed this legacy field to include 0 as a valid value. For Type 1/2 this was an illegal value, which now becomes a legal value, which leads to undefined behavior if used. This would not be a problem, were it not that Clause 33, by mistake, allows the value 0 in the variable that is linked to this field. We will need to file an MR to change the DLL state diagram in Clause 33, to restrict the value PDRequestedPowerValue from 1 through 255. Both changes together do not result in a change in legacy requirements.

79.3.2.6 PSE allocated power value

The PSE allocated power value field shall contain the PSE allocated power value defined in Table 79-6. ~~for PSEs connected to single-signature PDs and Type 1 and Type 2 PDs.~~

~~The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field, as defined in Table 79–6a, shall be provided in the PSE allocated power value field for Type 3 and Type 4 PSEs connected to a dual-signature PD. The sum of the PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field may be provided in the PSE allocated power value field for Type 1 and Type 2 PSEs when connected to a dual-signature PD.~~ "PSE allocated power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the PD PI. The PSE uses this value to compute PClass defined in 33.2.7 and 145.2.7.

Table 79–6—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~1~~ 0 through ~~255~~999.

0

Info (not part of baseline
We have now changed this legacy field to include 0 as a valid value. For Type 1/2 this was an illegal value, which now becomes a legal value, which leads to undefined behavior if used. This would not be a problem, were it not that Clause 33, by mistake, allows the value 0 in the variable that is linked to this field. We will need to file an MR to change the DLL state diagram in Clause 33, to restrict the value PSEAllocatedPowerValue from 1 through 255. Both changes together do not result in a change in legacy requirements.

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

The "Dual-signature PD requested power value Mode A and Mode B" fields shall contain the PD requested power value defined in Table 79–6a for mode A and Table 79–6aa for mode B of a dual-signature PD.

~~If mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0.~~

~~Single-signature PDs shall set the PD requested power value Mode A and Mode B fields to 0.~~

"Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

Info (not part of baseline
Each field has its own Table in Clause 79. Table 79–6a and 79–6b are the only exception where two fields share a Table. I'm splitting them into two Tables to be consistent.

Change Table 79–6a as follows and create new Table 79–6aa:

Table 79–6a— Dual-signature PD requested power value field for Mode A

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~+~~0 through 499.

Table 79–6aa— Dual-signature PD requested power value field for Mode B

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~+~~0 through 499.

79.3.2.6b PSE allocated power value Alternative A and Alternative B

The PSE allocated power value Alternative A field and the PSE allocated power value Alternative B field shall contain the values in Table 79–6b and Table 79ba. ~~for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.~~

Change Table 79–6b as follows and create new Table 79–6ba:

Table 79–6b— PSE allocated power value field for Alternative A

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~+~~0 through 499.

Table 79–6ba— PSE allocated power value field for Alternative B

Bit	Function	Value/meaning
15:0	PSE allocated power value for Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal ~~+~~0 through 499.

Move the paragraph below (with changes) to above Table 79–6b in this subclause.

The "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives. ~~"PSE allocated power value Alternative A" and "PSE allocated power value Alter-native B"~~ These fields are the power levels at the dual-signature PD PI. The PSE uses ~~this~~these value to compute $P_{Class\text{-}2P}$ as defined in 145.2.7. ~~A PSE providing power to a Type 1, Type 2, or single-signature Type 3 or Type 4 PD, places 0 in the "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields defined in Table 79–6b.~~

79.3.2.6e PSE maximum available power

Info (not part of baseline
Power management for single signature and dual signature cares only for the total port power. Parts of the power management then use this power to allocate it per A and B fields. The following changes will allow us to get rid of the requirement of Y=A+B in D3.0 and set Y=0 instead, when Type 3 /4 PSE operating over 4-pairs is connected to dual signature.

The PSE maximum available power field shall contain the highest power the PSE can grant as defined in Table 79 -6e to the port when supporting single-signature PD or dual-signature PD. The PSE shall set the value of this field taking available power budget and hardware capabilities into account.