IEEE802.3bt
# LLDP adhoc


# Meeting #5: Wednesday July 12, 2017
# Revision 002

Yair Darshan
IEEE802.3bt LLDP adhoc chair
Microsemi
ydarshan@microsemi.com

# Meeting # 05 Attendees.

| Name | Employed by: | Affiliated with: | Present |
|---|---|---|---|
| Bruce Nordman | IBL | LBNL | |
| Chad Jones | Cisco | Cisco | Y |
| Chris Bullock | Cisco | Cisco | Y |
| David Tremblay | HPE | HPE | |
| Geoff Thompson | Unemployed | Unaffiliated | Y |
| Heath Stewart | ADI/LT | ADI/LT | Y |
| John Skinner | Sifos | Sifos | |
| Yair Darshan | Microsemi | Microsemi | Y |
| David Law | HPE | HPE | Y |
| Murat Karaorman | ADI/LT | ADI | |
| David Stover | ADI/LT | ADI | Y |
| Lennart Yseboodt | Philips | Philips | Y |
| Arkadiy Peker | Microsemi | Microsemi | Y |
| David Abramson | TI | TI | Y |
| Andrea Agnes | ST | ST | Y |
| Joab Lemahica | ON | ON | Y |
| Dylan Walker | Cisco | Cisco | Y |
| Mathias Wendt | Philips | Philips | Y |
| Fred Dawson | Cherouzs | Cherouzs | Y |

# Proposed Agenda

- Chad has volunteered to take notes of this meeting.

| # | Time | Subject | Owner |
|---|------|---------|-------|
| 1 | 16:00 –16:05 | •Introduction<br>•Patent policy<br>•approving meeting minutes from last meeting<br>•Approving proposed Agenda for this meeting | Yair |
| 2 | 16:10 – 16:15 | Points of agreements from last meetings | Yair |
| 3 | 16:15 – 16:20 | Reviewing A.I. from last meeting. | Yair |
| 4 | 16:20 – 16:35 | Sync the transition between state machine | Yair/Group |
| 5 | 16:35 – 16:45 | Dual-signature state machine and single-signature state machine VS single mode DLL and dual-mode DLL | Yair/Group |
| 6 | 16:45 – 16:55 | MR for clause 33 | Yair/Group |
| 7 | 16:55 - 17:00 | Reviewing response to comment #130 | Yair/Group |
| 8 | *17:00 – 17:45* | *Reviewing updated proposed baseline sent by Yair / Lennart / others* | *Lennart/ Group* |
| 9 | 17:45 – 18:00 | Summarizing of A.I. and points of agreements | Yair |

# Introduction and other businesses 09:00 – 09:05

- **The purpose** of this ad-hoc is to resolve LLDP state machine related comments from D2.4 and related issues for PSE and PDs prior sponsor ballot for D3.0.

- Patent Policy

  - Please read the Patent Policy slides at http://www.ieee802.org/3/patent.html prior the meeting.

  - Approving meeting minutes from last meeting

- **Meetings process**.

  - During the meeting: Questions only after presenter done with his presentation.
  - Follow the agenda as much as possible. Other issues can be tabled to be discuss later at the meeting, over the reflector, or at the next meeting agenda.
  - Discussions over the reflector prior the meeting is valuable and saves time during the meeting to reach consensus.
  - If you want to present material, please ask from the LLDP chair to allocate time in the meeting agenda 2 working days prior the meeting.
  - After the meeting, please send your affiliation and attendance confirmation by email.

# Points of agreements from last meetings

- <u>Meeting #2</u>: Group agrees that the tables reflect the current spec in D2.5.

- <u>Meeting #3</u>:  Group agrees to the concept changes in the Table marked with BLUE text.

- <u>Meeting #3</u>:  Group agrees to the proposed changes to PD DLL state machine Figure 145-43. See Annex B for details.

- <u>Meeting #3</u>: Group agrees to the proposed response to comment #297 D2.4. See Annex B for details.

- <u>Meeting #3</u>: Group agrees to use total available power in the field "PSE maximum available power" in 79.3.2.6e instead of Y=A+B in the PSE for both single signature and dual signature. It will not be part of the state machine but it is available to the user as the rest of the new TLVs. See Annex B for details.

- <u>Meeting #3</u>: In the transition from 4-pair to 2-pair the minimum value that goes to Y is the last allocated value of A or B which ever stays active. (to be added to the description text of state machine and not to the state machine). See concept table.

- <u>Meeting #4</u>: Group agrees with the concept Table. Lennart will confirm by Sunday July 9, 2017.

- <u>Meeting #4</u>: To add text to 145.5.4.X to explain how the PSE and PD get into **sync** when they transition from 2P to 4P and back.

# A.I From LLDP adhoc meeting #4

| A.I | Subject | Owner | Due Date |
|---|---|---|---|
| 1 | To submit LLDP **adhoc** report to Chad for the current status **- DONE** | Yair | Tuesday July 11, 2017. |
| 2 | To allocate time in the Berlin meeting for LLDP **adhoc meeting #5** on **Wednesday July 12, 2017. - DONE** | Chad | |
| 3 | Presenting <u>updated</u> LLDP adhoc report to the group. **- DONE** | Yair | |
| 4 | Presenting initial baseline based on adhoc latest agreements and trying to get consensus during the meeting. . **- DONE.** | Yair/ Lennart | Wednesday  July 12, 2017 |
| 5 | Lennart to review and confirm agreement with the concept table. The rest of the group already confirmed. **- DONE** | Lennart | Sunday July 9, 2017 |
| 6 | Group to review and comment on baseline meeting #4 baseline. See http://www.ieee802.org/3/bt/public/lldpadhoc/Baseline_for_review-LLDP_adhoc_Rev002.pdf | Group | Tuesday July 11, 2017 |
| 7 | To generate updated baseline for the meeting based on item 6. **- DONE** | Lennart/ Yair | |
| 8 | To review and update the DLL state machine for dual-signature to comply with the agreed concept table. **In the TODO list of the adhoc.** | Lennart | |
| 9 | To add text to 145.5.4.X to explain how the PSE and PD get into **sync** when they transition from 2P to 4P and back. **UNDER REVIEW** | John | |
| 10 | To generate response to comment #130. **- Done. See LLDP Baseline** | Group | |

# LLDP concept review – **Cleaner version:** D2.5 text in black.
## Deletions from D2.5 in RED. Additions in BLUE. *(See Annex F for old version)*

| PD requested power value | PSE allocated power value | PD requested power value Mode A | PD requested power value Mode B | PSE allocated power value Alternative A | PSE allocated power value Alternative B |
| --- | --- | --- | --- | --- | --- |

| # | PSE Type | Operating over | PD | TLV field | | | |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | pse_allocated_power | pd_requested _power | pse_allocated _power_Alt(X) | pd_req_power _mode(X) |
| | | | | Y | Y | X (A or B or both) | X (A or B or both) |
| 1 | 3/4 | 4-pairs | SS | 1-999 | 1-999 | 0 | 0 |
| 2 | 3/4 | 2-pairs | SS | 1-999 | 1-999 | 0 | 0 |
| 3 | 3/4 | 4-pairs | DS | 1-999, ~~Y=A+B~~ (**). Y=0. | 1-999, ~~Y=A+B~~ (**) Y=0. | *1-499* | *1-499, Use A and B.* ~~Y=A+B.~~ |
| 4 | 3/4 | 2-pairs | DS | 1-499 , ~~Y=A+B~~ (**) Add: Y is the value of the active Alternative X. **Note (***)** | 1-499 , ~~Y=A+B~~ (**) Add: Y is the value of the active mode X. | 1-499. Set 0 on A and B | 1-499. Use A and B. ~~(*) if mode(X) is inactive, set to value 0.~~ (*) Deleted to resolve #297) |
| 5 | 1/2 | 2-pairs | DS | 1-499, ~~"May Y=A+B"~~ Same as in line 4. if the new TLV fields are used. | Same as in line 4. | Same as in line 4. if the new TLV fields are used. | Same as in line 4. |

The above Table covers all use cases (Type 3/4 connected to Single-signature or dual-signature PD over 4-pairs or 2-pairs and switching between 4-pairs to 2-pairs and back to 4-pairs.
(*) See IDLE state in Figure 145-45 and Figure 145-46 for supporting this use case.
(**) See Annex A for why we need Y=A+B and the alternative solution for it (to use "PSE maximum available power" in 79.3.2.6e.
**(***)David Tremblay** : In the transition for 4-pair to 2-pair what should be the minimum value that goes to Y. Suggested is to go to the value of the last allocated value of A or B. (to be added to the description and not to the state machine)

Microsemi

# Sync the transition between state machine

- (1) Yair: The main guidelines being proposed are:

  - The information from transition from 4P to 2P and back to 4P is available in the PSE and PD hardware state machine in the fasted way. As a result, this variable information can be copied to the DLL state machine and used there.

  - As for the TLV fields to be updated sync between the state machines, it will be done with the existing timings specifications for the DLL state machine.

- Other issues?
- Discussion?
- (2) **Yair:** To continue with the concept of single-signature state machine and dual-signature state-machine and consider NOT TO USE the proposal in the baseline regarding single-mode and dual-mode – Lennart agrees to delete the table with single mode and dual mode.
- (3) Heath: propose to have single PSE and single PD state machine.
- (4) **Yair:** Heath proposal (3) is will be more complicated. We have working simulation of the current D2.5 concept. I suggest not to go to (3).
- (5) **Heath:** To stay in the same state machine when flipping from 4P to 2P and update the parameters (Y etc.) there.
- (6) **Yair:** I believe that this is the best approach (5) it is inline with (1, 2) with minimum modifications to D2.5.
- Group to analyze the pros and cons of the proposals for next meeting #6.

# Dual-signature state machine and single-signature state machine VS single mode DLL and dual-mode DLL

- Currently the single-signature state machine and dual-signature state machine are independent

- The single-signature state machine is used when operating over 2P or when single-signature PD is supported.

- The dual-signature state machine is used when operating over 4P and each Alternative/Mode is operate independently.

- In the updated concept we need to put zeros in the unused fields and it looks that when we are operating on the "main" relevant state machine, we may need to "look" at the other state machine to updated the relevant variables the zero so one can say that we need to work with all the state machine.

- DISCUSSION:

- **Yair:** at first iteration, I would like to keep it as it is. **Independent and not to operate all state machines**. It is more simple and controlled behavior **especially in software**. As for to "look" to the other state machine and update variables to zero, **we can do the following**: Before we leave the current state machine, we will update the variables to zero and than transition to the other state machine. In this way we don't need to look on two state machines.

- *In addition*, one of the things that bothers me in the proposed baseline in the table on page 2 is for example: when you change from "145.5.3.2 Attribute to state diagram variable mapping (single-signature)" to "145.5.3.2 Attribute to state diagram variable mapping (singlemode

- DLL)" is confusing since single signature is working on 4-pairs i.e. both modes and not on single mode while Type 1 and 2 are working on two pairs (single mode), so the proposal I feel that will create more issues than help.

- Discussion: Lennart agrees to delete the table in the baseline that deals with single mode and dual mode operation. As a result we currently staying in the baseline with the concept of single-signature and dual-signature state machines.

# MR for clause 33

- Per the concept agreed in the concept table, to put zero in:
  - (a) PSEallocatedPower and PDrequestedPower fields when operating with dual-signature over 4-pairs or
  - (b) PSEallocatedPower_Alt(X) and PDrequestedPower_mode(X) when operating with single-signature
- We have now changed this legacy field (a) to include 0 as a valid value. For Type 1/2 this was an illegal value, which now becomes a legal value, which leads to undefined behavior if used. This would not be a problem, were in Clause 33, by mistake, it allows the value 0 in the variable that is linked to this field but in the TLV definitions in clause 79 it is correct i.e. the values 1-255 are only permitted.
- We will need to file an MR to change the DLL state diagram in Clause 33, to restrict the value PSEAllocatedPowerValue from 1 through 255. Both changes together do not result in a change in legacy requirements.
- **Discussion: Group agree**

# Comment #130, #293 D2.4 (D2.5 Page 74 line 11)

Added text, "Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension."
Incorrectly blocks legacy types from using TLVs, Power status, System setup, PSE maximum available power, Autoclass, and Power done. The existing text does indicate what legacy Types are required to place in all Type 3 and Type 4 extension fields.
*SuggestedRemedy*
Strike the called-out text.
ACCEPT IN PRINCIPLE.
OBE by 293
Comment 293 has the following response:
ACCEPT IN PRINCIPLE.
No changes to draft.
LLDP ad hoc was formed.
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Discussions: See meetings 1-4 discussions on Annex E.

- David Stover/Heath : To move 4PID field to the legacy TLVs and not allow Type 1 and 2 devices to use the new TLVs.

Yair: OK. It simplifies the issue.

Lennart: Implemented in the baseline.

Yair: Group to review the detailed proposal for the response to #130 D2.4 in the LLDP Baseline.

Group Agrees: YES (and change the "shall" to "out of scope")

# Points of agreements in this meeting

- Group to verify that that clean form of the concept table technical content is identical to the agreed concept table from meeting #4 shown in Annex F.

- To file MR to change the DLL state diagram in Clause 33, to restrict the value PSEAllocatedPowerValue from 1 through 255. Proposed change is not resulting in a changes to legacy requirements.

- Comment #130 from D2.4 resolution is resolve per the proposal in the LLDP baseline after changing the "shall" to "out of scope"

- **LLDP baseline:**
  - To delete from LLDP Baseline the proposed table to change from LLDP single-signature and dual-signature state machines to single-mode and dual mode operation. As a result we currently staying in the baseline with the concept of single-signature and dual-signature state machines.
  - To change the text from "Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension" to "Type 3 and Type 4 extension are out of scope for Type 1 and Type 2 devices" or equivalent wording.
  - To consider the changes to dll_enable (it was dll_enable_mode/Alt(X)) in the proposed LLDP baseline. We had good reason for why did I tin D2.5.

# A.I for next LLDP adhoc meeting #6

- Lennart will update the DLL state machines to meet the updated table concept
- Lennart to update baseline per meeting #5 discussion results.
- Heath and Yair will review LLDP baseline.
- Yair and Lennart to review John Skinner proposal regarding the sync between transition from 4P to 2P and back.

# Annexes

# Annex A: Why we need Y=A+B as currently in the spec?

**Argument #1**

- When we do LLDP simulations between Type 1, 2 PSE connected to dual-signature PD we encounter the following problem:

- Type 1, 2 PSE has only the pse_allocated_power field. He doesn't know about any other field such pd_requested_power_modeA or B fields/values.

- It means that PSE Type 1 and 2 can communicate with any PDs with pse_allocated_powerand and pd_requested_power fields only.

Now let's see what is going on step by step:

- PD puts values in pd_requested_power_modeA and B fields (what ever the values are)

- pd_requested_power_modeA and B fields are send through LLDP protocol and PSE tries to read it.

- PSE has only access to the content of pd_request_power_value because it doesn't know any other fields. If the content of pd_request_power_value in dual-signature PDs will be zero and not pd_request_power_value= pd_request_power_value_modeA+ pd_request_power_value_MODEb, the PSE will see ZERO as the pd_request_power_value so the pse_allocated power value will be ZERO as well. So how it will work?

- The solution is: If in the PD we will set pd_request_power_value= pd_request_power_value_modeA + pd_request_power_value_modeB then pse_allocated_power_value can work with pd_requested_power_value. Alternative solution for the 2-pair case: pd_request_power_value= pd_request_power_value_mode(X) where X is the active pairset.

## Argument #2

- Imagine that you have a dual signature that want on  modeA=45W and modeB=30W.

- But, PSE has only 29W.

- The question is how PSE will allocate the power. Please note the you have a single main power supply and the PSE **first** decides how to allocated power per port (i.e. the power needed per the whole port and then per the alternatives per the PD assigned class for each pair set (this is the only way it works in PSEs).

**Now, Per the rules:**

- PD mode A wants 45W but PSE has total 29W or <29W or whatever for mode A.

- PD mode B wants 30W but PSE has total 29W or <29W or whatever for mode B.

- So what PSE will do?

- Option 1: PSE will allocate power per the previous ratio (30W/45W). But this is not defined.

- Option 2: PSE will allocate power by splitting the 29W to half for each mode.  But this is not defined

- OR option 3: PSE supply the total power as well (The sum field) and PD will decide what to do in order that the whole PD will work or one of the PD modes will work or nothing will work.

  This is the best option. Why? Because this scenario is no different than the case when PSE is connected to single signature PD that wants 51W and PSE has only 30W. In this case, you give PD only 30W and let PD to decide how to use it. Please remember that in all dual signature PDs mode A and mode B are talking to each other by a single MCU.

Other alternative solution to this problem is to use the field "PSE max available power" which should be the total port power. We need to clarify in 79.3.2.6e that this value is applicable for PSE that supports single-signature and dual-signature.

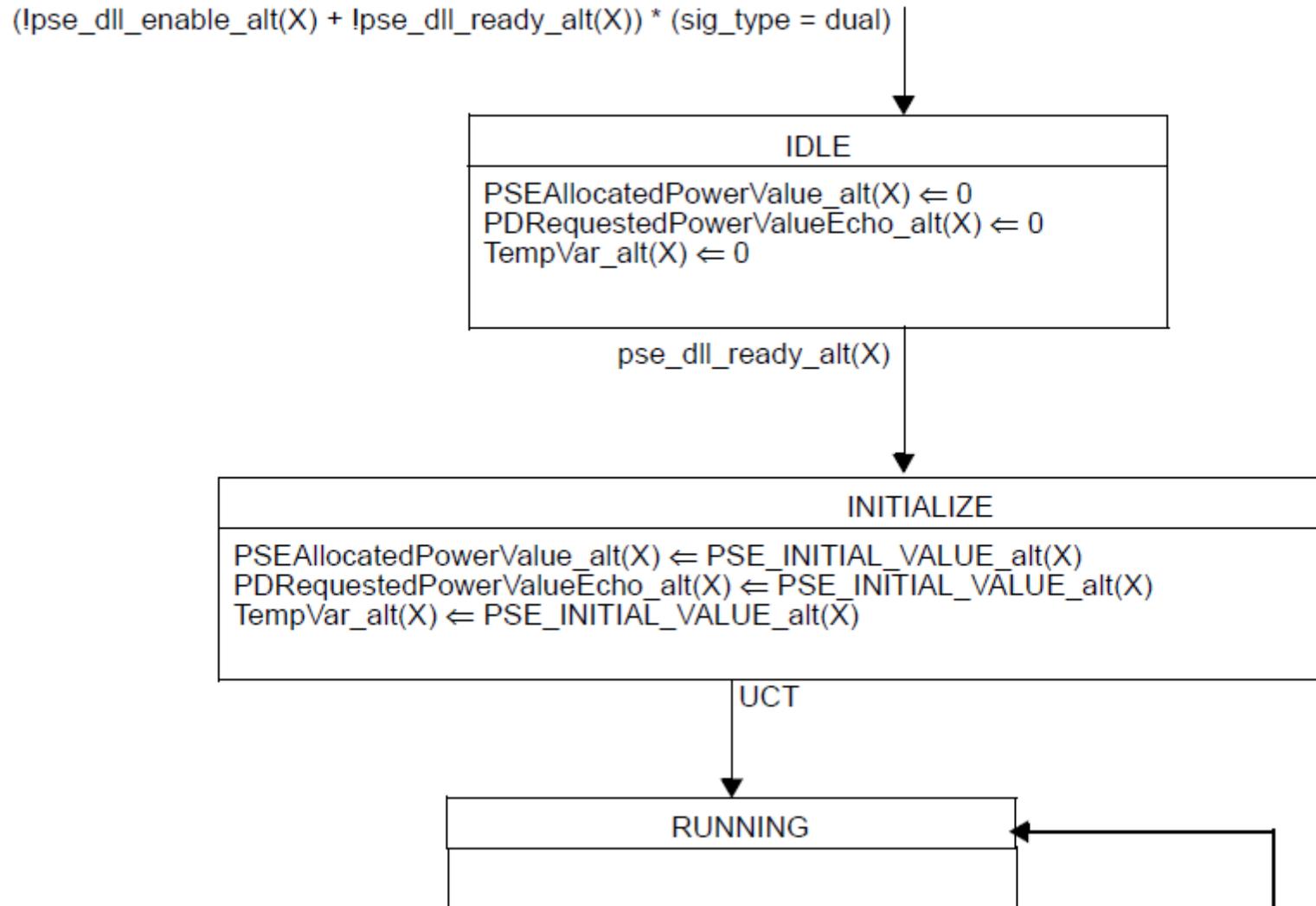## Annex A: Why we need Y=A+B as currently in the spec? -2

- Argument #3

High level power management care only for the total port power. The power management per pairset is kind of sublayer of the power management system. It is useful to pass the total power through the TLVs field. This is in general how current PSEs systems works.
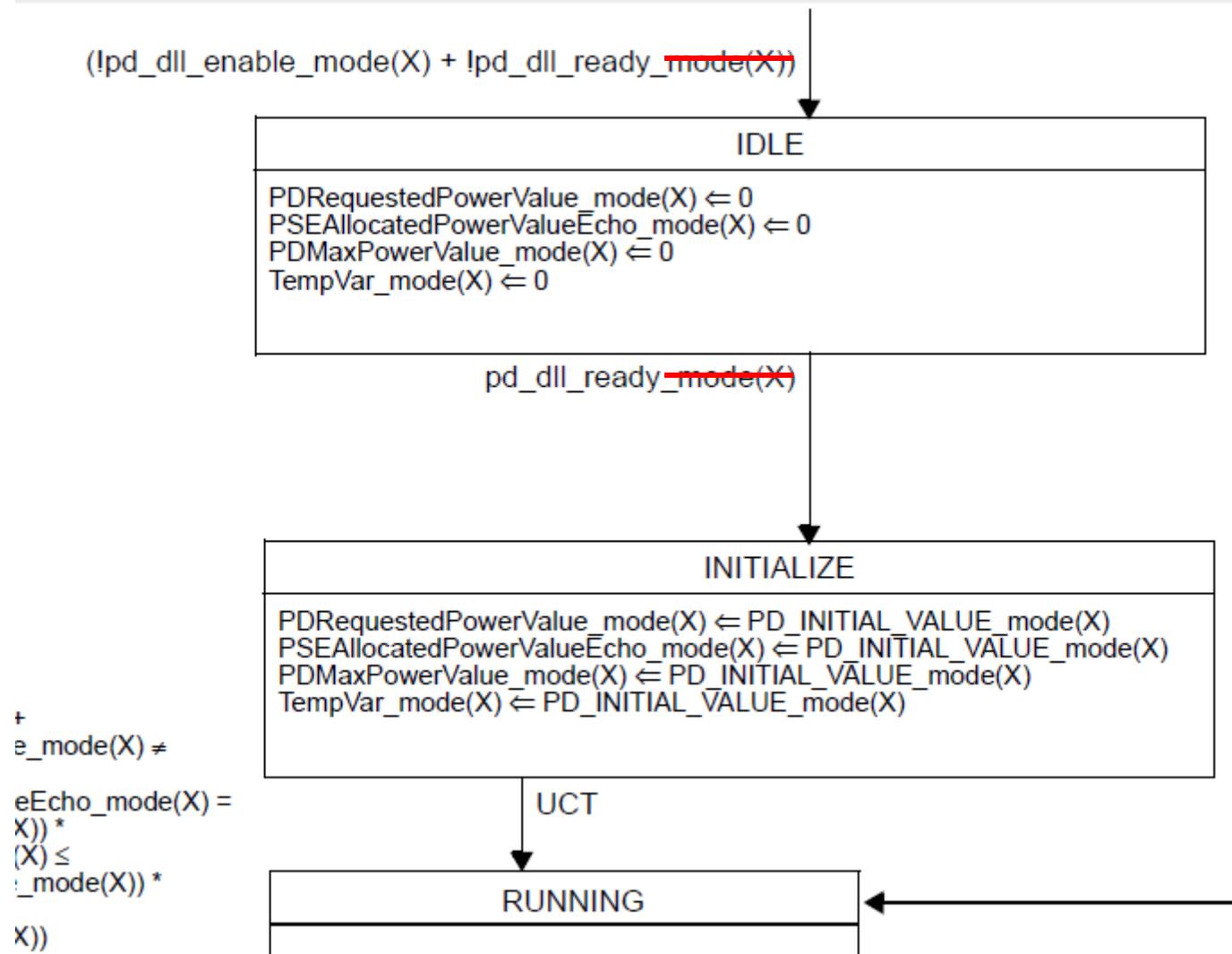
Other alternative solution to this problem is to use the field "PSE max available power" which should be the total port power. We need to clarify in 79.3.2.6e that this value is applicable for PSE that supports single-signature and dual-signature.

$$(!pse\_dll\_enable\_alt(X) + !pse\_dll\_ready\_alt(X)) * (sig\_type = dual)$$

**IDLE**

$PSEAllocatedPowerValue\_alt(X) \Leftarrow 0$
$PDRequestedPowerValueEcho\_alt(X) \Leftarrow 0$
$TempVar\_alt(X) \Leftarrow 0$

$pse\_dll\_ready\_alt(X)$

**INITIALIZE**

$PSEAllocatedPowerValue\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$
$PDRequestedPowerValueEcho\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$
$TempVar\_alt(X) \Leftarrow PSE\_INITIAL\_VALUE\_alt(X)$

UCT

**RUNNING**

# Annex B: Comment #297 D2.4 (Page 75 line 12 in D2.5) - Figure 145-44
## Proposal for a change marked in RED. Group is OK.



$(!pd\_dll\_enable\_mode(X) + !pd\_dll\_ready\_\cancel{mode(X)})$

**IDLE**

$PDRequestedPowerValue\_mode(X) \Leftarrow 0$
$PSEAllocatedPowerValue\bar{E}cho\_mode(X) \Leftarrow 0$
$PDMaxPowerValue\_mode(X) \Leftarrow 0$
$TempVar\_mode(X) \Leftarrow 0$

$pd\_dll\_ready\_\cancel{mode(X)}$

**INITIALIZE**

$PDRequestedPowerValue\_mode(X) \Leftarrow PD\_INITIAL\_VALUE\_mode(X)$
$PSEAllocatedPowerValue\bar{E}cho\_mode(X) \Leftarrow PD\_INITIAL\_VALUE\_mode(X)$
$PDMaxPowerValue\_mode(X) \Leftarrow PD\_INITIAL\_VALUE\_mode(X)$
$TempVar\_mode(X) \Leftarrow PD\_INITIAL\_VALUE\_mode(X)$

+
$e\_mode(X) \neq$

$eEcho\_mode(X) =$
$X)) *$
$(X) \leq$
$\_mode(X)) *$

$X))$

UCT

**RUNNING**

## Annex B: LLDP concept review as agreed in D2.5 – Updated per the current text
## Proposal for a change marked in RED.

- Discussion
  - The Table in previous slide is the current concept per D2.5. This closes questions from meeting #1 regarding item 4 and item 5 in the Table presented in meeting #1 (See Annex) regarding if it should be Y=A+B or Y=A or Y=B.

  Yair+Lennart discussion:
  - Y=A+B can be replaced to Y=mode(X) in the PD and Y=Alt(X) in the PSE. This is alternative solution to argument #1 in Annex A and will resolve the double information of A, B and Y=A+B confusion argument raised by Lennart.
  - We have the information of total available power in the field "PSE maximum available power" in 79.3.2.6e. This resolve argument #2 in Annex A.

- To resolve #297, Lennart suggests: In order to request power on the unpowered pairset, see proposed changes in the red text. In addition, the pd_dll_ready_mode(X) need to be changed to pd_dll_ready to allow progressing to the INITIALIZE state in case PD want power on the unpowered pairset. No changes required in the PSE portion.

- Yair it will work:

- The proposal is:
  - To change from pd_dll_ready_mode(X) to pd_dll_ready in the PD state machine.
  - To change "if this mode/Alt is inactive, set to value 0" to "if this Alt is inactive, set to value 0" i.e. keep this requirement only to PSE.

- Group is OK.

# Annex B: Comment #297 D2.4 (Page 75 line 12 in D2.5)

- Comment #297 D2.4 (D2.5 Page 78 line 46)

"If Mode (X) is non-active while the other mode is active, the inactive PD requested power value Mode (X) field value shall be set to 0."

- What is this trying to do ? The PD may wish to ask for power on an unpowered Mode...

*SuggestedRemedy*

Strike sentence.

- ACCEPT IN PRINCIPLE.

no changes to draft.

An LLDP ad hoc was formed

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Yair: What we are trying to do is:

- In Figure 145-44 and Figure 145-45 power control state diagrams when connected to dual-signature PD, we add in D2.3 an IDLE state in order to resolve non active Alternative(X) or no active mode(X) by setting the relevant variables to zero prior going to INITIALIZE state.

  - Figure 145-45: PSEAllocatedPowerValue_alt(X), PDRequestedPowerValueEcho_alt(X) and TempVar_alt(X)

  - Figure 145-46: PDRequestedPowerValue_mode(X), PSEAllocatedPowerValueEcho_mode(X), PDMaxPowerValue_mode(X) and TempVar_mode(X))

# Annex B: Comment #297 D2.4 (Page 75 line 12 in D2.5)

Discussion:
Yair: See concept description for why we did it.
A.I: Group to verify that they are OK with the state machine in Figure 145-43 and Figure 145-44.

- Lennart response: The proposed response to this comment is to adopt:
  - To change from pd_dll_ready_mode(X) to pd_dll_ready in the PD state machine.
  - To change "if this mode/Alt is inactive, set to value 0" to "if this Alt is inactive, set to value 0" i.e. keep this requirement only to PSE.

- **Group to discuss.**

- GROUP OPINION? Group is OK.
  - The modifications proposed to the state machine in Figure 145-43?
  - To change from pd_dll_ready_mode(X) to pd_dll_ready in the PD state machine.
  - To change "if this mode/Alt is inactive, set to value 0" to "if this Alt is inactive, set to value 0" i.e. keep this requirement only to PSE.

# Annex C: New topic – do we need the Y=A+B as currently in the spec?

- We agree that D2.5 is describe in the tables. And next meeting to present new table with the changes proposed – Group OK.

- Lennart presentation

- Yair inputs for the reasons we did it (See Annex A).

- Discussion

- (*) Lennart: We have the information of total available power in the field "PSE maximum available power" in 79.3.2.6e. This resolve argument #2 in Annex A.

- Yair: Agree.

- ## Yair: Group is OK (*)

## Annex D: -Table items 4 and 5 Discussion.
### -Item 4: Type 3 / 4 PSE connected to dual-signature over 2-pairs
### -Item 5: Type 1 / 2 PSE connected to dual-signature over 2-pairs (with or without the use of new TLVs fields)

- **Yair:**

-Item 4: The system was working over 4-pairs and now it is working over 2-pairs for some reason.

**-In the PD side:**

(a) Using both fields A and B although one of the pairs is not active. The reason is when it will be active to allow its operation in the state machine.

(b) The Y field must contain the value of the active field due to the fact that later, the Y field will have to communicate with the PSE Y field (operation over 2-pairs).

**-In the PSE side:**

(c) We need that the power value of the active field will be stored in Y so PSE Y field can communicate with PD Y field.

(d) In addition, we want to know what is the value of the active field to make sure that it is the correct value of the Y field because at this time of decision, the system may go through some undefined behavior during the transition and we must know what is the correct value.

(e) In addition to (d) it also gives us the correct last value of the active field prior the transition per David Tremblay comment.

-As a result, we need in the PSE side to use Y=X where X is the active field value. And we need X.

-Item 5: Type 1 or 2 PSE connected to dual-signature PDs (working over 2-pairs). Two subcases: (1) The PSE doesn't use the new TLVs. (2) The PSE can use the new TLVs. **PSE side:**

-Case 1: PSE have no choice but to use only the Y field (A and B fields doesn't exist).

-Case 2 (which is optional allowed case in the spec):  The PSE has accesses to the new TLVs. Y is connected to the active field A or B hence PSE knows Y and X (A or B). It is not important that PSE doesn't do connection check. It knows from LLDP fields that it is dual-signature. So it is the same as line 4.

**PD side:** It is dual-signature PD which is the same as line 4.

-As a result, we need in the PSE side to use Y with the content of the active field value. I wanted to set also the X filed where X is the active field and John is proposing to set it to X=A=B=0 whenever dual-signature is operated over 2-pairs.

Comments:

John Skinner: See John analysis summary.

Yair: I agree in principle to John analysis and updated my proposals accordingly. John main argument is the operation of PSE Type 3 or 4 over 2-pairs when connected to dual-signature PD is done with single-signature state machine that uses only the Y fields.

Lennart: Agrees with John analysis.

## Group is OK with the concept table. Lennart will review and confirm by Sunday July 9, 2017.

# Annex E: Comment #130, #293 D2.4 (D2.5 Page 74 line 11)

Added text, "Type 1 and Type 2 devices shall not support the Type 3 and Type 4 extension."
Incorrectly blocks legacy types from using TLVs, Power status, System setup, PSE maximum available power, Autoclass, and Power done. The existing text does indicate what legacy Types are required to place in all Type 3 and Type 4 extension fields.
***SuggestedRemedy***
Strike the called-out text.
ACCEPT IN PRINCIPLE.
OBE by 293
Comment 293 has the following response:
ACCEPT IN PRINCIPLE.
No changes to draft.
LLDP ad hoc was formed.
---------------------
Yair: The proposed response to delete this text make sense. No reason to block new features from existing Type 1 and 2. Strike the called out text.
Geoff: All "shalls' should be in clause 145.
Heath: We agree to delete the text if PSE/ PD requested/allocated power mode A/B is set to zero when Type 1 and Type 2 PSE are used.
Jhon/Yair: In this case of Type 1/2 PSE connected to dual-signature PD, the fields are already defined. We need to focus only on the PSE fields since DS PD has access to all fields.
Lennart: @Heath, makes only sense to PSE allocated power. Doesn't make sense to PD requested power.
Yair: Not clear why @Heath makes sense only to PSE. If PSE can use the new fields for legacy PSEs, why not to use the same rules used in Type 3, 4 PSEs that have access to this field by default. The idea is to enable legacy PSEs to benefit from new features and not to disable them.
Heath A.I to generate comment and remedy for discussion for next time.
David Stover: It looks that we have covered this issue in this meeting adhoc presentation and/or by Lennart presentation.

David Stover:  I certainly understand the desire to extend support for e.g. power price index, parametric measurement reporting, etc. to Clause 33 (C33) devices that can support the extensions. However, if all of these TLV extensions are made available to C33 devices, I believe there is insufficient guidance in Clause 79 to enforce the desired limitations on a C33 device. For example, the TLV extensions allow PSEs to indicate they provide 4 pair power, to indicate and negotiate up to 99.9W of power, and to indicate they are a Type 3 or Type 4 PSE. Certainly, C33 PSEs should not be allowed to indicate this information to a PD. In particular, raising the power level for 2 pair systems is prohibited by our PAR. To resolve this comment we'll also need to come to agreement on the additional limitations placed on C33 devices when using the TLV extensions.

Lennart: The Clause 33 state diagrams already have a limit of 25.5W for DLL negotiation. So there is no problem in thus case.

Lennart:: The only reason I made the comment to get rid of that shall, is for the 4PID bit. Everything else is either "does not apply", or "pretty clear what to do".

Lennart: I'm not sure I see what limitations need to be defined that are not already clearly in Clause 33 ?

Yair: Comment  #293 is similar and addressed in addition to 4PID bit the other new features we can use in Type 1 and 2 with the new TLV fields.

**Yair: David: Can you make a list of TLVs that you believe need to be addressed with limitations.**

**Heath/David Stover sendand Yair responsed:**

http://www.ieee802.org/3/bt/public/lldpadhoc/Recommended%20Type%201%20and%202%20TLV%20Usage_WITH_YAIR_RESPONSE.PDF

- Yair: The current spec is OK for the above use case. No need to change. See the following arguments.
- 1) The question was how to use TLVs when Type 1 or 2 PSE is connected to Type 3 and 4 dual-signature PD. So, my review is addressing that use case. The use case in which Type 1 and 2 is connected to PD Type 1 and 2 is addressed in clause 33.
- 2) Regarding Power Status, Dual-signature power Classx Mode A / B and Power Class x: See 79.3.2.6.c.  If the use case is Type 1 and 2 PSE is connected to dual-signature PD then If the device generating the TLV is a PD Type 3 or 4, then you must use it per the table and you can't set the lines that I marked with "X" as 000 etc. That is why I believe your proposal is incorrect and we should keep it unchanged.
- 3) In addition to (2) Type 3 and 4 dual-signature PD can't be Type 1 and Type 2 PD when connected to Type 1 and 2 PSE. They are still Type 3 and 4 dual-signature PD.
- 4) Regarding PD load: The PD is dual-sig PD and it is Type 3 or 4 PD so the PD knows if this field need to be set to 1 (isolated loads) or 0 (not isolated loads). Not clear what you are trying to block by proposing this option. I believe it should be unchanged as well. The PD knows what it is and it doesn't need the PSE to know its properties.
- 5. The question was a bout new TLV fields used by the PSE Type 1 and 2 when connected to dual-signature PD. It is not clear why you have addressed PD TLV fields while the question was about PSE related TLV fields?
- So, to summarize: I don't see a good reason to change this fields when Type 1 or 2 PSE is connected to dual-signature PD.
- Lennart: Originally I care about the 4PID.
- Yair/John: David Stover/Heath work is addressing PD TLVs for dual-signature PD that cant be changed. The question was for PSE Type 1 and 2 that uses new TLV fields and they didn't address this point.
- Yair: OK, we will finalize it in the Berlin meeting. Meanwhile since it was Lennart comment, Lennar will generate his response to #130. Yair will add his inputs to the proposed remedy.
- Yair: Meanwhile it looks that there is a consensus how to resolve this which is to move the 4PID field to the legacy fields and not allow Type 1 and 2 devices to use the new TLVs.

# Annex F: LLDP concept review: D2.5 text in black. Proposal for a change marked in RED. Agreed new concept marked in BLUE. Concept agreed on meeting #4

| PD requested power value | PSE allocated power value | PD requested power value Mode A | PD requested power value Mode B | PSE allocated power value Alternative A | PSE allocated power value Alternative B |
|---|---|---|---|---|---|

| # | PSE Type | Operating over | Connected to a PD | TLV field | | | |
|---|---|---|---|---|---|---|---|
| | | | | pse_allocated_ power | pd_requested _power | pse_allocated _power_Alt(X) | pd_req_power _mode(X) |
| | | | | Y | Y | X (A or B or both) | X (A or B or both) |
| 1 | 3/4 | 4-pairs | SS | 1-999 | 1-999 | 0 | 0 |
| 2 | 3/4 | 2-pairs | SS | 1-999 | 1-999 | 0 | 0 |
| 3 | 3/4 | 4-pairs | DS | 1-999, Y=A+B (**)<br>Lennart+Yair: Y=0. | 1-999, Y=A+B (**)<br>Lennart+Yair : Y=0. | *1-499* | *1-499, Use A and B. Y=A+B.*<br>Lennart+Yair : Delete Y=A+B |
| 4 | 3/4 | 2-pairs | DS | 1-499 , Y=A+B (**)<br>**Yair+Lennart**:<br>1) Delete Y=A+B<br>2) To add: Y is the value of the active Alternative X.<br>**David Tremblay** : In the transition for 4-pair to 2-pair what should be the minimum value that goes to Y. Suggested is to go to the value of the last allocated value of A or B. (to be added to the description and not to the state machine) | 1-499 , Y=A+B (**)<br>Yair+Lennart:<br>1) Delete Y=A+B<br>2) Add: Y is the value of the active mode. | 1-499.<br>Yair+Lennart+John: Set 0 on A and B | 1-499. Use A and B.<br>(*) if mode(X) is inactive, set to value 0.<br>Lennart+Yair:<br>To resolve #297, delete (*). |
| 5 | 1/2 | 2-pairs | DS | 1-499, "May Y=A+B"<br>**Yair+Lennart**: Delete "May Y=A+B"<br>**Yair**: To add: Y is the value of the active Alternative X if the new TLV fields are used. | Same as in line 4. | If new TLV fields are used, set A and B to 0. | Same as in line 4. |

The above Table covers all use cases (Type 3/4 connected to Single-signature or dual-signature PD over 4-pairs or 2-pairs and switching between 4-pairs to 2-pairs and back to 4-pairs.

(*) See IDLE state in Figure 145-45 and Figure 145-46 for supporting this use case.

(**) See Annex A for why we need Y=A+B and the alternative solution for it (to use "PSE maximum available power" in 79.3.2.6e. This resolve argument #2 in Annex A)