Electrical Specifications for 4-Pair

IEEE802.3bt – March 2014 Plenary

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Motivation

- To explore the electrical specification that will allow as many implementations as possible
- To identify use cases that might potentially have interoperability or other concerns

Table Items

- Detection
- Inrush (Startup)
- Current Limiting
- Disconnect

Detection

- Current Standard says “The PSE shall turn on power only on the same pairs as those used for detection”
- Possible Specification for 4PPoE:

  - PSE must detect at least on one of the 2Pairs (ALT-A or Alt-B) before turning on 4pair power

  - Or, PSEs may detect on both ALT-A and ALT-B pairs before turning on 4pair power (this should use a interleaved scheme – to accommodate all PD designs)

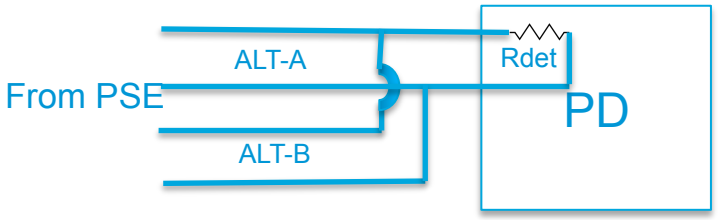
Key Considerations

1. *BACKWARD COMPATIBILITY*: Current Standard states the following for a PD

"PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

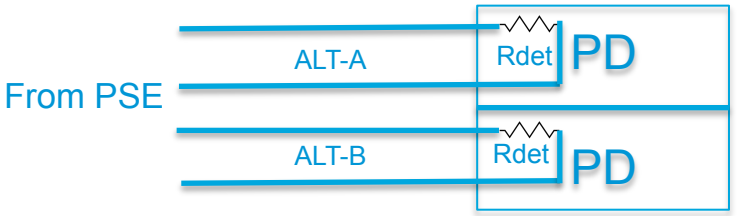
The above allows 2 different types of "AT" PD implementations in field today both of which are IEEE802.3at compliant, as shown below

PD Implementation 1



One combined Detection Resistance for Mode A and Mode B

PD Implementation 2



Separate Detection Resistance for Mode A and Mode B

We need to backward support both "AT" PD implementations in-field today. The "bt" detection specification should make sure both "AT" PD implementations will be detected as valid.

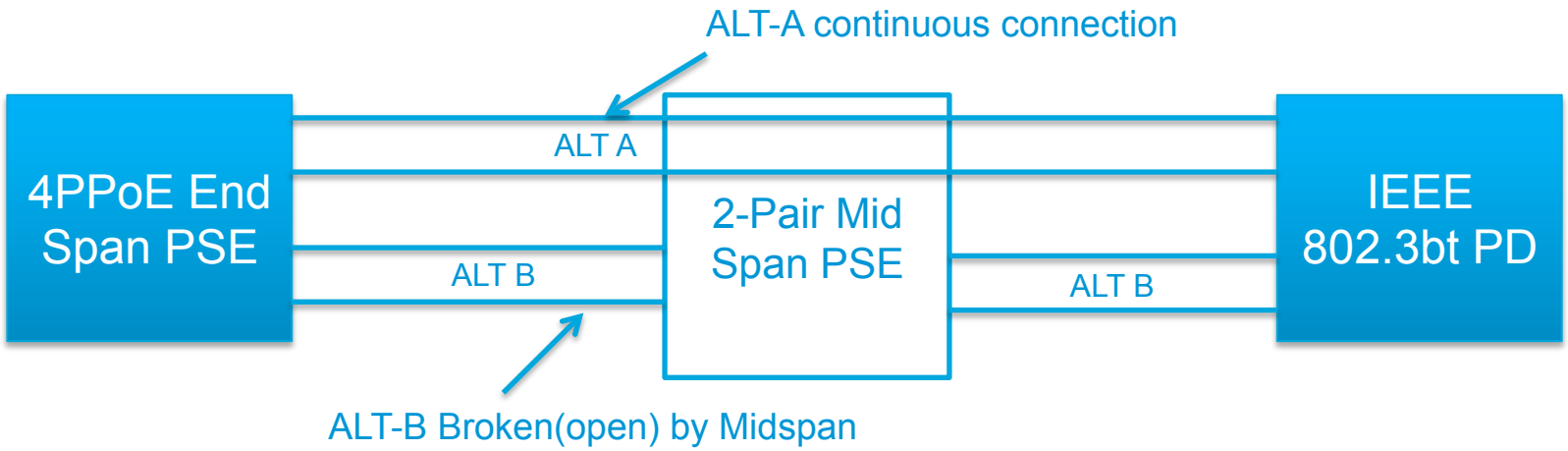
(ie) A) If PSE detects both Alt-A and Alt-B (optional clause from slide 4) – it needs to do it in an interleaved manner to support PD implementation 1

B) If PSE detects only on either Alt-A or ALT-B, then it needs to make sure Rdet is seen and not Rdet/2 on PD implementation 2

Potential Impact

- Potential Live Wire Scenario for implementations that don't cover the or clause from slide 4

  -When a valid PD is connected only on one of the 2-pair and other 2pair has no valid PD connected(e.g.: see picture below) – turning on voltage to the open set of pairs would affect network components



A Possible PoE Installation

Inrush (Startup)

- Current Standard specifies at >30V, 450mA for first 75ms (for full specification please refer to the standard)
- Possible Specification for 4PPoE:

  - Same as current standard for each of the 2pair channel in a 4pair Port (the max inrush current should be decided based on system imbalance).

  - Or A combined 2X Inrush limit for a 4Pair port

NOTE:

1. Other specifications are possible but above is arrived assuming – parity with IEEE802.3AT → 450mA over 2pair.

Current Limiting

- Current Standard specifies

  Optional Icut and Tcut → Icut between P_{Pd}/V_{port} and $I_{lim;}$ Tcut between 50 to 75ms

  Ilim and Tlim → Defined by a graph

- Possible Specification for 4Pair:

  - X mA (for 51W case, this will be same as current standard) for each of the 2pair channel in a 4pair Port

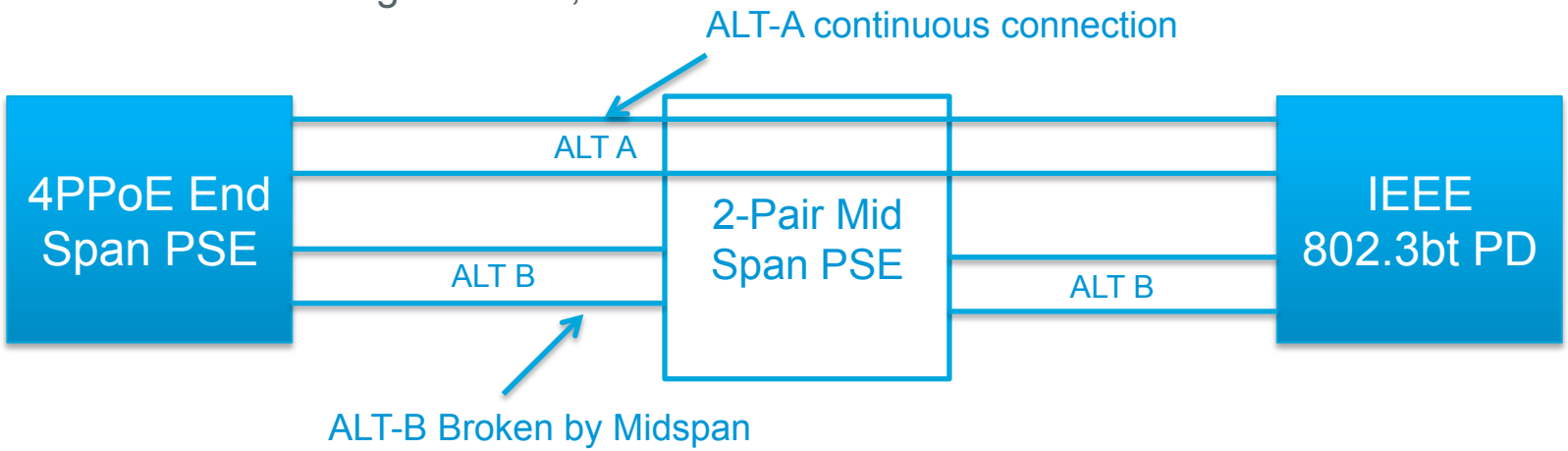
  - Or A combined 2X the current limit for a 4Pair port

NOTE:

- Other specifications are possible but above is arrived assuming – parity with IEEE802.3AT → same Current limit over 2pair

Potential Interoperability case #1

- Consider the following scenario,



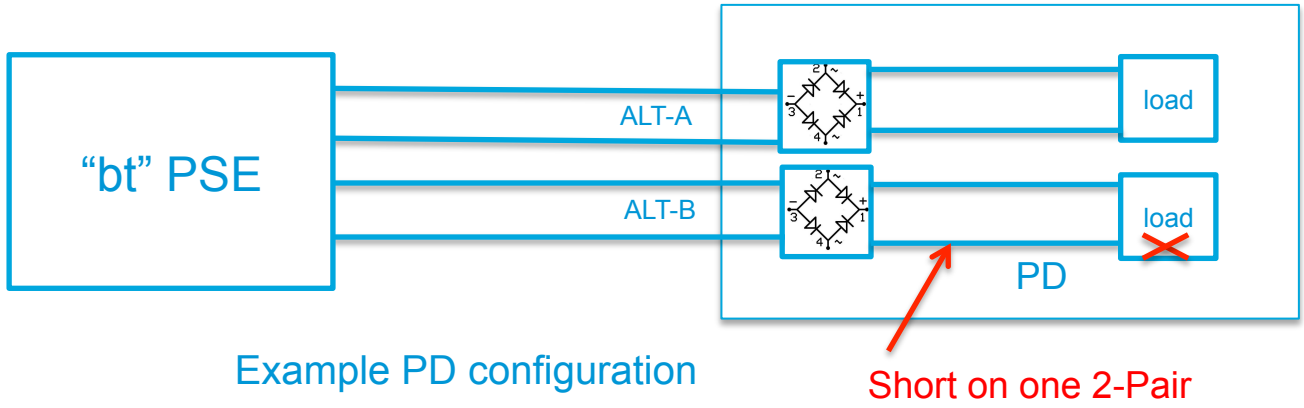
  - There are lot of mid-spans in the field today. IEEE802.3AT was written such that end-spans and mid-spans can co-exist → allows ease of deployment
  - So a installation like above is possible
  - Assuming End span PSE is providing power to the BT PD → all current goes through ALT A (ALT-B broken by midspan)
  - If current limiting is defined as shown in slide 7, then[1]
    - Combined 2X Current Limit PSE will power up
    - Independent XmA per 2Pair PSE will not power up

} Interoperability concern!!!

[1]This presentation doesn't suggest one is better than the other.

Potential Interoperability Case #2

- Consider an example Connection shown below.



- A Short on one of the 2-pairs
  - Combined current limit will remove all power
  - Independent current limit will remove power only from ALT-B

  } Interoperability concern!!!

- Will there be such a PD configuration??
  - PDs that would like to keep key core functionality separate from accessories (to avoid accessory fault causing full system shutdown)

DC-Disconnect

- Current Standard specifies Imps, Tmps and Tmpdo
- A possible specification for 4Pair (type3/type4 PD):

  - Imps, Tmps and Tmpdo value would be applied on 4pair collectively.

  - Or, PSE capable of identifying the PD configuration (1 Vs 2 chips, Y cable etc.,) may choose to remove power from a 2pair, if MPS is not maintained on that 2pair (imbalance should be taken into consideration)

Consideration

- Potential Live Wire Scenario for combined DC-Disconnect
  - If an implementation disconnects the load on one of the 2-pairs only, line voltage will still be present on that pair.

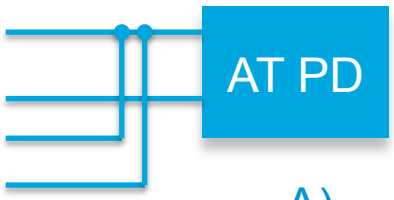
Summary

Function	Things to consider
Detection	- Considerations to guarantee backward compatibility (outlined in Slide 5) - Potential Live Wire Scenario
Inrush and operational Current Limit	Interoperability concerns
DC-Disconnect	Live Wire Scenario

THANK YOU

Backup Slides

Inrush/Current Limit - Options



A)

B)

C)

- “at” PD should always work with “bt” PSE
- The above 3 cases are considered for both options below in the table

X – Inrush/Current limit as per IEEE 802.3AT

	Current Per 2Pair	Total 4Pair Current	Supports AT PD in
Option 1	X/2 mA	X mA	A
Option 2	X mA	2X mA	A, B, C