Cost Comparison between Different 4PPoE Implementations

Kousi Balasubramanian
John Wilson
Sesha Panguluri
David Abramson

IEEE 802.3bt, March 2014 Plenary

Contributors

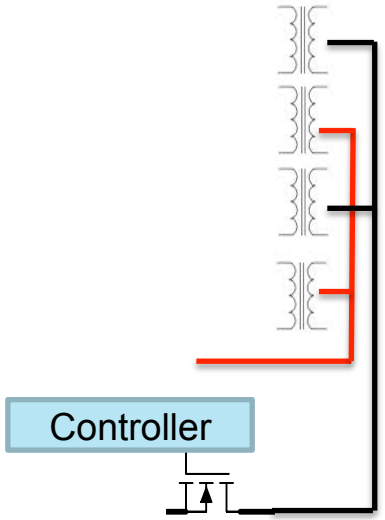
- Jean Picard – Texas Instruments
- Victor Renteria – Belfuse Inc.
- Farid Hamidy – Pulse Electronics
- Ken Coffman – Fairchild

Supporters

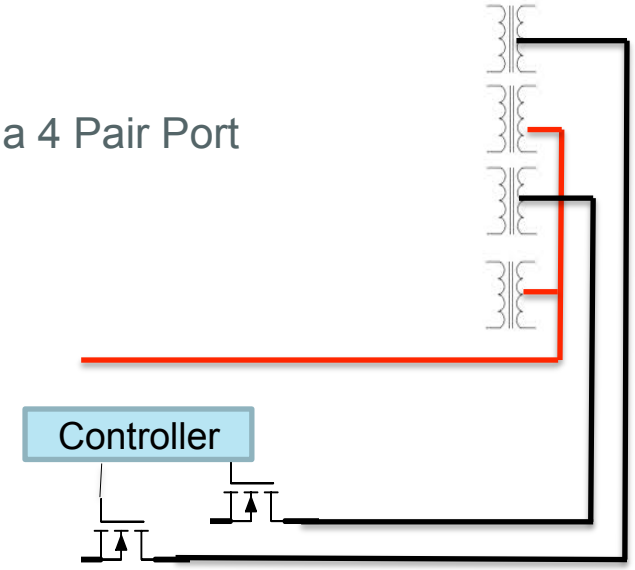
- Jean Picard – Texas Instruments
- Farid Hamidy – Pulse Electronics
- Victor Renteria – Belfuse Inc.
- Fred Schindler – Seen Simply
- Miklos Lukacs – Silicon Laboratories
- David Tremblay – Hewlett Packard
- Leonard Stencel - Bourns
- Yair Darshan – MircroSemi
- Rick Frosch – Phihong
- Yakov Belopolsky – Bel Stewart Connector
- Ken Coffman – Fairchild

Terminology

- 1 Power Channel
  - One FET switch for a 4 Pair Port



- 2 Power Channel
  - One FET switch per 2 pair for a 4 Pair Port



System Development & Deployment Costs

- PoE subsystem cost consists of 3 elements:

1. Material Costs

   PCB, Power suppl(ies), RJ45+Magnetics, Port Controller IC, Per-Port Discretes, I2C Bus Isolation

2. Development Costs

   Schematic design & component selection

   Layout: prototyping, system test, refinements

   Thermal studies

3. Inventory Costs and Marketing/Time-To-Market (TTM)

   Inventory: carrying costs, taxes, etc.

   Marketing (soft costs): opportunity loss if TTM stretches out

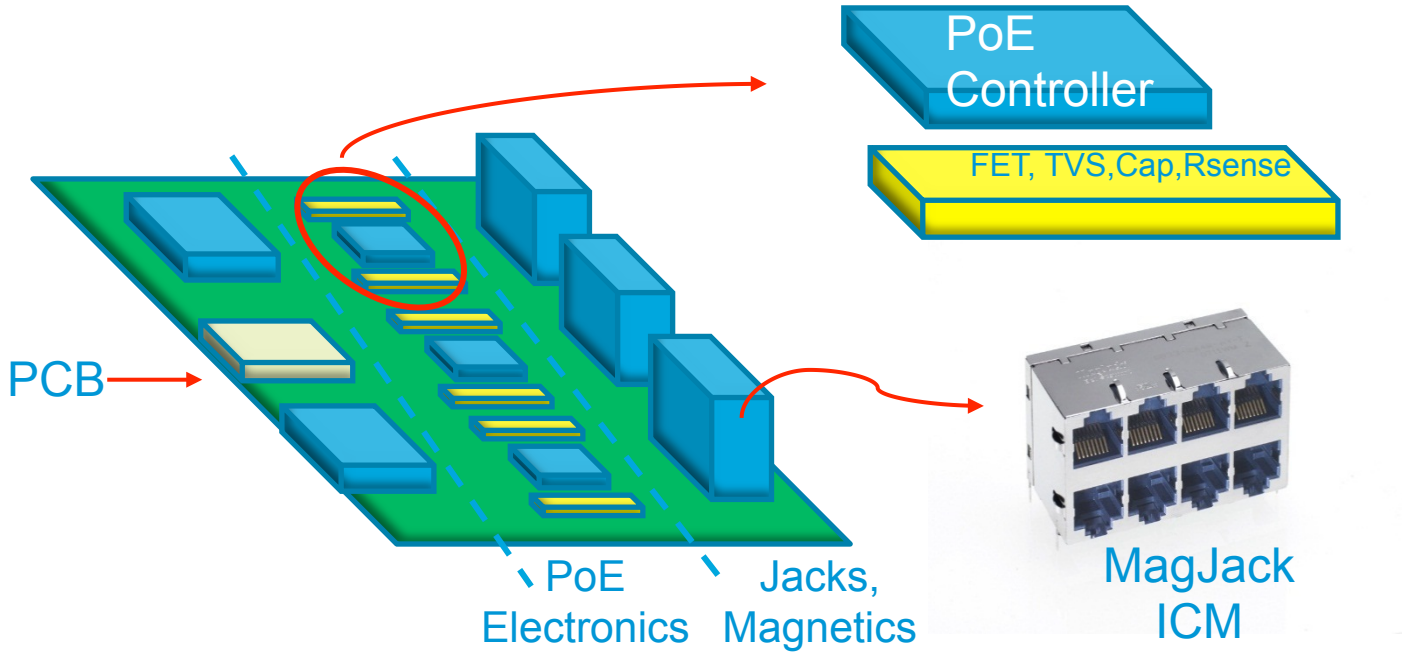
This presentation will focus on Material Cost comparisons between 1 Power Channel and 2 Power Channel implementations

PSE Material Cost – Drill Down

Material Costs

- PCB: multi-layer PCB
- Power suppl(ies)
- RJ45+Magnetics: center-tap capable transformer/injector, extra LED (optional) to indicate PoE is enabled
- Port Controller IC (power manager IC optional)
- Per-Port Discretes: FETs, Rsense, TVS, port cap
- I2C bus isolation: optocoupler or isolation IC

PSE Breakout: 24-port 4PPOE Switch Example

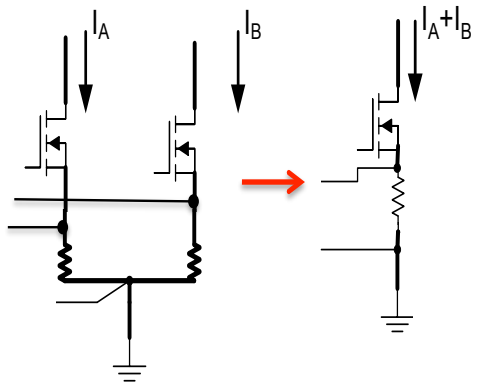


- Costs impacted by the choice of 2-Power Channel vs. 1-Power Channel architectures will be explored using a **24 Port Switch Use Case**
- The multipliers are compared to a 30W IEEE 802.3-AT base case
  - The multipliers are an estimate since actual prices and volumes vary
- The analysis includes components whose cost vary between the 2 implementations
  - Common components like Power Supply etc., are not included

PSE Breakout: Controller IC Cost Impact
External FET Solution

Solution	Cost Increase over 30W AT		Delta Between 1- and 2-Power Channel
	2-Power Channel	1-Power Channel	
External FET	2x	1.4x	-30%

- 1 Power Channel must support high accuracy ADC
  - 2x dynamic range/Higher SNR results in silicon cost increase
    - A larger dynamic range puts more stress on analog circuit design to meet accuracy requirements.
    - Could also require more complex digital circuitry.
    - Makes it more difficult to implement on low-cost mixed signal process[1].
- 2-Power Channel
  - Requires two “AT” chip ports per RJ45



[1] – Refer to Backup slides for more details

PSE Breakout: Controller IC Cost Impact
Internal FET Solution

Solution	Cost Increase over 30W AT		Delta Between 1- and 2-Power Channel
	2-Power Channel	1-Power Channel	
Integrated FET	2x	1.8x	-10%

- 1 Power Channel
  - Silicon Area Increase
    - Major contributing factor for this size increase is the FET
      - Required to keep total power dissipation at acceptable level and match power losses
- 2 Power Channel
  - Requires two “AT” ports per RJ45

PSE Breakout: Port TVS/Rsense Components Cost Impact

Component	Cost Increase over 30W AT		Delta between 1- and 2-power channel
	2-Power Channel	1-Power Channel	
TVS	2x	1x	-50%
Rsense	2x	3x	+50%

- ***TVS***: 2-power channel case requires 1 TVS per 2-pair.
- ***Rsense***: Assumes same sense resistor value (for current measurement accuracy during DC-Disconnect for existing "AT" PDs

2 POWER CHANNEL:	1 POWER CHANNEL:
Sample Power Dissipation per sense resistor: (for 60W Case) **- $P = I^2R = 0.6*0.6*0.25 = 0.09W$[1]** **- Including derating 0.25W rated sense would be good** **- Sense Resistor Size – 0805**	**Sample Power Dissipation per sense resistor: (for 60W case)** **- $P = I^2R = 1.2*1.2*0.25 = 0.36W$.** **- Including derating 1W rated sense would be good** **- Sense Resistor Size – 2512**

[1] - We are assuming a simplified model that doesn't cover unbalance.

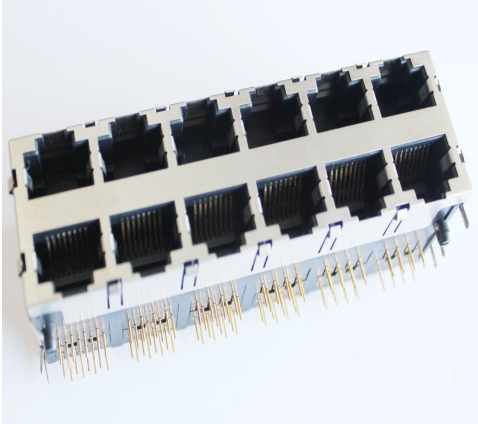
PSE Breakout: Port FET Component Cost Impact

Component	Cost Increase over 30W AT		Delta between 1- and 2-power channel
	2-Power Channel	1-Power Channel	
FET	2x	1.5x	-25%

- FET Choice is controlled by two considerations
  - Thermal Dissipation during normal operation
  - SOA (Safe Operating Area)
- Same power dissipation for 2 Power Channel and 1 Power channel assumed

2 POWER CHANNEL:	1 POWER CHANNEL:
- Current per FET = Iport/2 - Twice number of FETs per port	- Current per FET = Iport - SOA performance for 1 Power channel should support higher current compared to 2 power channel in all situations (including Short circuit) - FET die Size of 1 power channel = 2 X FET die size of 2 power channel → Cost Impact

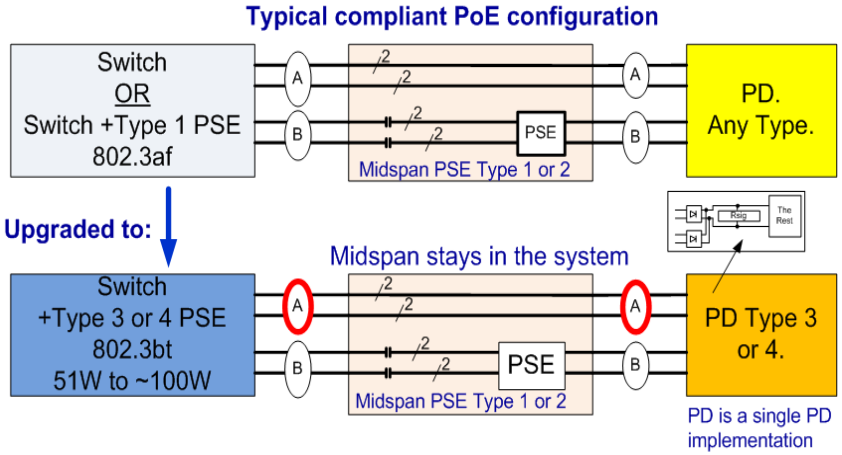
PSE Breakout: Magnetics/Jack Cost Impact



Cost Increase over 30W AT		Delta between 1- and 2-power channel
2-Power Channel	1-Power Channel	
1.15x[2]	1.35x[1,2]	27%

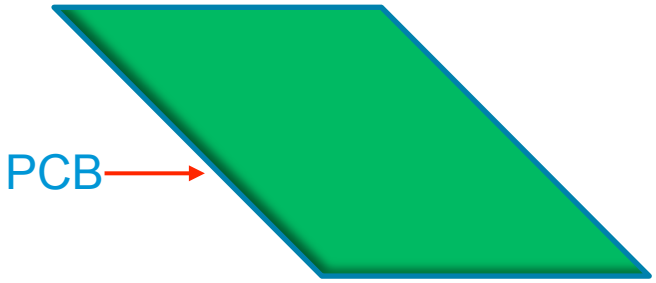
1,2 – See “Magnetics Cost Increase Notes” in backup slides for more information.

2 POWER CHANNEL:	1 POWER CHANNEL:
- Independent control over each 2pair - Worst case current per 2 Pair magnetics = Iport/2	- Has no independent control over each of the 2pair - Worst case current per 2 pair magnetics = Iport (refer to picture below) - To avoid damage, bigger Magnetics needed to handle higher current → Cost Increase



- When there is a 2-pair mid span and 4-pair end span connected to same PD:
- If end span wins the arbitration:
  - 1 power channel: all power will be provided on one 2-pair.
  - For example, if PD draws 60W → all of this is provided over 2-pair (1.2A over 2-pair Magjack as opposed to 0.6A).

PSE Breakout: PCB Cost Impact



Cost Increase over 30W AT		
2-Power Channel	1-Power Channel	**Delta between 1- and 2-power channel**
1x	1.2x	+20%

- Thermal Dissipation needs drive increased cost

  - Using the 1-power channel approach instead of the 2-power channel approach introduces additional dissipation

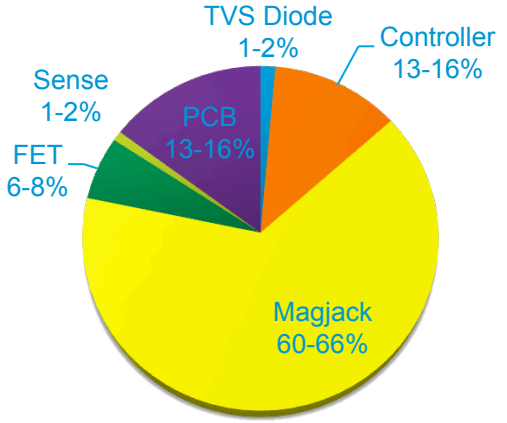
  - For a group of 24 ports operating at high power (60W PSE output):
    - 1-Power channel has 2X dissipation compared to 2-Power channel
      - Since the Rsense choice is same between 2-Power and 1-Power channel to provide accuracy
    - Multiple GND planes, thicker copper (ex: 2 ounces) per layer.
    - Larger board area is needed for same number of ports.
    - Maximum number of high power ports per unit of PCB area is lower

PSE System Comparison: Component Cost Weighting

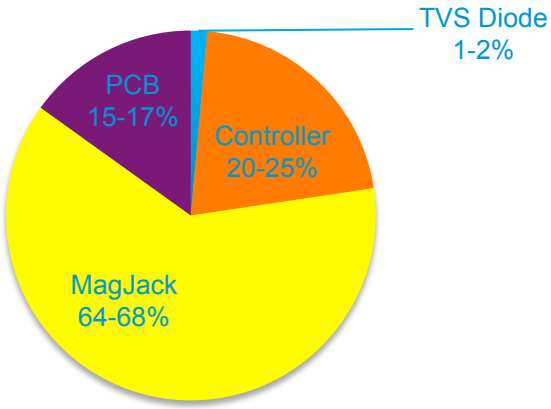
- Not all components contribute equally towards system cost
- Contribution in a typical base system of 2Pair 30W is shown
  - These percentages were taken from a variety of sources and vendors; thus ranges are given for each component

Component	Contribution in 30W 2-Pair External FET solution	Contribution in 30W 2-Pair Internal FET Solution
Sense	1-2%	NA
FET	7-9%	NA
TVS diode	1-2%	1-2%
Controller	13-16%	20-25%
PCB	13-16%	15-17%
Magjack	60-66%	64-68%

Component Contribution – External FET



Component Contribution - Internal FET



- The minimum of the component contributions are used along with the multipliers shown in slides 8-13 to arrive at the total system comparison between 1-power and 2-power channel

PSE Breakout: Cost Comparison Summary
External FET Solution

- Taking into consideration the weighting of the various components, the data shows that when building a 60W system using external FETs:

The 2-Power Channel architecture is approximately 2% less costly than the 1-Power Channel architecture.

$$\Delta = 1 - 1 + Dual\ Power\ Channel\ Cost\ Increase / 1 + Single\ Power\ Channel\ Cost\ Increase = 1 - 1 + 0.34 / 1 + 0.37 = 0.02$$

		Dual Power Channel		Single Power Channel	
Component	**Weighting**	**Increase over AT***	**Effective Contribution**	**Increase over AT***	**Effective Contribution**
Magjack	61.0%	15.0%	9.15%	35.0%	21.35%
PCB	14.0%	0.0%	0.00%	20.0%	2.80%
PoE Controller	14.0%	100.0%	14.00%	40.0%	5.60%
FET	8.0%	100.0%	8.00%	50.0%	4.00%
Sense Resistor	1.5%	100.0%	1.50%	200.0%	3.00%
TVS Diode	1.5%	100.0%	1.50%	0.0%	0.00%
Total Cost Increase			34.15%		36.75%

* Cost increase indicated is for a 60W system compared to a 30W AT system.

PSE Breakout: Cost Comparison Summary
Internal FET Solution

- Taking into consideration the weighting of the various components, the data shows that when building a 60W system using external FETs:

The 2-Power Channel architecture is approximately 7% less costly than the 1-Power Channel architecture.

$$\Delta = 1 - 1 + Dual\ Power\ Channel\ Cost\ Increase / 1 + Single\ Power\ Channel\ Cost\ Increase = 1 - 1 + 0.31 / 1 + 0.41 = 0.07$$

		Dual Power Channel		Single Power Channel	
Component	**Weighting**	**Increase over AT***	**Effective Contribution**	**Increase over AT***	**Effective Contribution**
Magjack	64.0%	15.0%	9.60%	35.0%	22.40%
PCB	15.0%	0.0%	0.00%	20.0%	3.00%
PoE Controller	20.0%	100.0%	20.00%	80.0%	16.00%
TVS Diode	1.0%	100.0%	1.00%	0.0%	0.00%
Total Cost Increase			30.60%		41.40%

* Cost increase indicated is for a 60W system compared to a 30W AT system.

Further Cost Considerations

- The numbers reported in this presentation are very conservative and the cost advantage of the 2-power channel architecture is probably greater than shown here.
- In addition, these factors have not been included in the previous analysis:

  2-Power Channel

  - The indirect savings that come from lower power dissipation (sense resistor, slide 6)
  - There is volume advantage as it can use parts available today

  1- Power channel

  - Includes only PSE side magjack cost increase
    - PD side will also need larger jack magnetics leading to increased cost
  - Cost increase for 100W case will be more and non linear increase vs. 60W case

Summary

- Magnetics are the main contribution to system cost (more than 60%)
  - 1-Power channel approach's magnetics are 20% higher than 2-Power channel
  - PoE controller cost contribution is much less than magnetics contribution
- Conclusion:
  - The data in this presentation affirms, 2-power channel is not twice as costly as 1 power channel. The costs are very comparable and in some cases that 2 Power channel implementations are less costly than 1 Power channel implementations

Backup

19

Magnetics Cost Increase Notes

- Note 1:

  This is an extremely conservative number for the following reasons:

  - Assumes bigger magnetics only on ALT- A pair in order to handle the midspan case.
  - Cost will increase even more if normal wire faults are considered where ALT-A or ALT-B both could be carrying full port current.
  - This increase is the cost associated with preventing damage to the magnetics (not ensuring operation).
  - The above cost increase is for 60W. Cost increase as we move to 100W will not be linear.
  - In addition, this does not include cost increase due to PD side magnetics.

- Note 2:

  Bringing out the extra center-taps drives a cost increase for both 1-power channel and 2-power channel implementations.

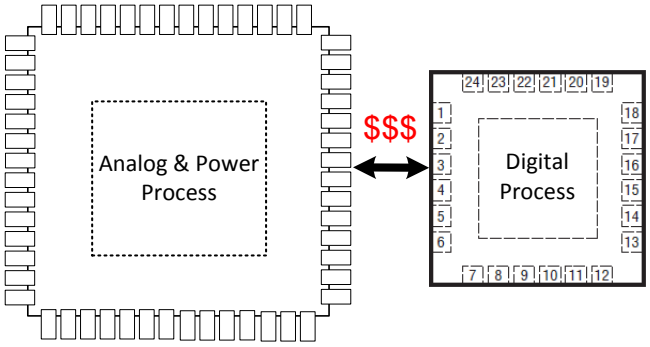
Impact of Doubling the Current Sensing Dynamic Range Beyond what is done Today

- Solutions could be:

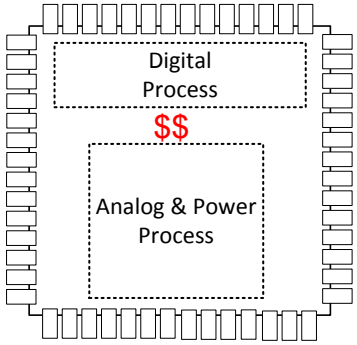
  Use 2 separate chips (maybe 2 separate devices) and different silicon process (each one optimized for analog or digital), which means much higher cost.

  If single-chip solution: use a different process and/or larger/more expensive die to meet analog accuracy requirement.

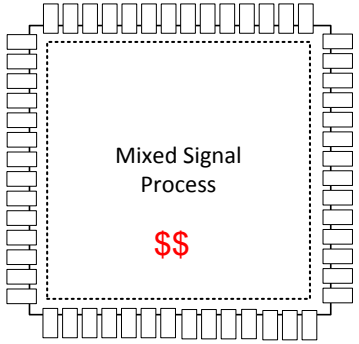
- In all cases, there will be significant cost increase.
- Also consider that some manufacturers have capability to do multi-chip while others don't, or can do it at much higher costs.



Chipset solution



Multichip solution



Integrated solution

PSE Breakout: Cost Comparison Summary
External FET Solution[1]

Component	Cost Increase of a 60W system compared to an AT 30W system		Reasons for Cost Increase compared to 30W IEEE802.3AT system
	2-Power Channel	1-Power Channel	
TVS diode	100%	0%	2 Power Channel : Twice number of Diodes
PoE Controller	100.00%	30-50%	2 Power Channel: Twice number of chips 1 Power Channel: Silicon Area increase
Magjack	15.00%	30-40%	2 Power Channel: Extra center tap access 1 Power Channel: Extra center tap access + bigger Magjack capable of carrying all current in one 2pair[2]
FET	100.00%	50.00%	2 Power Channel: Twice number of FETs 1 Power Channel: Bigger FET to carry all current
Sense	100.00%	200.00%	2 Power Channel: Twice number of resistors 1 Power Channel: Bigger Sense Resistor – 4X Power rating compared to 2 Power channel
PCB	0.00%	20.00%	1 Power channel: More thermal relief needed due to increased dissipation

[1] For 2 power channel solution, there is a volume advantage as it can use parts available today – The above table does not reflect this additional cost benefit

[2] Includes only PSE side magjack cost increase. Note PD side will also need bigger magjack → More cost
Shows only 60W case – Cost increase for 100W case will be more and non linear increase
Assumes bigger magnetics only on ALT- A pair → to handle the midspan case
Cost will increase even more if normal wire faults are considered where ALT-A or ALT-B both could be carrying full port current

PSE Breakout: Cost Comparison Summary
Internal FET Solution[1]

Component	Cost Increase of a 60W system compared to an AT 30W system		Reasons for Cost Increase compared to 30W IEEE802.3AT system
	2-Power Channel	1-Power Channel	
TVS diode	100.00%	0%	2 Power Channel : Twice number of Diodes
PoE Controller	100.00%	80%	2 Power Channel: Twice number of chips 1 Power Channel: Silicon area increase
Magjack	15.00%	30-40%	2 Power Channel: Extra center tap access 1 Power Channel: Extra center tap access + bigger Magjack capable of carrying all current in one 2pair[2]
PCB	0%	20.00%	1 Power channel: More thermal relief needed due to increased dissipation

[1] For 2 power channel solution, there is a volume advantage as it can use parts available today – The above table doesn't include this cost benefit

[2] Includes only PSE side magjack cost increase. Note PD side will also need bigger magjack → More cost Shows only 60W case – Cost increase for 100W case will be more and non linear increase

Discrete Magnetics – External FET

Component	Weighting	2- Power Channel		1-Power Channel	
		Increase over AT	Effective contribution	Increase over AT	Effective Contribution
Discrete magnetics	50%	15%	7.5%	35%	17.5%
PCB	21%	0%	0%	20%	4.2%
PoE Controller	17%	100%	17%	40%	6.8%
FET	8%	100%	8%	50%	4%
Sense Resistor	2%	100%	2%	200%	4%
TVS diode	2%	100%	2%	0%	0%
TOTAL COST INCREASE			36.5%		36.5%

Discrete Magnetics – Internal FET

Component	Weighting	2- Power Channel		1-Power Channel	
		Increase over AT	Effective contribution	Increase over AT	Effective Contribution
Discrete magnetics	53%	15%	7.95%	35%	18.55%
PCB	24%	0%	0%	20%	4.2%
PoE Controller	21%	100%	24%	80%	19.20%
TVS diode	2%	100%	2%	0%	0%
TOTAL COST INCREASE			33.95%		41.95%