An Optimum Approach to Apply DC Disconnect

System Efficiency, Accuracy and Thermal Considerations

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Working Premises

The motivation of this work is to analyze DC-Disconnect to outline impact on

- System Efficiency, that includes
  - PSE Dissipation
  - Cable Dissipation
- Thermal impact on PSE internal circuitry
- Current Measurement Accuracy

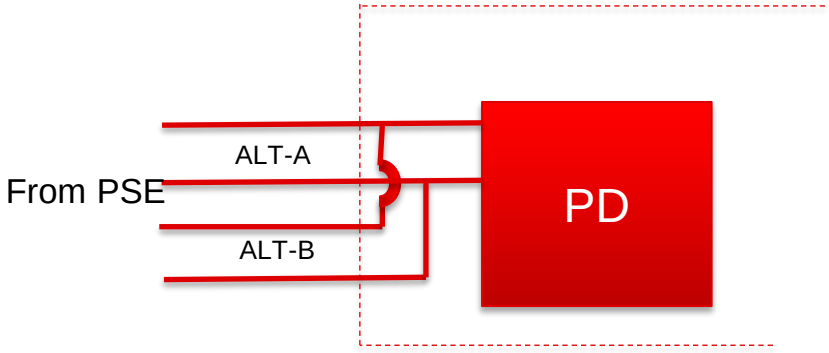
The above are analyzed as applicable to the following cases:

- “bt” PD interface
- Backwards compatibility

DC-disconnect as applicable to “bt” PDs

- We need to maintain the accuracy in disconnect sensing.
- Hence, for the “bt” PD, DC disconnect threshold should be doubled (7.5 +/- 2.5mA $\Rightarrow$ 15 +/- 5mA) to support multiple implementations.
  - DC disconnect based on sum of currents ($I_A + I_B$)
  - Shorter MPS duty-cycle to reduce standby system consumption
  - Depending on implementation, also able to detect if one pair set has been disconnected while the other one is still providing power.

DC Disconnect as applicable to single “AT” PD interface



- If “bt” PSE is connected to single “at” (Type 1 or 2) PD interface:
  - DC disconnect threshold **CANNOT** change → defined in IEEE spec: 5-10mA
- There are different approaches towards meeting the above
  - Approach #1: Drive 4P all the time.
  - Approach #2 (Best): Mix and Match

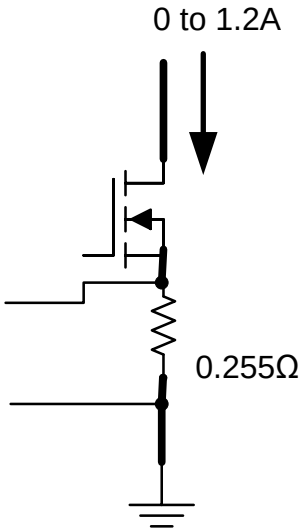
4P Power Savings

- To proceed with the comparison of the two approaches, we use the example of 48 port switch configured as following:
  - 36 ports connected to low power PDs
  - 12 ports connected to high power PDs
- In the CFI (http://www.ieee802.org/3/4PPOE/public/mar13/index.html), it was demonstrated how 4P is more efficient than 2P even for <25.5W PDs. For system above, the savings from running the low power ports over 4P is shown below.

System Assumptions		Value	Units
Cable length		40	m
Link Resistance		0.125	Ohm/m
Number of low power Ports (assumption)		36	
Voltage at PSE output		50	V
Example #1			
Average PD Input Power		8	W
Average PSE output power if 2P		8.13	W
Cable savings in going to 4P for low power ports	per port	0.066	W
	all low power ports	2.36	

Approach # 1 – Drive 4P All the Time

- If “bt” PSE is connected to a single “at” PD interface:
  - DC disconnect threshold **CANNOT** change
    - ⇒ is same as defined in “at” spec: 5-10 mA
    - ⇒ **this mandates a “sense” resistor value** (0.255 Ohms [1]) otherwise the accuracy of DC-Disconnect measurement will go down.
- System power loss in high power (>25.5W PD or >30W PSE) cases will be the drawback



A 1-power channel configuration drives all pairs at the same time.

This limitation is due to its architecture.

Note 1: Lowest in industry sense resistor value used by PSE controllers working with external MOSFET is 0.255 Ohm.

Approach # 1 – Drive 4P All the Time
Additional System loss from High Power ports

1-Power Channel System Parameters		Value	Units
Number of High Power PSE Ports (53.9W) [1]		12	Port
Voltage at PSE output		50	V
Rsense		0.25	Ohm
1-Power Channel			
Current per switch		1.08	A
PSE Power loss (due to Rsense only)	per “53.9W” PSE output Port [1,2]	0.296	W
	all “53.9W” PSE output Ports [1,2]	**3.56**	

Note 1: PSE with 53.9W output corresponds to PD with 51W input 40m cable length.
Note 2: If **60W PSE** output, the Rsense **loss becomes 0.3672 W each**, which means **4.406W** for 12 ports.

Approach # 1 – Drive 4P All the Time
Additional System loss from High Power ports

Approach #1 Summary:

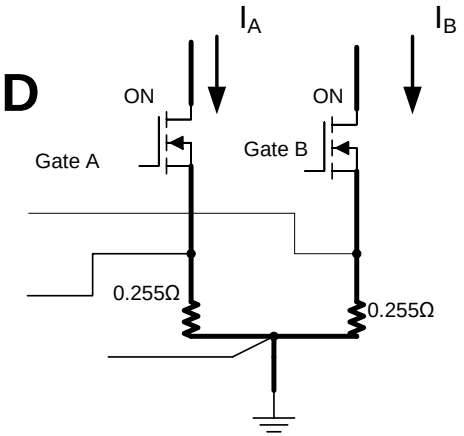
- The 4P efficiency savings are lost by excess power dissipation on the sense resistor.
  - The concept of **4P power savings is lost**.
  - The extra dissipation is concentrated inside the PSE, leading to **potential severe thermal** issues.
- Ways to counter act this include:
  - Reduced accuracy in DC-Disconnect
  - Increased System cost
  - Or Use approach #2

Approach #2 Mix and Match

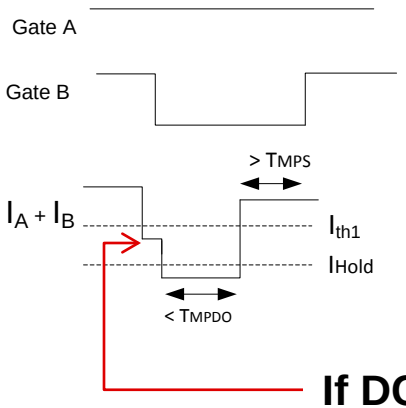
- **Methodology:**
  - Drive 4P if “bt” PD
  - If “at” PD:
    - Drive 4P, then if DC disconnect is “suspected” [1], turn off 2nd switch and do DC disconnect check with 1st switch (I_A).
    - If the test indicates there is no disconnect, or if the current goes back up for some time, turn back ON 2nd switch.
    - This will provide Higher accuracy due to higher signal amplitude in sensing element.
- This method combines <u>all the positive</u> system aspects

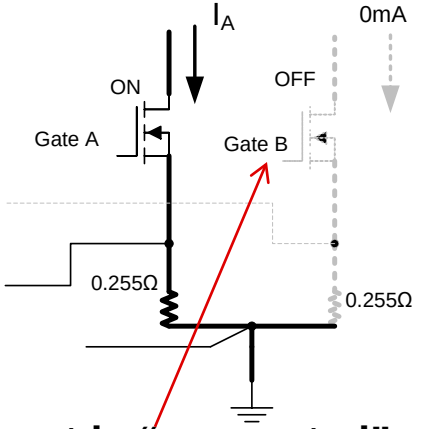
Note 1: DC disconnect “suspected” means (I_A + I_B) < 1st arbitrarily defined threshold.

If “at”PD



If regular “at” load current





If DC disconnect is “suspected”

Approach #2 Mix and Match

2-Power Channel System Parameters		Value	Units
Number of High Power PSE Ports (53.9W)		12	Port
Voltage at PSE output		50	V
Rsense		0.255	Ohm
2-Power Channel	**Approach #2**		
Current per switch		540	mA
PSE Power loss (due to Rsense only) [1]	per “53.9W” PSE Port [2]	0.148	W
	all “53.9W” PSE Ports [2]	**1.78**	
Overall System Efficiency, Comparison with 1-Power Channel			
Extra Power Loss on Rsense from the 12 High Power PSE Ports if with 1-Power Channel [1,2]		1.78	W
Cable savings in going to 4P for low power ports if 36 x 8W PDs		2.36	W

With 1-Power Channel, the **4P efficiency savings are lost** by excess power dissipation on the sense resistor.

Note 1: FET losses assumed to be the same, a **larger (expensive) FET will be needed** for the 1-Power channel configuration to compensate for 2x the current and higher junction temperature.
Note 2: PSE with 53.9W output corresponds to PD with 51W input if 40m cable length.

Approach #2 Mix and Match

Approach #2 Summary:

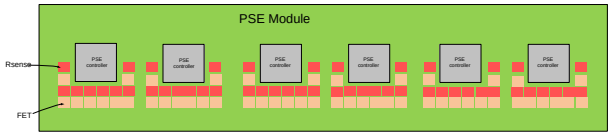
- This method combines:
  - High sensing accuracy.
  - Low PSE internal dissipation
    - Maximizing the savings from the use of 4P distribution.
    - Simplifying thermal design, lower costs.
  - Both of them already achieved with technologies and implementations used today
- AND it also provides improved cable efficiency for low power ports by using 4P distribution.
- This approach is not possible with single switch configuration.

Thermal Analysis Discussion

- System-level thermal analysis has been conducted to verify the feasibility and limitations of implementing multiple 4P higher power (**60W**) ports while using the 1-power channel architecture.
  - Comparisons were done with a 2-power channel architecture (case A).
- The system parameters were:
  - Generic system model, operating at 55C ambient.
  - With PSE controllers card (PCB Size = 6.8” x 1.15”) inside an enclosure with forced air convection.
  - 0.255 ohm Rsense per power channel.

SIM Case	# HP Ports [1] (1.2A)		Description	FET Rdson @25°C	Rsense Physical size
	Total	per controller		Normalized (unit)	
A	24	4	2 power channel	1	1x
B	24	4	1 power channel, “bigger” FET and Rsense	0.5	3.5x
C	48	8	1 power channel, “bigger” FET and Rsense	0.4	3.5x

Note 1: High Power Ports



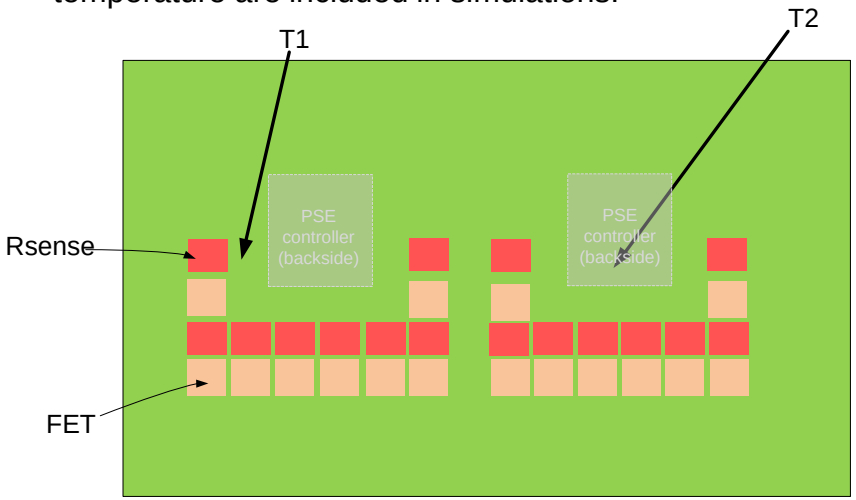
Thermal Analysis – Simulation Results

SIM Case	# HP Ports	Description	FET	PCB T1	PCB T2
A	24	2 power channel	94 °C	90 °C	92 °C
B	24	1 power channel, “bigger” FET (2x) [1]	108 °C	97 °C	103 °C
C	48	1 power channel, “bigger” FET (2.5x) [1]	146 °C	132 °C	131 °C

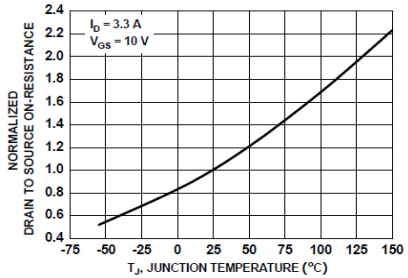
Ambient outside of the enclosure : 55°C

Note: these simulations are only for comparison purposes. Also, simplified models were used for the analysis.

Note 1: Impact on FET dissipation of Rdson variation over junction temperature are included in simulations.



Typical FET Rdson vs T_J



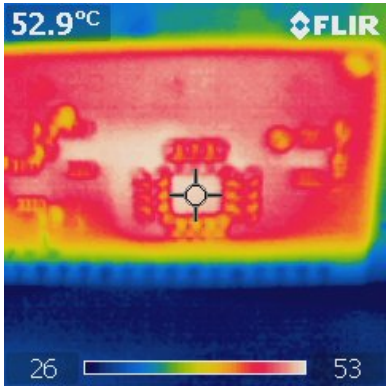
Implementing a high number of High Power ports with 1-power channel approach results in thermal issues.

Thermal Test Results

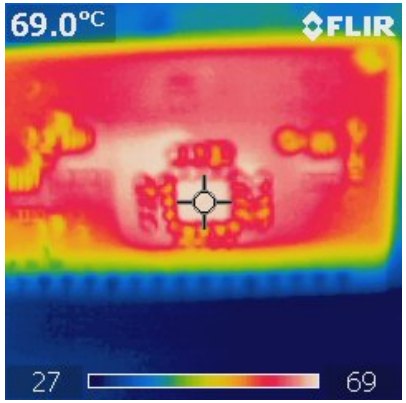
- Tests have been conducted to validate the limitations of implementing multiple 4P higher power (**60W**) ports while using the 1-power channel architecture.
- The system parameters were:
  - Operating free air at ~25°C ambient.
  - With 4-layer (2oz copper) 8-Power Channel PSE daughter card.

Test Case	# HP Ports [1]	Description	PCB	Free air	Temp Elevation
A	4	2 power channel	53 °C	~23 °C	~30 °C
B	4	1 power channel, “bigger” FET (2x)	69 °C	~23 °C	~46 °C
C	8	1 power channel, “bigger” FET (2x)	91 °C	~23 °C	~68 °C

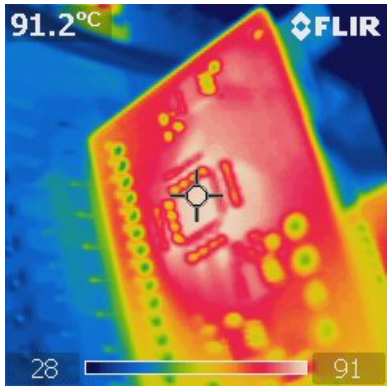
Note 1: High Power Ports



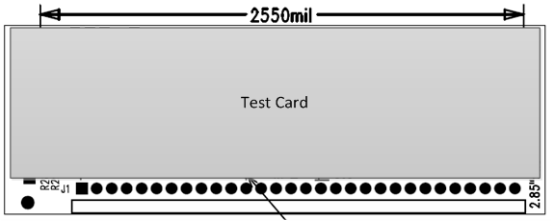
Case A



Case B



Case C



A vs B: Temp elevation of 2sw approach is < **66%** of 1sw approach.

Thermal Analysis – Summary

- Implementing a high number of High Power ports with 1-power channel approach greatly complicates the thermal design and increases costs.
  - More PCB copper (# layers and thickness) for better heat spread.
  - Larger board for better board convection/radiation.
  - If fanless system, more thermal contacts from board to chassis.

- The table below summarizes the impact of the thermal limitations of 1-power channel approach on system design:

	Dual Power Channel	Single Power Channel
Maximum Number of **HP Ports/inch^2 of PCB**	Higher	Lower
Maximum Number of **HP Ports/Controller** on a High Port Density Card	Medium	Medium-Low

DC Disconnect Method – Comparison Summary

PD Configuration	Dual Power Channel Approach #2	Single Power Channel Approach #1
“bt” PD Interface	Supported	Supported
	Can detect if one 2-pair set is individually disconnected	Cannot detect that only one 2-pair set is disconnected
“bt” PD Interface, High Power PDs	Simple thermal design	Thermal issues, complex thermal design
Single “at” PD Interface	High accuracy	Highest PSE dissipation & temperature and system cost and/or Highest IC + PCB cost
	Lowest PSE dissipation & temperature	
	Lowest system cost	
	Highest system efficiency	Medium-Low system efficiency