

Connection Check: Baseline Text

David Abramson

Texas Instruments

IEEE802.3bt Task Force

March 2015

History of the “Connection Check”

- The connection check was originally introduced as a method for PSEs to determine if they were connected to a single PD interface or dual PD interfaces.
- Multiple methods for implementing the connection check have been presented. See:
 - http://www.ieee802.org/3/bt/public/nov14/Lukacs_01_1114.pdf
 - http://www.ieee802.org/3/bt/public/nov14/darshan_10_0914.pdf
 - http://www.ieee802.org/3/bt/public/sep14/dwelley_01_0914.pdf
- The purpose of this presentation is to present baseline text for the connection check.
- **This presentation specifically does not address 4-Pair ID and whether connection check is sufficient to apply 4-pair power.**

Connection Check: Electrical Specifications

- As the connection check will be performed before the PSE has determined if the PD has a valid or invalid signature, the PSE should use the same electrical specifications as though used for detection.
 - Specifically, the open circuit voltage and short circuit current defined for detection should be followed as these specifications were developed in order not to damage devices that do not want to receive PoE power.
 - In addition, for results to be consistent, only tests that result in voltages in the valid test voltage range should be used.
 - As we are not defining the exact method used, the voltage difference for a multi-point test (item 4 in Table 33-4) and the slew rate (item 5 in Table 33-4) are not applicable.

Table 33–4—PSE PI detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state only
2	Short circuit current	I_{sc}	A		0.005	In detection state only
3	Valid test voltage	V_{valid}	V	2.80	10.0	—

Connection Check: Timing Requirements

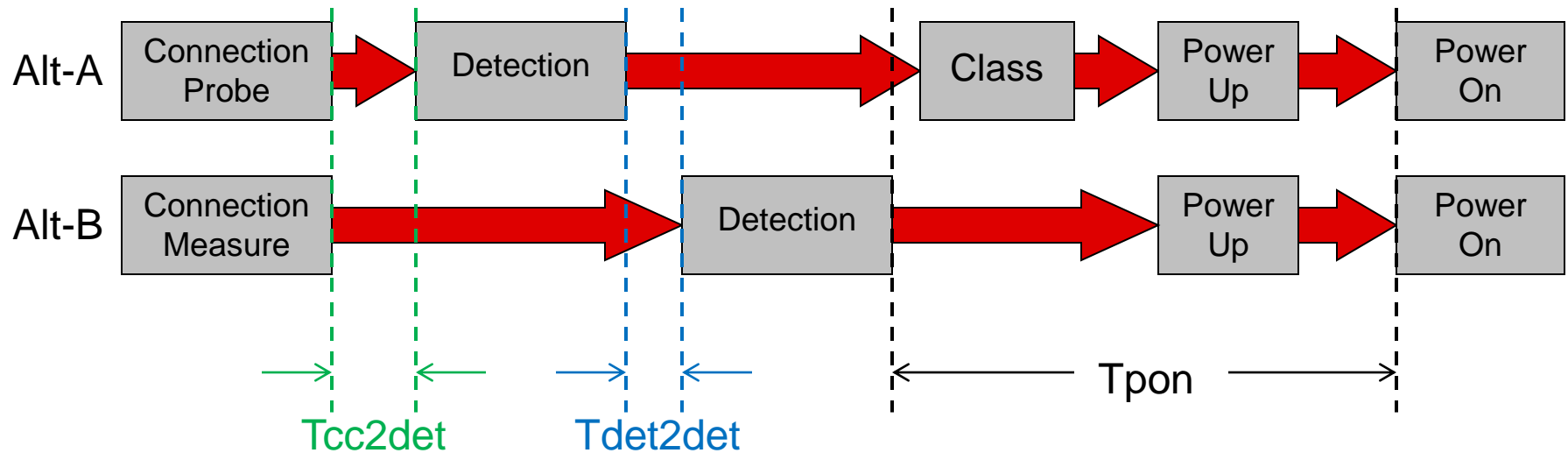
- The goal of the timing requirements for the connection check (and rest of the powering procedure) are to not allow gaps of greater than 400ms where a cable could be unplugged and another cable plugged in without the PSE recognizing it.
 - The Tpon requirement makes sure that a PD is powered within this 400ms limit from the end of detection.
 - There is now information gained during the connection check (as well as independent detections on each pair set) that must be “maintained” until the PD is powered.
 - “Maintained” means that we must ensure the load is not switched without the PSE restarting the connection check/detection/power up procedure.

More Timing/Transition Requirements

- If the connection check is performed after detection, it must be fast enough to squeeze into T_{pon} along with class and power up (inrush).
- If the connection check is performed as part of detection, it will be included in the T_{det} timing requirements.
- If the connection check is performed before detection, we will need to add a new timing requirement to ensure gaps of more than 400ms are not created.
- If the connection check is performed before (or during) detection, it must not result in the PD presenting an invalid signature.
 - If the connection check causes the PD voltage to raise into the class range and return to a lower voltage (in the V_{valid} range), Type 2, Type 3, and Type 4 PDs will transition to mark and present invalid signatures.
 - If the voltage is brought below the reset threshold between the connection check and detection, this PD would transition back into detection and present a valid signature.

Connection Check Timing: An Example

4PPoE PSE Connected to 4PPoE PD with Single PD Interface



- Tpon: Ensures cable is not switched between end of detection and power on.
- Tcc2det: Ensures cable is not switched between end of connection check and beginning of detection.
 - Possible wording to allow flexibility: “The end of the connection check shall be no more than 400ms before the beginning of detection.”
- Tdet2det: Ensures cable is not switched between end of first detection and beginning of 2nd detection.
 - Possible wording to allow flexibility: “There shall be no more than 400ms from the end of the detection on first pair-set to the beginning of detection on the other pair-set.”

Connection Check Baseline Text

33.2.5.X Connection Check Requirements

Type 3 and Type 4 PSEs that operate over both pair sets shall complete a connection check prior to the detection of a PD as specified in clause 33.2.5. The purpose of the connection check is to determine the architecture of the PD connected to the PSE PI, specifically the PSE shall determine if it is connected to a single PD interface or a dual PD interface. See Annex 33TBD for more information about the connection check.

Editor's Note: Definitions of single PD interface and dual PD interface need to be added or text needs to be cleaned up when final terminology is decided.

While the exact method of the connection check is left to the implementer, the PSE shall meet the specifications for open circuit voltage and short circuit current in Table 33-4. In addition, only tests that result in a voltage at the PSE PI that is within the V_{valid} voltage range as specified in Table 33-4 shall be used to determine the architecture of the PD.

Timing requirements TBD.

Summary

- The connection check should use the same electrical parameters as those defined for detection.
- Some options for the timing requirements for the connection check have been presented but need to be carefully considered.
- Baseline text has been presented that leaves the method of the check implementation independent and makes the timing requirements TBD.
- I will move to adopt this baseline text as part of the “motion madness” session during this meeting.