Power Matters

IEEE802.3bt 4-Pair Power over Ethernet Task Force

DC disconnect (MPS) baseline proposal principles

Rev 006a

March 2015

Yair Darshan
Microsemi
ydarshan@microsemi.com

Objectives

- Review main results of Diode Vdiff effect on:
  - E2EP2PRunb at low current Affects DC Disconnect (MPS) requirements
  - E2EP2PRunb at high current – Affects maximum pair current and the whole E2EP2PRunb system equation behavior.
  - See details: http://www.ieee802.org/3/bt/public/jan15/darshan_02_0115.pdf
- Review latest discussions
  - Proposing DC Disconnect Baseline principles

Maximum realistic Vdiff at low current

Vdiff max. [mV]	Notes
120 - 150	Probability =~0 to happen on the same pairs of the same polarity at the same time.
60	*Possible to happen. System results >10K sample*
10	66% of the diodes of same part number and same manufacturer.
Vdiff as function of temperature:Tdiff <1°C with uniform temperature source. Tdiff <6°C with nonrealistic diode assembly and with narrow heat source on one diode.	

- **Conclusions**
- Type 1, Type 2 and Type 3 Class 0-4: Sane behavior in term of unbalance.
  - Vdiff max at low current: 60mV (E2EP2PRunb= 75% at MPS levels)
  - This number is applicable to high current as well to limit pair Imax. E2EP2PRUNB<31%
  - No evidence for higher PSE+PD Vdiff=60mV in real systems in very large samples
  - Temperature Tdiff effect: reasonable to handle with typical PCB thermal design.

Conclusions from last meeting

- Two solution options were proposed
  - To have minimum guaranteed current of 5.5mA over each 2P requires Vdiff≤34mV.
  - 7mA guaranteed over each 2P require < 34mV.
    - See slide 20 at: http://www.ieee802.org/3/bt/public/jan15/darshan_02_0115.pdf
- January 2015 room feedback: prefer specifying minimum guaranteed current over 2P instead of specifying low Vdiff ≤34mV.
- 4 possible solutions in PSE side was proposed to address MPS unbalance of PD.
  - Summing the currents and apply MPS rules
  - If after connection check, result is single load PD, apply MPS rules on the pair with higher current. 2nd pair just to check I>0 (not open load case) or ignore (TBD)
  - Independent MPS capability per 2P (5.5mA(or 7mA)/2Pair guaranteed in the PD.
  - To disconnect one of the 2P and check MPS.
- The idea is to generate the wording that will allow all possible PSE solution for maximum PSE vendor design flexibility based on his PSE architecture.

Latest discussions -1

- **Claim:**
- (a) If Type 3 PSE need to support Type 1 / 2 PD with total 10mA MPS THEN (b) Type 3 PSE CONNECTED TO Type 3P class 0-4 (same Type 1 and 2 power levels) will have to work with total MPS=10mA and apply MPS rules of Type 1 / 2
- This is backward compatibility based argument since we can't tell the difference between the above two PDs (They have the same class. See Annex L.)

- **Discussion**
- This claim make sense but ignores long term system considerations:
- 10mA total MPS for Type 3 PDs with class 0-4: may be OK.
- We can do better in term of complete spec and preventing future undefined behavior:
  - Type 3 PD for any class, P2P current unbalance need to be limited and not left undefined. 75% max (=60mV PD Vdiff) is what we get for existing Type 1 and 2 in the field with typical diodes that we are using.
    - We can't allow zero current on one pair and max current on 2nd pair. It will prevent detection of open load/open wire etc. if we want to do it.

Latest discussions -2

- It is also recommended to consider keeping PD Type 3 class 0-4 total current 22mA to improve PSE ability have better cost effective solutions (it allows 2mA minimum current which is >1mA which is PoE systems cost effective noise floor.
  - (Yes, we need to address 10mA total anyway so why to bother? See FAQ)
  - Does' it requires different thresholds in PSE? To be discussed.

- **Claim: Using 4 class events to change Type 3 PSE thresholds and PD MPS**
  - PD MPS is changed from 7mA/2P min if PSE class event is >4 or total 10mA if PSE class event is <=4
  - Pule timing capability can be identified
  - PSE MPS thresholds is changing from 5-10mA to 2-7mA accordingly.
- **Discussion:**
  - Make sense to use lass event number to detect MPS capability (amplitude and timing.)
  - Consider to unify PSE MPS thresholds to 2mA-7mA for all Type 3, 4 class 0-7 for simple specification.
  - Reducing Ihold_min to 2mA for all Type 3, Type 4 use cases due to unbalance.
  - Consider to increase MPS in Type 3 class 0-4 from 10mA to 22mA for better current detection

DC disconnect (MPS) baseline proposal principles

- Why discussing principles before suggesting baseline text?
- DC disconnect is critical function
  - DC disconnect for 4 pairs is more complex issue than it was for 802.3at
  - High unbalance at low current (75% max, 1.25mA,8.75mA for total 10mA)
  - Type 3 and 4 PSE need to work with Type 1 and 2 PDs with 10mA total MPS.
  - Single interface PD
  - Dual Interface PD
- As a result, we need to identify different use cases and agree on the requirements for PSE and PD side and then, and only then start to create the baseline text.
- PSE Has to have several solutions for addressing MPS at 75% unbalance
- Otherwise we miss use cases and create holes in the standard.

PD DC Maintain Power Signature - Table 33–TBD

Item	Parameter	Symbol	Units	Min	Max	PD Type	Current 2P/4P	Conditions
1	Input current	I_{Port_MPS}	A	0.01		1,2	Total 4P	
2				0.01		1,2,3,4	Per 2P	Dual Signature PD
3				0.01		3-4	Total 4P	1. Class 0-4. 2. If # of class event <4
				0.0075		3, 4	Per 2P	1. Class 5-8 2. If # of class event ≥4 3. Tested with PSE Vdiff=2mV.
4	PD maintain power signature time	T_{MPS_PD}	ms	75		1, 2	-	
						3, 4	-	If no long first class event
				7		3, 4	-	If long first class event (T_{LCF})
5	PD dropout period	T_{MPDO_PD}	ms		250	1, 2	-	
						3, 4	-	If no long first class event
					318	3, 4	-	If long first class event (T_{LCF})

1. We will add test conditions. First we need to agree on the concept.
2. If I meet this test conditions, We need to be certain that the PD and link segment will not be disconnected

(xx Dave it force implementation ….Prefer: if single interface then sum total 10mA (all single interface) and at least 2.75mA per pair.)

PSE DC Maintain Power Signature - Table 33–TBD

Item	Parameter	Symbol	Units	Min	Max	PSE Type	2P/4P	Conditions
1	DC MPS current	I_{Hold}	A	0.005	0.01	1, 2	One 2P only	
				0.002	0.007	3,4	Per 2P.	Dual PD configuration
				0.005	0.01[a]	3, 4	Total 4P[a]	PD class 0-4.
				0.002	0.007[a]		If connection check=single interface then The highest 2P current and TBD on the 2nd	
				0.002	0.007	3, 4	per 2P each	PD class 5-8, at least 4 class events .
				0.002	0.014		Total 4P	
				0.002	0.007		If connection check=single interface then The highest 2P current and TBD on the 2nd	
				0.002	TBD		Any other solution TBD.	

- Main point: Do we want or need to check the current at the pair with minimum current? If not we don't have an issue.
- Power demotion issue: Lennart, Christian
- Dave Ab. Wwhat if it is balance the new may disconnect with the hight threshold. To verify.
- For Type 3 and 4: Min value must be lower than old value due to unbalance: 2mA min.
- a= could be other implementations that may need to bee addressed
  For simplicity: Consider to unify if possible, all ranges to 2-7mA.

Discussions

FAQ-1

- Q:Vdiff=60mV is maximum real case (E2EP2PRUNB=75%) IN Type 1,2 PDs when connected to Type 3 PSEs and will be the same for Type 3 PDs class 0-4 if using the same diodes in the market today, however theoretically it can be 120mV etc. How we guarantee system will work with existing diodes.
- A:
- (1) The probability to 120mV on the same pair, on the same box at the same time of production while we know (conditional probability effect) 60mV is maximum realistic than the probability is well below 10^-11.
- (2) Thousands of systems were check and for 10mA total MPS it was found that worst case unbalance was 1.25mA, and 8.75mA which is 75% maximum P2P unbalance which is equivalent to 60mV system Vdiff. Due to the fact that at low current and short cable only PSE Vdiff and PD Vdiff affects the P2P Unbalance and PSE Vdiff=~0 at those systems, then PD Vdiff=60mV. See curves in http://www.ieee802.org/3/bt/public/jan15/darshan_02_0115.pdf
- (3) The are many specifications component related factors that are not defined at 100% certainty or defined at all but yet counting on our measurements, experience and some common sense, we can guarantee interoperability and compatibility.
- (4) We also cant guarantee operation below 3m cable for data integrity since TIA model was 3m for meeting Return Loss as an example.
- (5) We cant also guarantee that diode leakage is less than 10uA to allow detection function and yet the datasheet guarantees leakage current 1mA max….and it was never been a reason to do detection with >>1mA current levels. Why? Because we did measurements and saw that real leakage current is <10uA…..

FAQ-2

- Q:Wy we need to require some unbalance requirements for Type 3 class 0-4 PDs that have the same power as Type 2 class 0-4 when connected to Type 3 PSE to work as 4P.
- A:
- **If we don't do it, it means we have to design our PSE solution to address zero current on one pair and 10mA on the other pair. This will prevent sensing the current on one of the pairs (since no current is allowed) and derive system decisions regarding detection of open load/wires etc.**
- This is new standard and new PD. This is the only opportunity to do it right and leave NO HOLES.
- While it is justified to require same MPS=10mA total from both use case PDs above, we must put a limit to Type 3 PD unbalance caused by the diodes at low current to Vdiff=58mV max (75% maximum unbalance) This will allow clear and complete PSE solutions to be addressed. PSE will know that it has at least 1.25mA on one of the pair-set.
- It doesn't matter that existing Type 1, 2 PDs have no unbalance requirements. Practically it Type 1,2 PDs and Type 3 class 0-4 has the same 75% maximum unbalance (same diodes are used).
- We just need to close a hole in Type 3 PDs class 0-4, so we can guarantee the validity of PSE MPS solution and in the future we can't claim that "this was not defined so we have hole". **Not defining critical parameter is invitation for problems…**

FAQ-3

- Q: Why we need Current>0, on one of the pairs when we have P2P unbalance conditions at low current as a result of PD P2P unbalance?
- A: Current is the way we sense that a pair-set is not left open without having a load connected to it
- In previous presentations we show that we could have before and after Connection check/ Detection phase:
  - Open wires with live 57V
    - Dual PD loads
    - X cables with two different PDs
    - Open pins/wire
    - Loose Pin/Wire
    - Etc.
  - We need to guarantee some minimum current and the rest what PSE will do with it is implementation.

Thank You

Backup Slides

Most of the material was taken from http://www.ieee802.org/3/bt/public/jan15/darshan_02_0115.pdf
Slides 25-25 are new.

References

1. http://www.ieee802.org/3/bt/public/mar15/darshan_03_0315.pdf