IEEE P802.3bt
PSE State Diagram Update

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March 15

Outline

- Introduction
- PSE States
- Diagram Hierarchical Concept
- Diagram Transition Simplification

Introduction

- First, we create a high-level state diagram with blocks defined by the management status register.
- Next, we identify all arcs in the existing PSE state diagram with numbers.
- Next, we build a top-level block diagram showing all of the relevant arcs between those blocks
- Then we redraw the individual blocks with arcs coming in, exiting.

Defining Blocks & Identifying Arcs

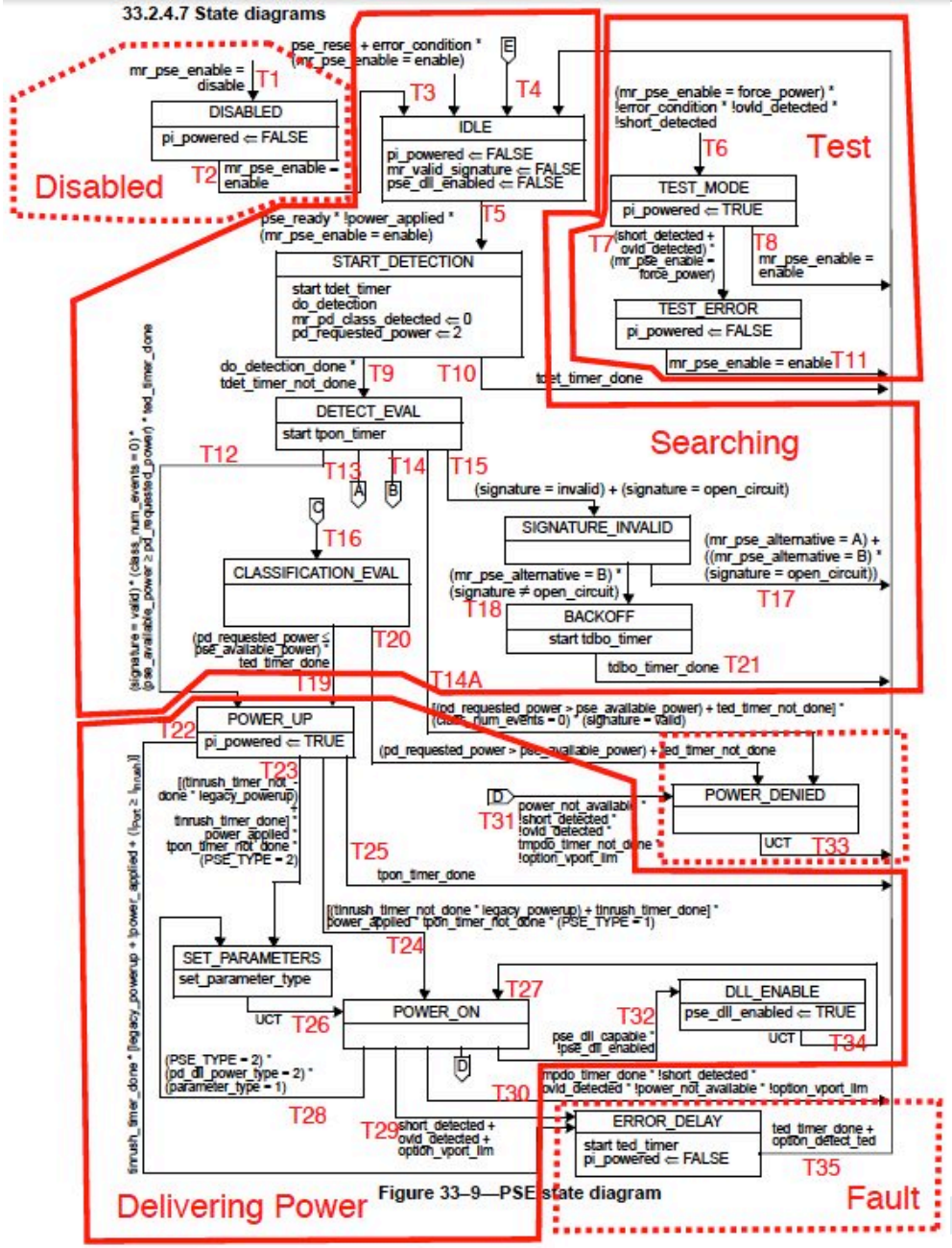
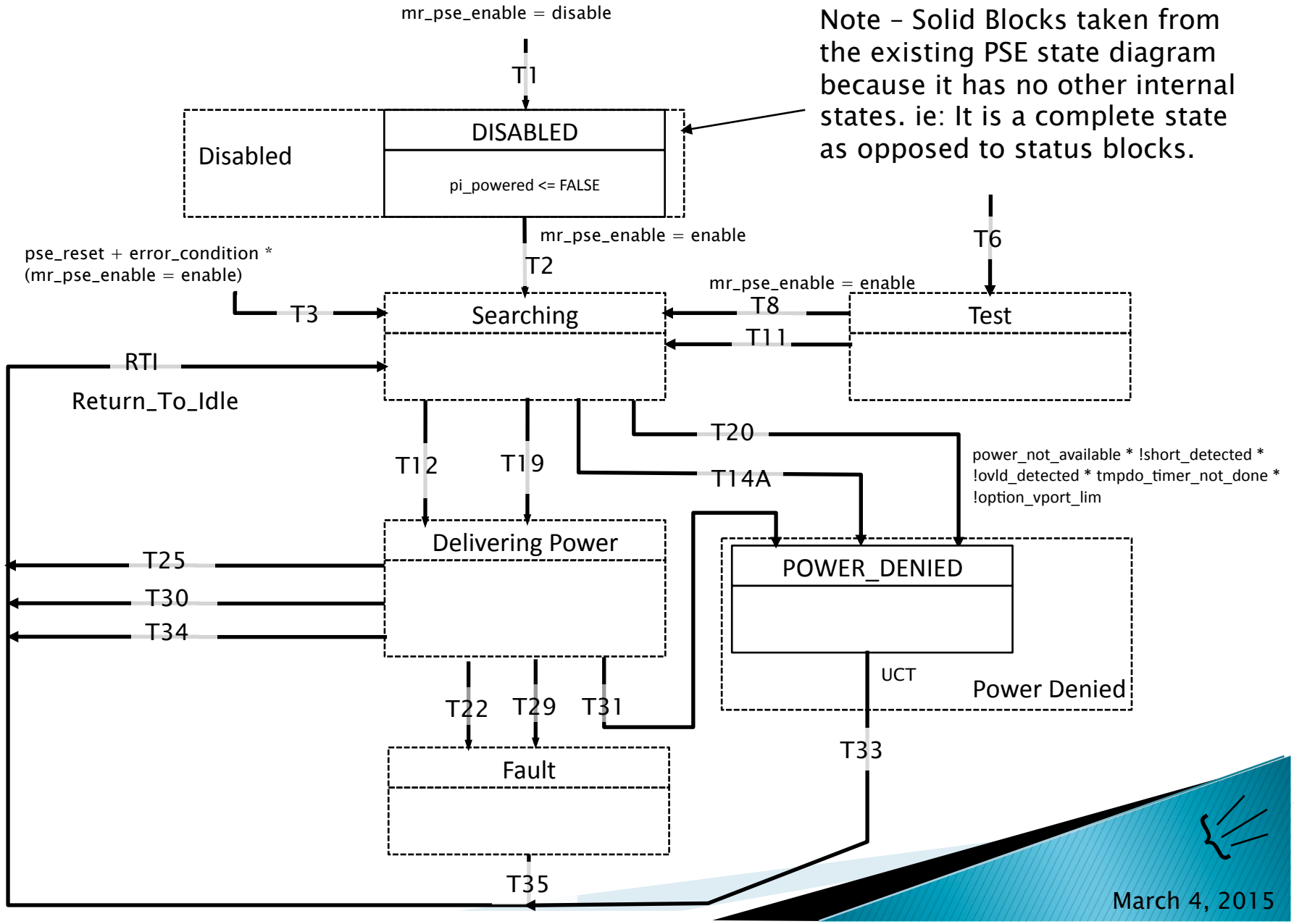
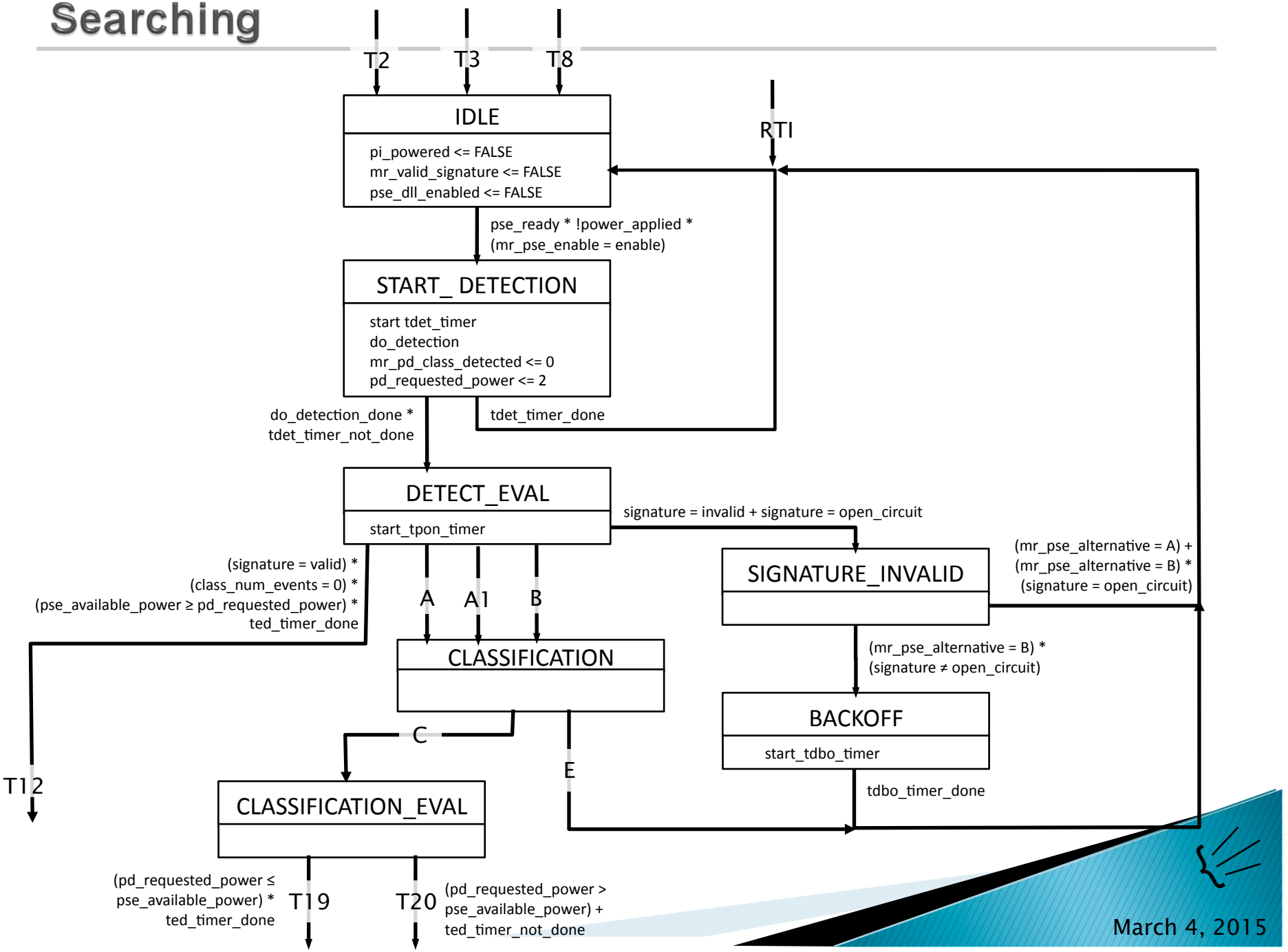


Image taken from
IEEE P8023bt-33_D0p2

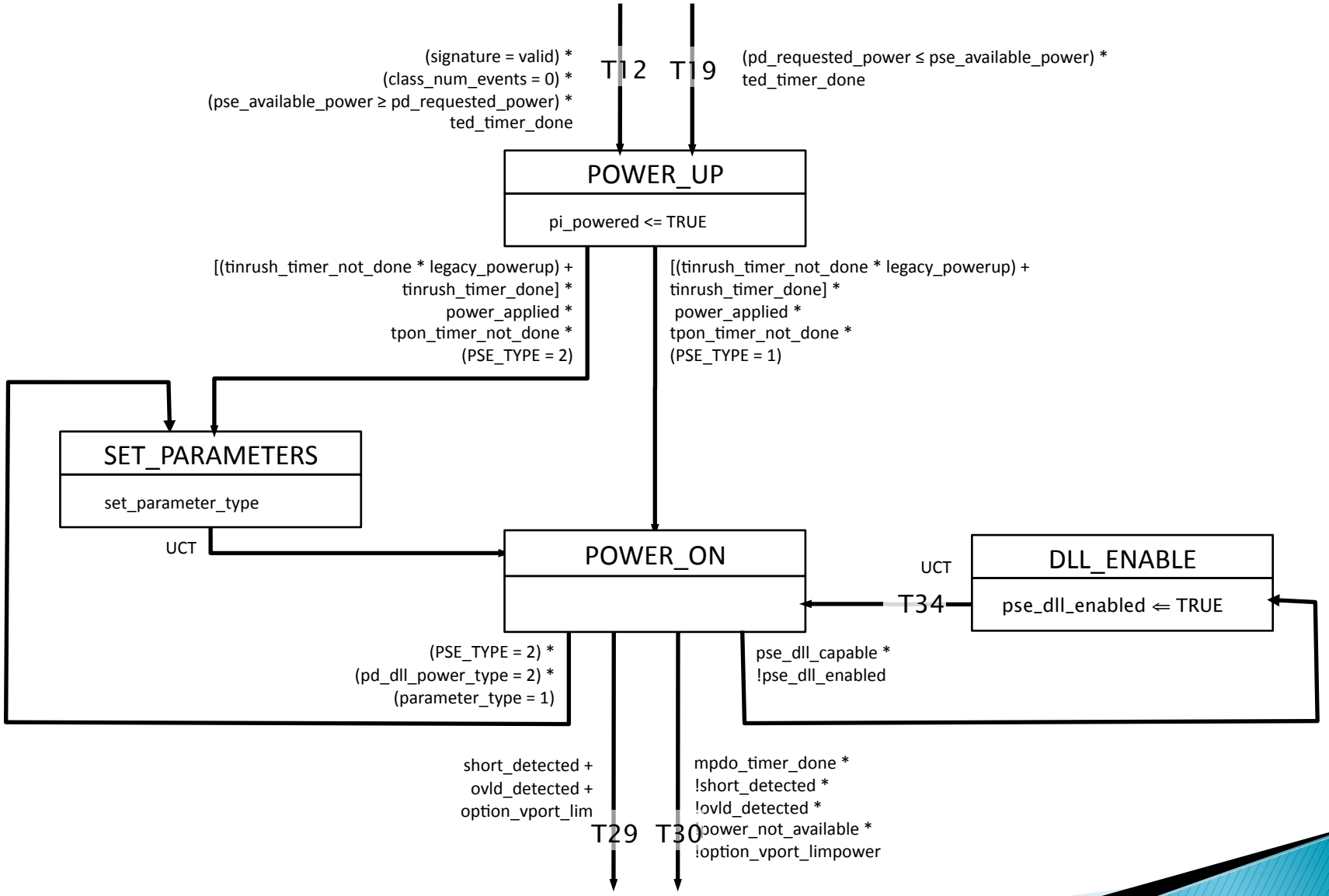
High Level State Diagram



Searching


T2
T3
T8
IDLE
pi_powered <= FALSE
mr_valid_signature <= FALSE
pse_dll_enabled <= FALSE
RTI
pse_ready * !power_applied *
(mr_pse_enable = enable)
START_ DETECTION
start tdet_timer
do_detection
mr_pd_class_detected <= 0
pd_requested_power <= 2
do_detection_done *
tdet_timer_not_done
tdet_timer_done
DETECT_EVAL
start_tpon_timer
signature = invalid + signature = open_circuit
(signature = valid) *
(class_num_events = 0) *
(pse_available_power ≥ pd_requested_power) *
ted_timer_done
A
A1
B
SIGNATURE_INVALID
(mr_pse_alternative = A) +
(mr_pse_alternative = B) *
(signature = open_circuit)
CLASSIFICATION
(mr_pse_alternative = B) *
(signature ≠ open_circuit)
BACKOFF
start_tdbo_timer
tdbo_timer_done
C
E
T12
CLASSIFICATION_EVAL
(pd_requested_power ≤
pse_available_power) *
ted_timer_done
T19
T20
(pd_requested_power >
pse_available_power) +
ted_timer_not_done

Delivering Power



Test, Fault & Power Denied

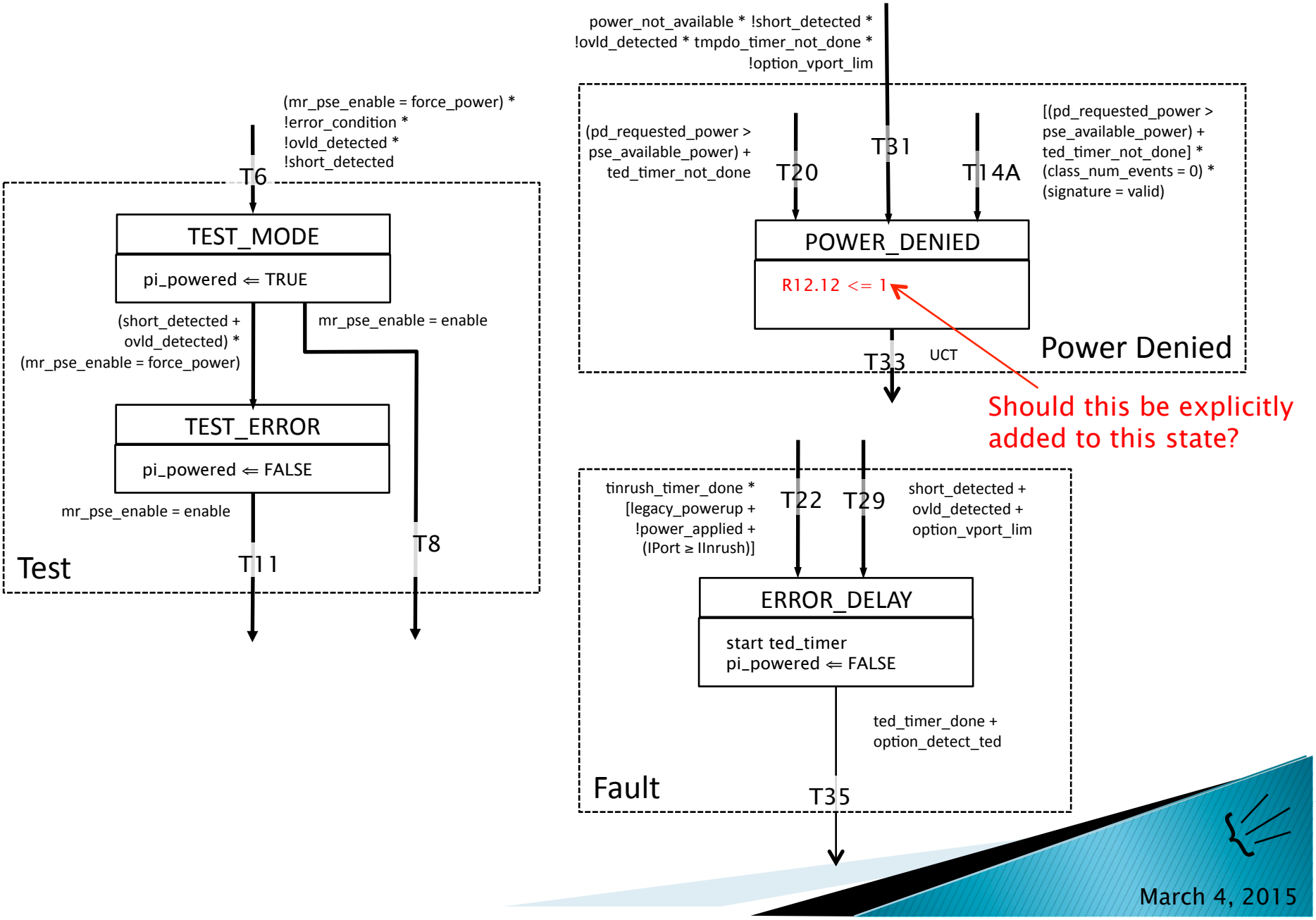


Diagram Transition Simplification

- Identify transition terms that are either common or very complex
- Define new logic terms and then describe that logic in the State Diagram Variables
- Define a common node (RTI) to simplify diagram

Examples:

Complex:

Ready_2_Power = [(tinrush_timer_not_done * legacy_powerup) + tinrush_timer_done] * power_applied * tpon_timer_not_done

- Makes T23 = Ready_2_Power * (PSE_TYPE = 2)
- Makes T25 = Ready_2_Power * (PSE_TYPE = 1)

Common:

Enable_Pwr = (mr_pse_enable = enable)

Disable_Pwr = (mr_pse_enable = disable)

- Simplifies and reduces many terms in readability/size

RTI = Node called "Return To Idle" which is extremely common node in that many states lead to it. Much simpler than showing 8+ arcs all going into IDLE state.

Comments

- This is a “Work in Progress” and expected to draw some constructive criticism, recommendations, etc.
- The outcome if adopted, would be to have multiple diagrams in the specification rather than a single two-page diagram, but these diagrams will be smaller, easier to understand, and easier to modify to accept future changes.
- The classification portion of the existing PSE State Diagram is assumed to be the current page pretty much as is.
- A few minor modifications have been made that are assumed to be errors.
  - A typo taken out of T23 (removed hyphen)
  - A1 arc added to “Searching” block since it appears as entry into the Classification State
- It’s the author’s opinion, that a good specification is done from the top down, rather than the bottom up. The existing PSE state diagram, while it accurately represents behavior of a PSE, appears to have been designed from the bottom up to explain PSE behavior, rather than to direct design.
- I look forward to further discussion on this approach.