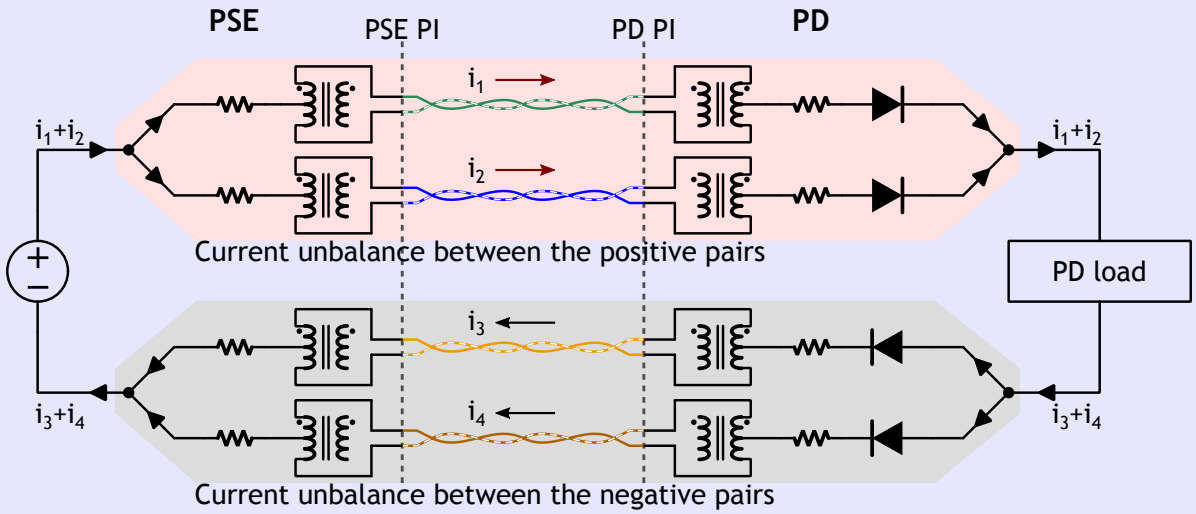
Current specification v100

Info (not part of baseline)

In D3.2 it finally dawned on us that there is no such thing as a "pairset current". The reason being that pair-to-pair current inbalance operates on pairs of **the same polarity** and as such, in 4-pair, the positive current and the negative current of a pairset are different. This baseline reviews all instances of the word "current" in the draft and clarifies or fixes where required.



In addition, on the PD side, we need to specify that current specifications apply to the negative pair (given that one or two positive pairs may conduct).

145.1.3 System parameters

Info (not part of baseline)

Does TIA TSB-184-A only deal with Type 4 current unbalance ? As written, the note suggest Type 3 systems may not have current unbalance...

Table 145–1—System parameters

PSE Type	Nominal highest current per pair (I_{Cable}, A)	Number of powered pairs	Channel pairset maximum DC loop resistance (R_{Ch}, Ω)	Minimum cabling type
Type 3	0.6	2 or 4	12.5	Class D (ISO/IEC11801:1995) or Category 5 (ANSI/EIA/TIA-568-A:1995)
Type 4	0.6	2	12.5	
	0.96	4	12.5	

NOTE—The current per pairset may be impacted by pair-to-pair system resistance unbalance. See 145.2.10.5.1. For additional information on Type 4 current unbalance, see TIA TSB-184-A [Bx1] and ISO/IEC TS 29125.

Change the NOTE below Table 145–1 as follows:

NOTE — The current ~~per pairset~~ on the pairs may be impacted by pair-to-pair system resistance unbalance. See 145.2.10.5.1. For additional information on ~~Type 4~~ current unbalance, see TIA TSB-184-A [Bx1] and ISO/IEC TS 29125.

. . .

In addition to I_{Cable}, the requirements of this clause reference ~~current on a per port and per pairset basis~~ the total current and pairset current, which are described here.

I_{Port} is the total current on both pairs with the same polarity and is defined in Equation (145–7).

$I_{Port\text{-}2P}$ is the current on the negative pair of a pairset and is derived from $I_{Port\text{-}2P\text{-}pri}$ and $I_{Port\text{-}2P\text{-}sec}$ in Equation (145–5).

Insert new definition for "pairset current" as follows:

Pairset current is the current on the negative pair associated with a given pairset. Note that the positive pair and the negative pair of a pairset may carry a different amount of current, caused by the independent pair-to-pair current unbalance in the positive pairs, and in the negative pairs, when the system is providing power over more than 2 pairs.

Info (not part of baseline)

This definition for "pairset current" makes use of that term in the draft correct for a large number of cases.

145.2.4 PSE PI

Info (not part of baseline)

Involving a pairset in the second sentence is confusing, as this tries to explain that a pair acts as a conductor. Has nothing to do with pairsets.

A PSE device may provide power via one or both of the two valid four-conductor connections, named pairsets. A pairset consists of a pair at the positive V_{PSE} and a pair at the negative V_{PSE}. ~~In each pairset, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity.~~ The two conductors associated with a pair each carry the same nominal current in both magnitude and polarity.

. . .

Info (not part of baseline)

The requirement below was added to D3.2 as a catch-all. With the new definitions and clarifications in the text, I don't think we need it anymore.

~~The PSE shall meet all specifications related to current on the negative pair or pairs unless otherwise noted.~~

145.2.10 Power supply output

Change the Parameter of the listed items in Table 145–16 as follows

Info (not part of baseline)

The definition for $I_{Con\text{-}2P\text{-}unb}$ is tricky and best handled in 145.2.10.5.1. Because unbalance must be supported on both positive and negative, use of "pairset current" does not suffice here.

5	$I_{Con\text{-}2P\text{-}unb}$	Supported ~~pairset~~ pair current to account for unbalance per the assigned Class (for single-signature PDs)
7	$I_{Inrush\text{-}2P}$	Output current ~~per pairset~~ on the powered negative pairs during power up per the assigned Class
8	T_{Inrush}	Inrush time ~~per pairset~~
10	T_{CUT}	Overload time limit ~~per pairset~~
12	T_{LIM}	Short circuit time limit ~~per pairset~~
18	$I_{Hold\text{-}2P}$	DC MPS current ~~to be met~~ on at least one pairset, per the assigned Class DC MPS current ~~to be met~~ on each powered pairset
19	I_{Hold}	DC MPS total current ~~to be met when the sum of both~~ on both pairs ~~with~~ of the same polarity ~~is measured~~, per the assigned Class

145.2.10.5 Continuous output current capability in the POWER_ON state

$I_{Port\text{-}2P}$ and $I_{Port\text{-}2P\text{-}other}$ are the currents on the negative pairs ~~with the same polarity~~ and are defined in Equation (145–5) and in Equation (145–6).

. . .

Info (not part of baseline)

The PSE needs to support $I_{Con\text{-}2P\text{-}unb}$ both on the negative pairs and the positive pairs (but not on both pairs at the same polarity at the same time). To make that work we use the construct "the current the PSE supports on both pairs of each powered pairset".

Propagate changes to parameter descriptions consistently in Clause 145.

(Equation 145–8)
where

$I_{Port\text{-}2P\text{-}pri}$ is the output current ~~sourced~~ supplied on the negative pair of the Primary Alternative
$I_{Port\text{-}2P\text{-}sec}$ is the output current ~~sourced~~ supplied on the negative pair of the Secondary Alternative

PSEs shall be able to ~~source~~ supply $I_{Con\text{-}2P}$, the current the PSE supports on both pairs of each powered pairset, as defined in Equation (145–8). $I_{Con\text{-}2P}$ should be measured using a sliding window with a width of 1 second.

(Equation 145–8)
where

$I_{Con\text{-}2P\text{-}unb}$ is the current a PSE is able to ~~source~~ supply on ~~a pairset~~ each pair to account for pair-to-pair unbalance as defined in Table 145–16
$I_{Port\text{-}2P\text{-}other}$ is the output current on the other ~~pairset~~ negative pair as defined in Equation (145–6)

When powering a single-signature PD over 4 pairs, a PSE supports:

– A total current of I_{Con}, defined in Equation (145–9), over both pairs with the same polarity;
– ~~A minimum current of $I_{Con\text{-}2P\text{-}unb}$ one of the pairs of the same polarity under maximum unbalance condition (see 145.2.10.5.1) in POWER_ON.~~
– A minimum current of $I_{Con\text{-}2P\text{-}unb}$ on each pair, while the PSE provides a total current less than I_{Con}, to account for pair-to-pair unbalance (see 145.2.10.5.1).

. . .

The PSE shall support the AC current waveform parameter $I_{Peak\text{-}2P}$, defined in Equation (145–10), on on both pairs of each powered pairset, while within the operating voltage range of $V_{Port\_PSE\text{-}2P}$, for a minimum of T_{CUT} and a duty cycle of at least 5%.

(Equation 145–10)

where

$I_{Port\text{-}2P\text{-}other}$ is the ~~output~~ current on the other ~~pairset~~ negative pair as defined in Equation (145–6)
$I_{Peak\text{-}2P\text{-}unb}$ is the minimum peak current ~~due to unbalance effects~~ a PSE ~~supports~~ is able to supply on each pair ~~a pairset~~ to account for pair-to-pair unbalance as defined in Equation (145–12)

. . .

$I_{Peak\text{-}2P\text{-}unb}$, defined in Equation (145–12), is the minimum current ~~due to unbalance effects~~ that a PSE ~~supports~~ is able to supply on ~~a pairset~~ on each pair, while the PSE provides a total current less than I_{Peak}, when powering a single-signature PD over 4 pairs, in order to account for pair-to-pair unbalance.

145.2.10.5.1 PSE pair-to-pair current unbalance

. . .

The PSE PI pair-to-pair effective resistance unbalance determined by R_{PSE_max} and R_{PSE_min}, along with any other parts of the system, i.e., the cabling and the PD, bounds the current such that the ~~pairset~~ pair with the highest current including unbalance does not exceed $I_{Unbalance\text{-}2P}$ as defined in Table 145–17 during normal operating conditions. $I_{Unbalance\text{-}2P}$ is the highest ~~pairset~~ pair current in case of maximum unbalance and will be higher than $I_{Con}/2$. $I_{Unbalance\text{-}2P}$ applies to link section common mode pair resistances from 0.2 Ω to R_{Ch}, as defined in 145.1.3.

145.2.10.6 Output current during power up

Info (not part of baseline)

total output current on the negative pairs = total current

. . .

The PSE shall limit the current on each powered negative pair to $I_{Inrush\text{-}2P}$ and the total output current ~~on the negative pairs~~ to I_{Inrush} during power up per the requirements of Table 145–16, with the exception of the initial per pairset transient described in Equation (145–16).

145.2.10.7 Overload current

If $I_{Port\text{-}2P}$ ~~, the current supplied on a pairset by the PSE to the PI,~~ exceeds $I_{CUT\text{-}2P}$ for longer than T_{CUT}, the PSE may remove power from that pairset. The cumulative duration of T_{CUT} is measured using a sliding window of at least 1 second width.

145.2.10.8 Output current — at short circuit condition

A PSE may remove power from the PI if the ~~PI~~ current on any pair meets or exceeds the "PSE lowerbound template" in Figure 145–23 or Figure 145–24. Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" in Figure 145–23 or Figure 145–24. When connected to a single-signature PD, the PSE should remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset. ¶

. . .

(Equation 145–20)
where

$I_{Peak\text{-}2P}$ is ~~$I_{Peak\text{-}2P}$ per pairset~~ the minimum peak current supported on each powered pair, as defined in Equation (145–12)

$I_{Con\text{-}2P}$ is the minimum supported continuous current on ~~a pairset~~ each powered pair as defined in 145.2.10.5

145.3.2 PD PI

Info (not part of baseline)

We need to explain how the PD's requirements related to current need to be met. For a single-signature, with the exception of current unbalance limits during POWERED, the PD needs to meet a total current requirement (ergo, no unbalance limit), unless otherwise specified. For a dual-signature, the PD needs to meet the current requirement on the negative pair of a given Mode, unless otherwise specified.

The PDs PI consists of 8 conductors. The two conductors associated with a pair are at the same nominal voltage. A pairset consists of two pairs, as defined in 145.2.4. The two pairsets are named Mode A and Mode B, which correspond with Alternative A and Alternative B. Figure 145–12 in conjunction with Table 145–20 illustrate the two power modes.

PDs shall be capable of accepting power in any valid 2-pair configuration and any valid 4-pair configuration as defined in Table 145–20.

A single-signature PD shall meet all specifications related to current by drawing the correct total current, where total current is the combined current of the two pairs at the same polarity, unless otherwise noted. A dual-signature PD shall meet all specifications related to current by drawing the correct current on the negative pair of a given Mode, unless otherwise noted.

The PD shall be insensitive to the polarity of the voltage applied on each Mode regardless of the polarity of the voltage applied on the other Mode. Single-signature PDs that request Class 4 or less shall be able to operate if power is supplied with any valid configuration defined in Table 145–20. All other PDs may require being supplied with a valid 4-pair configuration to operate at their nominal power level.

145.4.2 Fault tolerance

Info (not part of baseline)

First of all, it isn't the PSE PI that should not be damaged, it is the PSE itself. Second, the current magnitude limit is appropriate for any one to any one conductor. The damage requirement however should apply to any set of conductors shorted together.

The PSE ~~PI~~ shall withstand without damage the application of short circuits of any conductors ~~to any other conductor~~ within the cable for an indefinite period of time. The magnitude of the current caused by a short circuit of any one conductor to another conductor in the cable ~~through such a short circuit~~:

– shall not exceed $I_{PSEUT\text{-}Type3\text{-}2P}$, as defined in Equation (145–17), for Type 3 PSEs
– shall not exceed $I_{PSEUT\text{-}Type4\text{-}2P}$, as defined in Equation (145–18), for Type 4 PSEs