ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

Inrush NOPOWER

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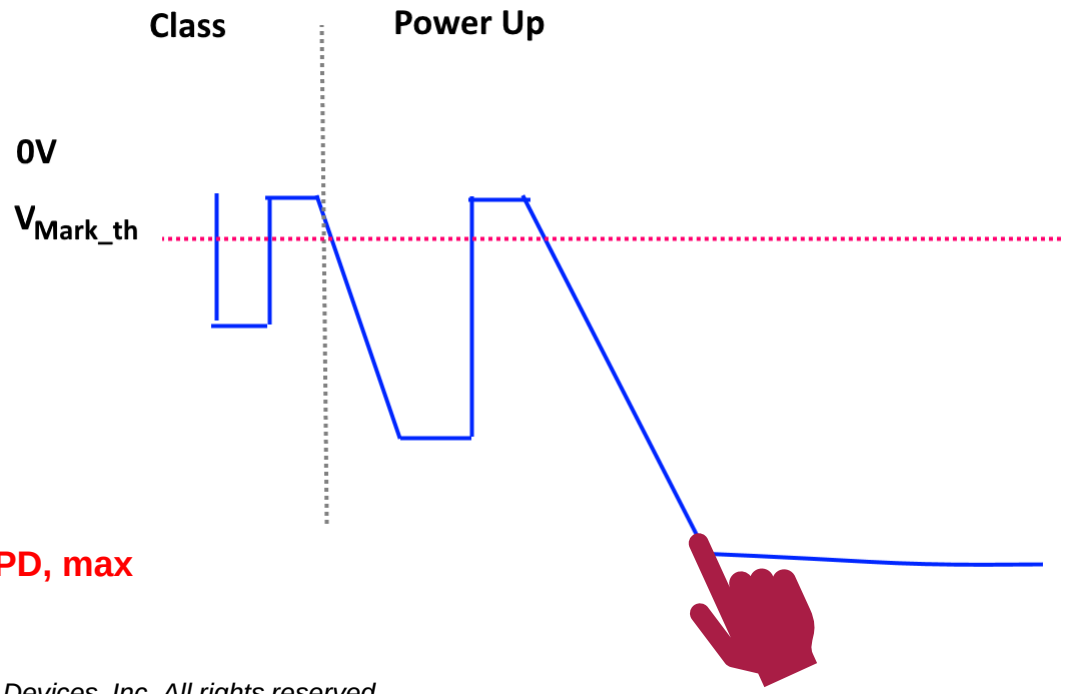
Summary

- As written PD INRUSH state does not allow a PD to increment pse_power_level
- PD INRUSH state has a duration of exactly 50ms
- PD PI V_{PD} may drop below V_{Mark_th} during the INRUSH state
  - **Case 1:** PD itself causes the voltage transient
    - e.g. Switching on a substantial bulk capacitance
  - **Case 2:** PD input voltage is manipulated externally
    - e.g. PD compliance testing
  - This voltage manipulation may be interpreted as a “false” mark event

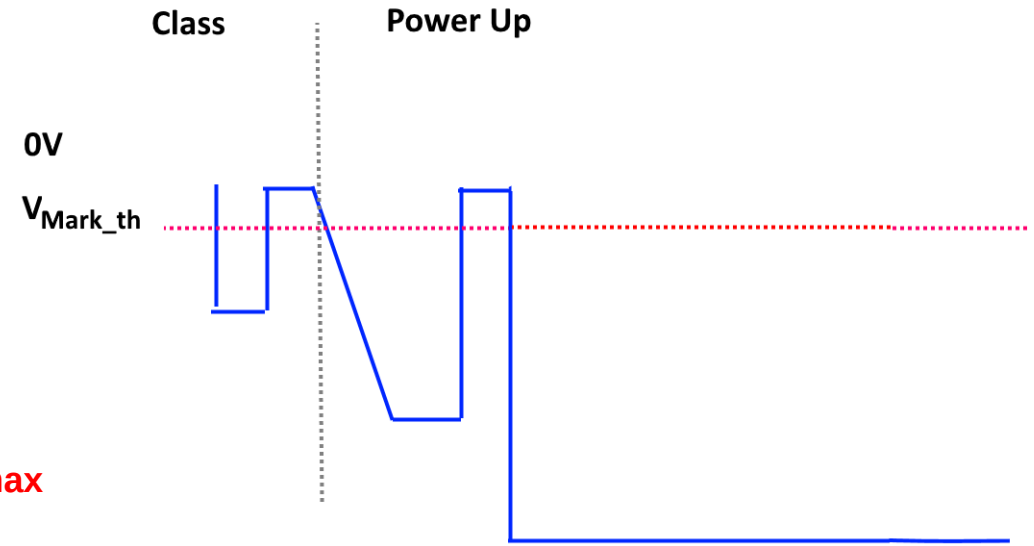
Case 1
PD Causes “False” Mark Event

- In this case, PD has *caused* the voltage drop
- Burden is on PD not to “increment” pse_power_level
  - Risks tricking itself into thinking it has been allocated additional power
- Note: A PD is not allowed to oscillate during power up



Case 2
(Invalid) PSE Causes “False” Mark Event

- Many PDs stay below I_{Inrush_PD} during power up
  - A valid PSE will **not** collapse the voltage in this case
- In a compliant system, PD input voltage does not drop below V_{Off_PD} during inrush
  - No interoperability requirement exists in this case
- Compliance with D3.3 INRUSH is an unnecessary burden for these PDs
  - No interoperability benefit



$I_{PD} < I_{Inrush\_PD, max}$

Baseline Fix