Analysis of High Side Current Sensing Architecture with Single Power Channel

System Efficiency, Accuracy, Thermal and System Costs Considerations

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Goal of this Presentation

The motivation of this work is to clarify and correct statements in stewart_01_0514.pdf presentation. This is done by analyzing the new architecture \(^1\) which uses two high side current sensing elements and a single PSE power switch.

- Power Dissipation and Heat
- Current Measurement and FET Control Complexity
- System Cost

\(^1\) – See stewart, “4 Pair PoE Cost Comparison Redux”
Impact of DC Disconnect Accuracy on High Side Current Sensing and System Efficiency

- The new architecture \(^1\) uses one sense resistor per 2P, as shown below.

- As explained in previous presentation \(^2\), if “bt” PSE is connected to a single “at” PD interface, the DC disconnect threshold **CANNOT** change

  \[ \Rightarrow \] is same as defined in “at” spec: 5-10 mA

  \[ \Rightarrow \] **this mandates a “global” (4P) sense resistor value** of 0.255 Ohms\(^3\) while doing DC disconnect measurement otherwise the accuracy of the measurement goes down.

  \[ \Rightarrow \] In the present case, same current is split between 2 elements and there is still only one power switch, this mandates **0.51 Ω** per resistor, to just maintain same accuracy.

- The system power loss in high power is **the same**, there is no improvement and it is still problematic.

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1-power channel configuration drives all pairs at same time.

This limitation is due to its architecture.

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2 – See Picard, “An Optimum Approach to Apply DC Disconnect”

3 - Lowest in industry sense resistor value used by PSE controllers working with external MOSFET is 0.255 Ohm.
Calculation Example

- PD with 51W input and 40m cable length (for more details see 2)
- As shown below, the system power loss in high power is **the same** as the old architecture, there is **no** improvement.
- As explained before 2, the 4P efficiency savings are (still) lost by excess power dissipation on the sense resistor. The concept of **4P power savings is lost**.
- Consequently, the following conclusions of document 1 are proven to be incorrect.
  - Slide 11 says “Heat argument eliminated by 2 sense architecture”.
  - Slide 8 says “Rsense argument eliminated by 2 sense architecture”

**Old Architecture**

Calculation Example:

\[
(1.08A)^2 \times 0.255 \Omega = 0.296W
\]

**New Architecture**

Calculation Example:

\[
(0.54A)^2 \times 0.51 \Omega \times 2 = 0.296W
\]
Why the 2 Switches Approach is More Efficient and Accurate at Same Time?

- **Methodology:**
  - Drive 4P if “bt” PD
  - If “at” PD:
    - Drive 4P, then when DC disconnect is “suspected”, do DC disconnect check with **1st switch only** for high accuracy.
    - This explains why with 2 switches, each sensing resistor can be as low as 0.255 ohm (and not 0.51 ohm).
  - This method combines **all the positive system aspects**

![Diagram showing the circuit and current flow](image)
Additional Thermal Problems with High Side Current Sensing

- Dissipation is from 2 main elements, the FET and the resistor.
- The FET heat is usually transmitted to air through FET body and drain PCB trace/copper surface, which size is limited.
- The Resistor heat is usually directly transmitted to GND plane through electrical & thermal contact, which large copper surface helps to keep temperature low.
- But, with the high side sensing, the resistors are on the drain of the FET:
  - There is no longer any GND plane to which the resistor can transfer its heat.
  - *Where will the heat go?*
- Even worse, both the resistors and FET transfer their heat to the *same drain trace*, which is limited in size.
- This can be the source of serious FET temperature problems and failures.
Other Considerations, Complexity & Costs

• Sensing voltage across a shunt with one side referenced to GND is easiest

• The architecture using two “floating” drain current sense resistors (one for each pair) introduces significant design complexity:
  – Requires means to shift that voltage down to digital domain voltage range.
  – Using a difference amplifier to measure a small voltage and ignore a large common mode voltage is challenging.
  – Even worse when the common mode is “variable” (the drain is not a constant voltage).
  – Requires accurate rail to rail, low offset/high speed, high CMRR current sense instrumentation amplifier for each of the current sense drain resistors
  – Needs additional circuit blocks for each sense resistor to manage high speed short circuit and closed loop ILimit control. Reaction to severe overload (ex: short circuit) must be fast, otherwise very high current may be reached which would be detrimental to the system.

Simple Ground referenced sense Architecture

New 2 high side sense Architecture

50V

Addtl circuitry, level shifters,...

Addtl circuitry, level shifters,...

Control

Load
High Side sensing: Complexity & Costs

- One approach would be to have floating circuitries “riding” on the DRAIN pin, adding a LOT of complexity.
  - Much larger size than a low side, high speed comparator with the direct feedback to the GATE amplifier.
- Another approach would be to fully isolate and float (for each channel) the A/D, Ilim and Isc blocks, ..., which means fundamental changes.
- So, the savings with high side sensing would be minimal, if any.

<table>
<thead>
<tr>
<th></th>
<th>2-power channel</th>
<th>1-power channel High side Drain sensing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Current Sense</td>
<td>2 very simple</td>
<td>2 Highly complex</td>
</tr>
<tr>
<td># pins</td>
<td>+3 per 4P</td>
<td>+1 per 4P</td>
</tr>
</tbody>
</table>
Systems Costs and Complexity

- Below is a summary of overall cost per port.
- Note that document 1 says "field data support 1.25x" for the MOSFET is not clear. The 1.5x shown below is based on true high volume prices.
- In fact, this factor could even be 2x, since the volume would be much lower for the bigger FET (most of “30W and lower” market would use a smaller FET).
- Also (not shown below), the 2-power channel architecture has indirect savings from being more efficient.

<table>
<thead>
<tr>
<th>Component</th>
<th>Weighting</th>
<th>Increase over AT*</th>
<th>Effective Contribution</th>
<th>Increase over AT*</th>
<th>Effective Contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magjack</td>
<td>61.0%</td>
<td>15.0%</td>
<td>9.15%</td>
<td>35.0%</td>
<td>21.35%</td>
</tr>
<tr>
<td>PCB</td>
<td>14.0%</td>
<td>0.0%</td>
<td>0.00%</td>
<td>20.0%</td>
<td>2.80%</td>
</tr>
<tr>
<td>PoE Controller</td>
<td>14.0%</td>
<td>100.0%</td>
<td>14.00%</td>
<td>40.0%</td>
<td>5.60%</td>
</tr>
<tr>
<td>FET</td>
<td>8.0%</td>
<td>100.0%</td>
<td>8.00%</td>
<td>50.0%</td>
<td>4.00%</td>
</tr>
<tr>
<td>Sense Resistor</td>
<td>1.5%</td>
<td>100.0%</td>
<td>1.50%</td>
<td>200.0%</td>
<td>3.00%</td>
</tr>
<tr>
<td>TVS Diode</td>
<td>1.5%</td>
<td>100.0%</td>
<td>1.50%</td>
<td>0.0%</td>
<td>0.00%</td>
</tr>
<tr>
<td>Total Cost Increase</td>
<td></td>
<td>34.15%</td>
<td></td>
<td>35.15%</td>
<td>36.75%</td>
</tr>
</tbody>
</table>

* Magjack savings applicable only if overload protection (ICUT) is a requirement per 2P to avoid damage to the data transformers.
**Summary**

In summary, the high side drain current sensing combines all the negative system aspects of complexity, thermal, efficiency with _no_ cost benefit.

<table>
<thead>
<tr>
<th>PD Configuration</th>
<th>Dual Power Channel</th>
<th>Single Power Channel with High Side Sensing</th>
</tr>
</thead>
<tbody>
<tr>
<td>“bt” PD Interface, High Power PDs</td>
<td>Simple thermal design</td>
<td>Thermal issues, highly problematic thermal design</td>
</tr>
<tr>
<td>Single “at” PD Interface</td>
<td>High accuracy, Low complexity</td>
<td>Highest PSE dissipation &amp; temperature, Highest system + PCB cost, Highest Complexity</td>
</tr>
<tr>
<td></td>
<td>Lowest PSE dissipation &amp; temperature</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Lowest system cost</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Highest system efficiency</td>
<td>Medium-Low system efficiency</td>
</tr>
</tbody>
</table>