PI – 57 V – Comment 142, Maintenance Request 1274

IEEE 802.3: 4PPOE Task Force

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Comment 142

Cl **33** *SC* **33.3.1** *P* **64** *L* **53** # 142

Jones, Chad Cisco

Comment Type **T** *Comment Status* **D** *PD PI*

Maintenance Request #1274 on behalf of George Zimmerman, CME Consulting/LTC

Text in the existing standard is ambiguous and is inconsistent with terminations and usage commonly found in Ethernet equipment. The intent is to require PDs to be able to withstand application of common-mode PoE voltage. Application of 57V DC voltages in across the pins corresponding to the two pairs twisted differentially to form a balanced pair of the link segment would run a DC current across the transformer windings commonly found in BASE-T Ethernet equipment and burn them out.

SuggestedRemedy

Change: The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.
To:The PD shall withstand any common-mode voltage from 0 V to 57 V applied to any two sets of two pins at the PI indefinitely without permanent damage. The two pins in each set shall correspond to the balanced twisted wire pairs of the connected link segment.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This should be clarified. Can we use the definition of pair-set make this simpler?

33.3.1

- “The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.”
- Issues:
  - Clearly this doesn’t mean across balanced differential pairs?
  - Voltage at the PI? It has 8 pins.
    - Between what two points?
    - Which combinations of pins?

The concept

- 57V can be applied in common mode between pin-sets: (1,2), (3,6), (4,5), (7,8)
- Voltage can be between, say:
  - (1,2) and (3,6)
  - (1,2) and (4,5)
  - (1,2) and (7,8)
  - (3,6) and (4,5)
  - (3,6) and (7,8)
  - (4,5) and (7,8)

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{P}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

Original Proposed Remedy

- Original proposed remedy is incomplete – only covers “common mode” vs. “differential mode” issue
  - Editor’s suggestion to use pair-sets is good, but would require a mapping from pair-sets to pins at the PD. (Table 33-13 is a start, but requires new text to be carefully crafted to connect to pinout to pair-sets)
    - Also, isn’t a pair-set 4 pins?

New Proposed Remedy

Change: The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

To: The PD shall withstand any voltage difference from 0 V to 57V applied between any pin-pairs at the PI indefinitely without permanent damage. The two pins in each pin-pair shall correspond to those which connect to balanced twisted wire pairs of a link segment, and include any combination of pin-pairs from the set {(1,2), (3,6), (4,5), (7,8)}, as indicated in Table 33-13.

The voltage may be simultaneously applied across more than one set of two pin-pairs.

The text highlighted in yellow appears to be the issue still to be resolved.