Comment # 30 page 141 lines 25-40.
Adding text that addresses the new 110uF value for dual-signature class 1-4.

To update 33.3.7.3 page 141 lines 25 - 40

33.3.7.3 Input inrush current

Input inrush currents at startup, I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, as defined in Table 33–17, are limited by the PSE if $C_{Port} < 180$ µF for single-signature PDs assigned to Class 0 to 6, and if $C_{Port} < 360$ µF for PDs assigned to Class 7 or 8.
Input inrush current at startup, $I_{Inrush\ PD\text{-}2P}$, is limited by the PSE if $C_{Port\text{-}2P} < 110$ µF for dual-signature Type 3 PDs~~.~~ and if $C_{Port\text{-}2P} < 180$ µF for dual-signature Type 4 PDs.
If a PD has a larger C_{Port} or $C_{Port\text{-}2P}$ value, then the PD shall limit the input inrush current such that I_{Inrush_PD} max and $I_{Inrush\_PD\text{-}2P}$ max, as defined in Table ~~33–17~~33-28, are met.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush\text{-}2P}$ min. See 33.2.8.4 for details.

C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port\text{-}2P}$ in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–37 for a simplified PSE-PD C_{Port} and $C_{Port\text{-}2P}$ interpretation model.