Changes from SS PD to DS PD state machine.

1) Dual-signature PD operating principle: two separate state machines for Mode A and Mode B.

2) Naming constants, variables, timers and functions: xxxx_modeA and xxxx_modeB.

Autoclass is not used for dual-sig. (No need per inputs got so far).

There is a consensus between Yair, Fred, Dylen, Chriss and Lennart so far that AUTO_CLASS is not required for dual-sig PDs. It is not a problem to add it later. We need more marketing inputs.

3) present_det_sig_modeA, present_det_sig_modeB: A text was added that defines this variable should be valid or not regardless if the other pairset is powered with voltage above Vreset.

Other options such not allow a pairset to go into OFFLINE when the other pairset is powered was considered however the problem with this approach is that if we look at dual-sig PD as two independent PDs that are closed in a single PD box than one of the pairsets can be in OFF-LINE at any time regardless of what the other pair is doing.

4) present_class_sig_A_modeA/B and present_class_sig_B_modeA/B is TRUE also if power__recived_modeB/A is TRUE is OK automatically whenever Vclass is in range.

5) pd_dll_capable was removed since dual-signature PD need to support DLL.

6) pd_max_power_modeA values were set to 5 max.

7) PSE state machine for supporting dual-signature PD needs separate DLL_ENABLE for primary and secondary.

Baseline starts at next page:

1. Update 33.3.3.11 as follows:
2. Add the dual-signature state machine drawings darshan_07_0516.pdf and darshan_08_0516.pdf
3. To add the following editor note at the PSE state machine section: "Editor Note: PSE state machine for supporting dual-signature PD needs separate DLL ENABLE for primary and secondary."

33.3.3.11 Type 3 and Type 4 dual-signature PD State diagrams

Editor Note: PD power control state diagram (Figure 33-50) need to be evaluate and sync with the dual-signature state machine.

33.3.3.x1 Type 3 and Type 4 Constants for dual-signature PD

To reuse the constant from Table 33-26 to be per pairset, a text was added to indicate it without the need to change Table 33-26 or change it to Vreset-2P, Vreset_th_2P, and Vmark_th-2P respectively in Table 33-26.

The PD state diagram uses the following constants:

VReset

Reset voltage per pairset (see Table 33–26)

VReset_th

Reset voltage threshold per pairset (see Table 33–26)

VMark_th

Mark event voltage threshold per pairset (see Table 33–26)

pd_req_class_modeA

A constant indicating the requested Class of the PD over mode A.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

pd_req_class_modeB

A constant indicating the requested Class of the PD over mode B.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

33.3.3.x2 Type 3 and Type 4 Variables for dual-signature PD

The PD state diagram uses the following variables:

mdi_power_required_modeA

A control variable indicating that over mode A, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:

FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

mdi_power_required_modeB

A control variable indicating that over mode B, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:

FALSE:PD functionality is disabled.

TRUE:PD functionality is enabled.

pd_dll_enabled_modeA

A variable indicating whether the Data Link Layer classification mechanism is enabled over mode A.

Values:

FALSE:Data Link Layer classification is not enabled.

TRUE:Data Link Layer classification is enabled.

pd_dll_enabled_modeB

A variable indicating whether the Data Link Layer classification mechanism is enabled over mode B.

Values:

FALSE:Data Link Layer classification is not enabled.

TRUE:Data Link Layer classification is enabled

pd_max_power_modeA

A control variable indicating the max power that the PD may draw from the PSE over mode A. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power

2: PD may draw Class 2 power

3: PD may draw Class 3 power

4: PD may draw Class 4 power

5: PD may draw Class 5 power

pd_max_power_modeB

A control variable indicating the max power that the PD may draw from the PSE over mode B. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power

2: PD may draw Class 2 power

3: PD may draw Class 3 power

4: PD may draw Class 4 power

5: PD may draw Class 5 power

pd_reset_modeA

An implementation-specific control variable that unconditionally resets the PD state diagram over mode A to the OFFLINE_modeA state.

Values:

FALSE:The device has not been reset (default).

TRUE:The device has been reset.

pd_reset_modeB

An implementation-specific control variable that unconditionally resets the PD state diagram over mode B to the OFFLINE_modeB state.

Values:

FALSE:The device has not been reset (default).

TRUE:The device has been reset.

pd_undefined_modeA
A control variable that indicates that the PD is in an undefined condition over mode A. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeA variable.
Values:
FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

pd_undefined_modeB
A control variable that indicates that the PD is in an undefined condition over mode B. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeB variable.
Values:
FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

power_received_modeA
An indication from the circuitry that power is present on the PD's PI over mode A.
Values:
FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

power_received_modeB
An indication from the circuitry that power is present on the PD's PI over mode B.
Values:
FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

present_class_sig_A_modeA
Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode A.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_A_modeB
Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode B.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B_modeA
Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode A (see 33.3.5) by the PD.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B_modeB
Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode B (see 33.3.5) by the PD.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

A text was added to present_det_sig_modeA and present_det_sig_modeB in order to ensure that that providing a power on a pairset will not cause to the unpowered pairset signature to be invalid.

present_det_sig_modeA
Controls presenting the detection signature (see 33.3.4) by the PD over mode A.
Values:
invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
.
valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
either: Either a valid or non-valid PD detection signature may be applied to the link.

present_det_sig_modeB
Controls presenting the detection signature (see 33.3.4) by the PD over mode B.
Values:
invalid: A non-valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.
.
valid:A valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.
either: Either a valid or non-valid PD detection signature may be applied to the link.

present_mark_sig_modeA
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode A.
Values:
FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mark_sig_modeB
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode B.
Values:
FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mps_modeA
Controls applying MPS over mode A (see 33.3.7.10) to the PD's PI.
Values:
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

present_mps_modeB
Controls applying MPS over mode B (see 33.3.7.10) to the PD's PI.
Values:
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

pse_dll_power_level_modeA
A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode A.
Values:
1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5

pse_dll_power_level_modeB
A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode B.
Values:
1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5

pse_power_level_modeA
A control variable that indicates to the PD over mode A the level of power the PSE is supplying.
Values:
3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.
4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.
5: The PSE has allocated the PD's requested power or Class ~~6~~ 5 power, whichever is less.

pse_power_level_modeB
A control variable that indicates to the PD over mode B the level of power the PSE is supplying.
Values:
3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.
4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.
5: The PSE has allocated the PD's requested power or Class ~~6~~ 5 power, whichever is less.

VPD_modeA
Voltage at the PD PI as defined in 1.4.425 over mode A.

VPD_modeB
Voltage at the PD PI as defined in 1.4.425 over mode B.

33.3.3.x3 Type 3 and Type 4 Timers for dual-signature PD

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer_modeA
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode A and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode A during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.

tpowerdly_timer_modeB
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode B and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode B during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.

33.3.3.x4 Type 3 and Type 4 Functions dual-signature PD

do_class_timing_modeA
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode A. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

do_class_timing_modeB
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode B. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.