

Comment #11 (Clause 33.3.2.7.1, Page 140, Line 36)

Proposed remedy

33.3.7.2.1 System stability test conditions during startup and steady state operation

The following note was moved to the beginning of this sub clause as a text to address the stability title.

~~Note~~— When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

Yair: I agree that equation 33-23 alone is meaningless. $P=V*I$ is always true and it is not sufficient as test condition for stability. [The following changes were made to correct it and it doesn't add requirements to PSE nor PD.](#)

When ~~the a Type 1, Type 2, single-signature Type 3, or single-signature Type 4~~ PD is supplied with $V_{Port_PSE-2P\ min}$ to $V_{Port_PSE-2P\ max}$ with R_{Ch} (as defined in Table 33–1) in series, [it shall operate at \$P_{Port_PD}\$ shall as defined in Table 33-28 with the ripple and noise content as defined in Table 33-28 and with the DC input operating voltage range as defined by Table 33-28.](#) ~~be defined as shown in Equation (33–23):~~

$$P_{Port_PD} = \{V_{Port_PD-x} I_{Port}\}_w \quad (33-23)$$

where

~~V_{Port_PD} is the static input voltage at the PD PI~~

~~I_{Port} is the input current, either DC or RMS~~

When a dual-signature PD is supplied with $V_{Port_PSE-2P\ min}$ to $V_{Port_PSE-2P\ max}$ with R_{Ch} (as defined in Table 33–1) in series, [it shall operate at \$P_{Port_PD-2P}\$ shall as defined in Table 33-28 with the ripple and noise content as defined in Table 33-28 and with the DC input operating voltage range as defined by Table 33-28.](#) ~~be defined as shown in Equation (33–24):~~

$$P_{Port_PD-2P} = \{V_{Port_PD-2P-x} I_{Port-2P}\}_w \quad (33-24)$$

where

~~V_{Port_PD-2P} is the static input voltage over the pairset as defined in Table 33–28~~

~~$I_{Port-2P}$ is the current on a pairset as defined in 33.2.8.4~~

~~NOTE~~— When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.