33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with $V_{port\_PD\text{-}2P}$ requirements as defined in Table 33–28, and ending when ~~C_{Port}~~ the PD input voltage has reached ~~a~~99% of steady state ~~and is charged to 99% of its final value~~. This period shall be less than $T_{Inrush\text{-}2P}$ min per Table 33–17, with the PSE minimum inrush behavior defined in 33.2.8.5. ~~Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay\ 2P}$ min, Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay\ 2P}$ min. This allows the PSE to properly complete inrush.~~

~~Editor's Note: This paragraph needs further review as the requirement to charge the capacitor does not apply to PDs that limit their inrush current.~~

Editor's Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277.

$T_{delay\text{-}2P}$ for each pairset starts when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to change the available current on each pairset from $I_{Inrush\text{-}2P}$ to $I_{Con\text{-}2P}$.

C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port\text{-}2P}$ in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–37 for a simplified PSE-PD C_{Port} and $C_{Port\text{-}2P}$ interpretation model.

Input inrush currents at startup, I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, as defined in Table 33–17, are limited by the PSE if C_{Port} < 180 µF for single-signature PDs assigned to Class 0 to 6, and if C_{Port} < 360 µF for PDs assigned to Class 7 or 8. Input inrush current at startup, $I_{Inrush\_PD\text{-}2P}$, is limited by the PSE if $C_{Port\text{-}2P}$ < ~~180~~ 110 µF for dual-signature Type 3 PDs~~.~~ and if $C_{Port\text{-}2P}$ < 180 µF for dual-signature Type 4 PDs. If the PSE is limiting input inrush current, C_{Port} shall be charged to 99% of its final value within $T_{Inrush\text{-}2P}$. If the PSE is limiting input inrush current, PDs shall conform to either I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, or I_{Con} and $I_{Con\text{-}2P}$, whichever is lower, between $T_{Inrush\text{-}2P}$ min and $T_{delay\text{-}2P}$.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush\text{-}2P}$ min. See 33.2.8.4 for details.

If a PD has a larger C_{Port} or $C_{Port\text{-}2P}$ value, then the PD shall limit the input inrush current to either I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, or I_{Con} and $I_{Con\text{-}2P}$, whichever is lower, for at least $T_{delay\text{-}2P}$ per Table 33–28, with the PSE minimum inrush behavior defined in 33.2.8.5.~~such that I_{Inrush_PD} max and $I_{Inrush\_PD\ 2P}$ max, as defined in Table 33–17, are met.~~ PDs limiting input inrush current may extend inrush beyond $T_{delay\text{-}2P}$. PDs limiting input inrush current should consume a lower DC load current value to guarantee positive charging current into C_{Port}.

~~C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. C_{Port_2P} in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–37 for a simplified PSE-PD C_{Port} and C_{Port_2P} interpretation model.~~