33.3.7.3 – PD Input Inrush Current

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Problem Statements

- PD inrush requirements section has become fragmented, creating conflicting requirements and unclear behaviors
  - Requirement conflict between
    - PD Inrush Current ($I_{Inrush\text{-}2P}$)
    - PD Inrush Power (*"shall consume a maximum of xyz power…"*)
  - Unclear behavior for PD-controlled inrush
    - C_{Port} "charged to 99%" vs PD-controlled inrush
  - Unclear behavior for PSE and PD-controlled inrush
    - I_{Con}, $I_{Con\text{-}2P}$ vs $I_{Inrush(\_PD)}$, $I_{Inrush\_(PD)\text{-}2P}$

Presentation Objectives

- Create an implementable set of rules
  - Clean up inconsistencies
  - Improve clarity
- Clearly sort requirements into
  - Definitions
    - $T_{Inrush-2P}$
    - $T_{delay-2P}$
    - C_{Port}, $C_{Port-2P}$
  - PD requirements for…
    - PSE-controlled Inrush
    - PD-controlled Inrush

Original 802.3at PD Inrush Text

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99 % of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Definition of T_{Inrush}

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Definition of T_{delay}

Input inrush current at startup is limited by the PSE if C_{Port} < 180 µF, as specified in Table 33–11.

PSE-controlled Inrush

If C_{Port} ≥ 180 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

PD-controlled Inrush

Proposed Solution

- Reinstate 33.3.7.3 template per 802.3-2012
  - Definition and explanation of $T_{Inrush-2P}$
  - Definition and explanation of $T_{delay-2P}$
  - New to bt: Definitions of C_{Port}, $C_{Port-2P}$
  - Conditions for PSE-controlled inrush
    - New to bt: Note regarding PSE transition from POWER_UP into POWER_ON state
  - Conditions for PD-controlled inrush

Proposed Solution: Paragraph #1, $T_{Inrush-2P}$

- Definition and explanation of $T_{Inrush-2P}$
  - Decouple $T_{Inrush-2P}$ from "C_{Port} charged to 99%"
    - Allow PD-controlled inrush to extend beyond $T_{Inrush-2P}$, $T_{delay-2P}$
  - Move $T_{delay-2P}$ requirements into PSE- and PD-controlled inrush requirements
    - $T_{delay-2P}$ requirements differ, depending on who controls inrush

Proposed Solution: Paragraph #1, $T_{Inrush-2P}$

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{port_PD-2P} requirements as defined in Table 33–28, and ending when ~~C_{Port}~~ the PD input voltage has reached ~~a~~99% of steady state ~~and is charged to 99% of its final value~~. This period shall be less than $T_{Inrush-2P}$ min per Table 33–17, with the PSE minimum inrush behavior defined in 33.2.8.5. ~~Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay-2P}$ min, Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay-2P}$ min. This allows the PSE to properly complete inrush.~~

Decouple T_{Inrush} from requirement that C_{Port} shall be charged.

Note 1: For PSE-controlled inrush, this requirement is preserved in the PSE-controlled inrush paragraph.

Note 2: This is identical text to existing note in 33.3.7.3, regarding PSE transition from POWER_UP to POWER_ON.

$T_{delay-2P}$ requirements are moved to PSE- and PD-controlled inrush.

Statement about PSE properly completing inrush is removed; “PD input voltage to 99% within $T_{Inrush-2P}$” is not the only requirement for PSE to properly complete inrush.

Proposed Solution: Paragraph #2, $T_{delay-2P}$

- Definition and explanation of $T_{delay-2P}$
  - Fix typographical error

Proposed Solution: Paragraph #2, $T_{delay-2P}$

$T_{delay-2P}$ for each pairset starts when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to change the available current on each pairset from $I_{Inrush-2P}$ to I_{Con-2P}.

Added a missing word

Proposed Solution: Paragraph #3, C_{Port} and $C_{Port-2P}$

- Move definitions of C_{Port}, $C_{Port-2P}$
  - Definitions of C_{Port} and $C_{Port-2P}$ should precede usage (PSE- and PD-controlled inrush paragraphs)

Proposed Solution: Paragraph #3, C_{Port}

C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port-2P}$ in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–37 for a simplified PSE-PD C_{Port} and $C_{Port-2P}$ interpretation model.

No text is changed within C_{Port} paragraph.

Proposed Solution: Paragraph #4, PSE-controlled Inrush

- Conditions for PSE-controlled inrush
  - Maintain "C_{Port} charged to 99%" requirement for PSE-controlled inrush
  - Define PD $T_{delay\text{-}2P}$ requirement
    - For PSE-controlled inrush, this is the time period between…
      - The minimum time at which the PSE may inspect "power_applied" ($T_{Inrush\text{-}2P}$ min), and,
      - The minimum time at which the PD may transition to MDI_POWER2 ($T_{delay\text{-}2P}$ min)

Proposed Solution: Paragraph #4, PSE-controlled Inrush

Input inrush currents at startup, I_{Inrush_PD} and I_{Inrush_PD-2P}, as defined in Table 33–17, are limited by the PSE if C_{Port} < 180 µF for single-signature PDs assigned to Class 0 to 6, and if C_{Port} < 360 µF for PDs assigned to Class 7 or 8. Input inrush current at startup, I_{Inrush_PD-2P}, is limited by the PSE if $C_{Port-2P}$ < ~~180~~110 µF for dual-signature Type 3 PDs~~.~~ and if $C_{Port-2P}$ < 180 µF for dual-signature Type 4 PDs. If the PSE is limiting input inrush current, C_{Port} shall be charged to 99% of its final value within $T_{Inrush-2P}$. If the PSE is limiting input inrush current, PDs shall conform to either I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, between $T_{Inrush-2P}$ min and $T_{delay-2P}$.

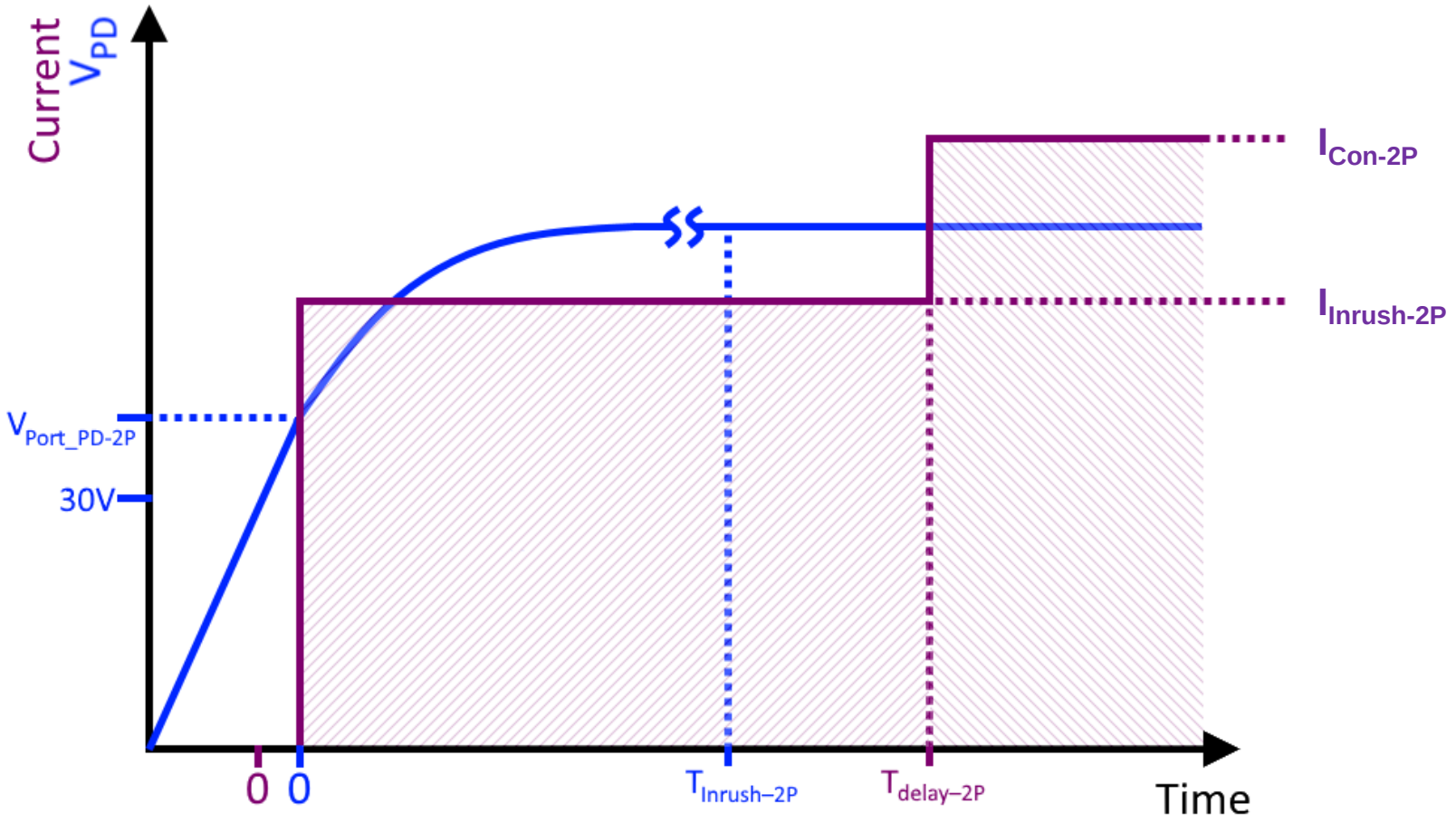
Update threshold for PSE-controlled inrush, to reflect changes in Tables 33–17 and 33–28 from D1.7.

Preserve legacy guarantee: For PSE-controlled inrush, C_{Port} shall be charged to 99% of final value within $T_{Inrush-2P}$.

Enforce requirements:

- PD is not allowed to transition into a high-power state prior to $T_{delay-2P}$.
- PD is not allowed to draw more current than its continuous current allocation (see “pd_max_power” usage, 33.3.3.5)

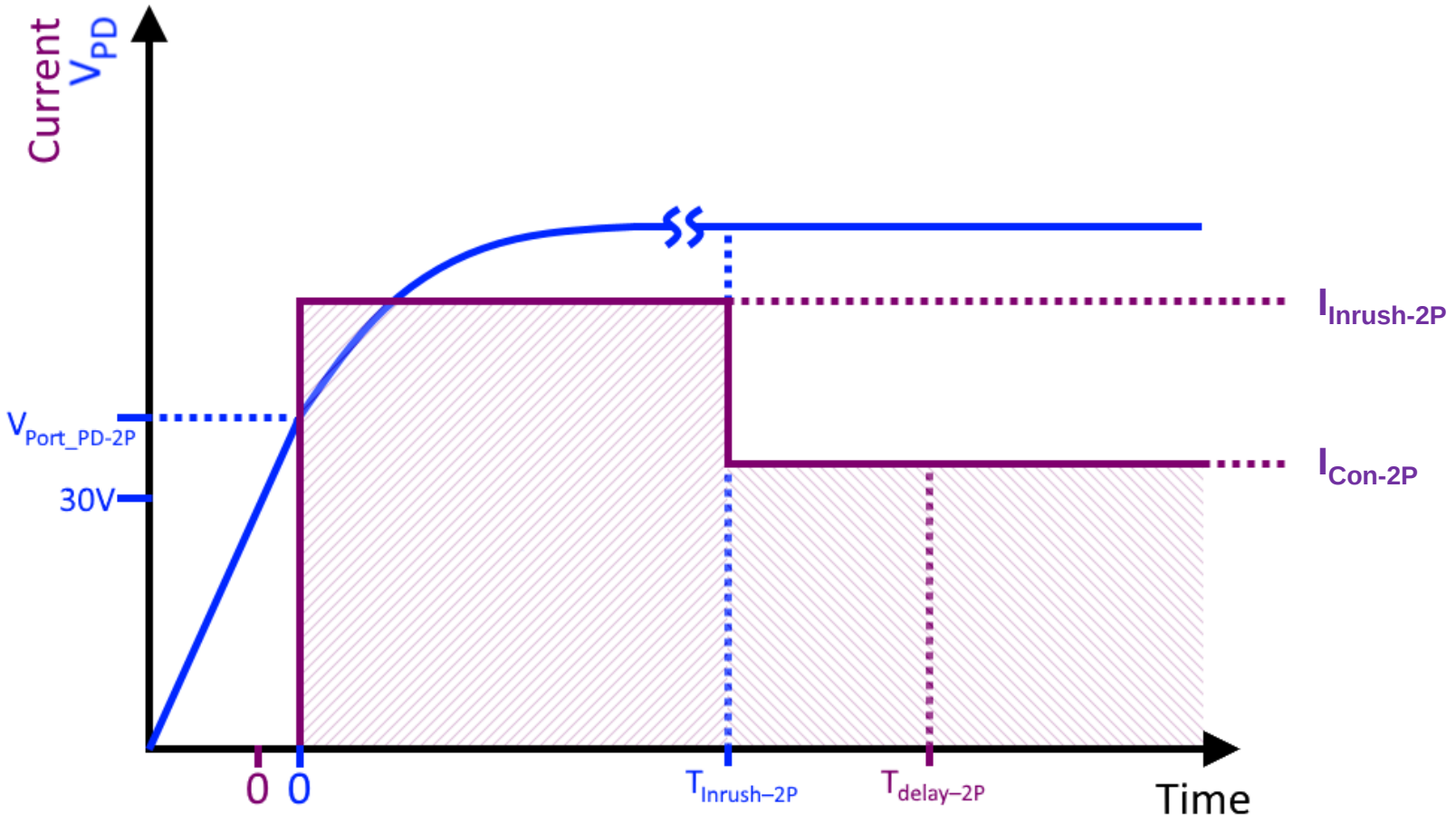
PSE-controlled Inrush: “Whichever is lower”



Consider the example case of PSE-controlled inrush where I_{Con-2P} is **greater than** $I_{Inrush-2P}$, such as a Class 6 single-signature PD.

- PSE-controlled inrush means current at PD PI can reach $I_{Inrush-2P}$ for $T_{Inrush-2P}$
- PDs shall conform to I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, between $T_{Inrush-2P}$ min and $T_{delay-2P}$.

PSE-controlled Inrush: “Whichever is lower”



Consider the example case of PSE-controlled inrush where I_{Con-2P} is **less than** $I_{Inrush-2P}$, such as a Class 1 single-signature PD.

- PSE-controlled inrush means current at PD PI can reach $I_{Inrush-2P}$ for $T_{Inrush-2P}$
- PDs shall conform to I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, between $T_{Inrush-2P}$ min and $T_{delay-2P}$.

Proposed Solution: Paragraph #5, NOTE

- NOTE regarding PSE transition from POWER_UP into POWER_ON state

Proposed Solution: Paragraph #5, NOTE

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush-2P}$ min. See 33.2.8.4 for details.

No text is changed within NOTE paragraph.

Proposed Solution: Paragraph #6, PD-controlled Inrush

- Conditions for PD-controlled inrush
  - Allow PD-controlled inrush period to extend beyond $T_{Inrush-2P}$, $T_{delay-2P}$
    - Requirements in Table 33–28, 33.2.8.5 maintained
  - Maintain PD-controlled inrush requirement that PD shall limit to I_{Inrush_PD-2P} or I_{Con-2P}, whichever is lower
  - Add note to alert PD designer that C_{Port} should have positive charging current

Proposed Solution: Paragraph #6, PD-controlled Inrush

If a PD has a larger C_{Port} or $C_{Port-2P}$ value, then the PD shall limit the input inrush current to either I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, for at least $T_{delay-2P}$ per Table 33–28, with the PSE minimum inrush behavior defined in 33.2.8.5. PDs limiting input inrush current may extend inrush beyond $T_{delay-2P}$. PDs limiting input inrush current should consume a lower DC load current value to guarantee positive charging current into C_{Port}.

Enforce requirements:

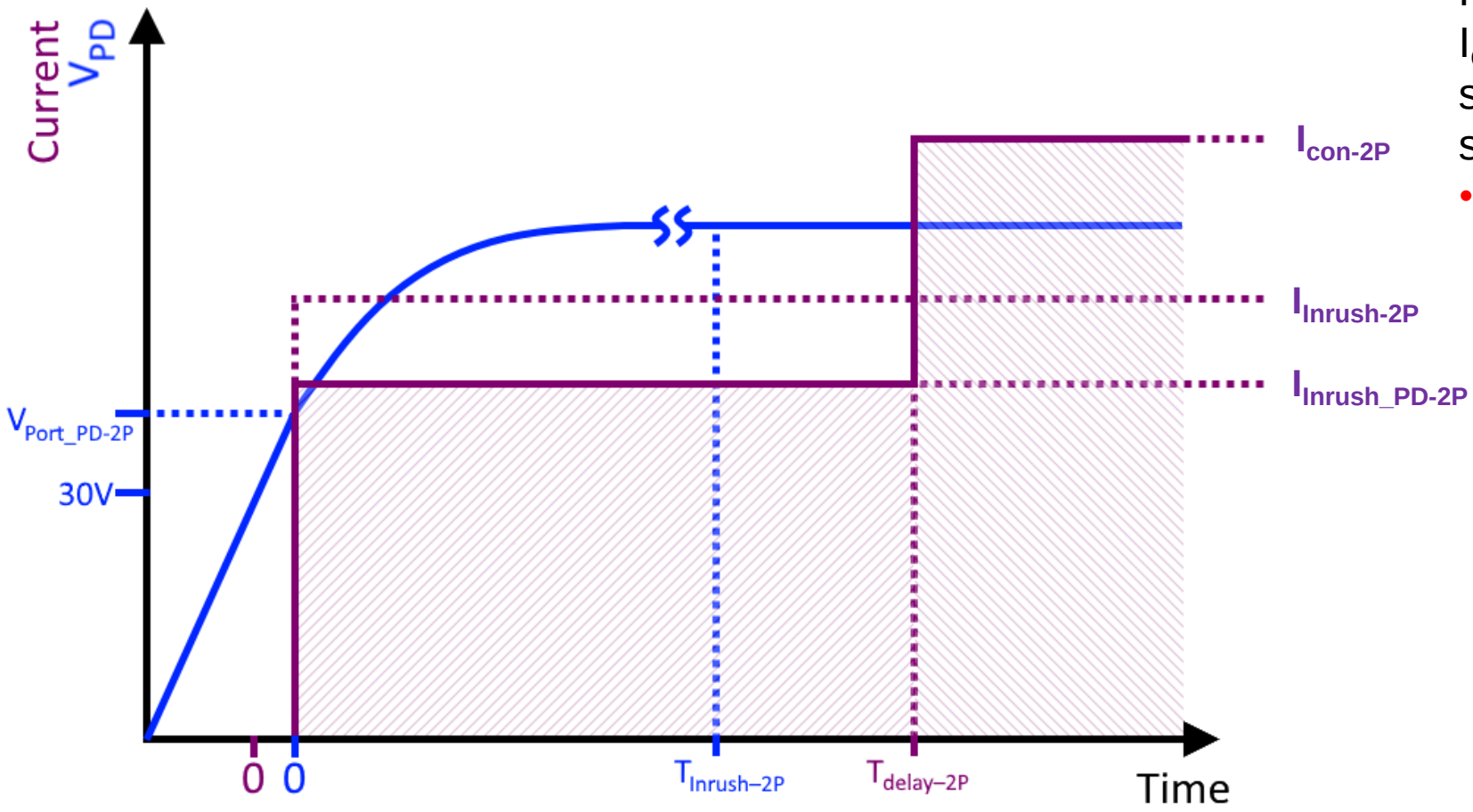
- PD is not allowed to transition into a high-power state prior to $T_{delay-2P}$.
- PD is not allowed to draw more current than its continuous current allocation (see “pd_max_power” usage, 33.3.3.5)

Reference from Table 33–17 is updated to Table 33–28, where PD-controlled inrush requirements live.

Explicitly state that PD-controlled inrush beyond $T_{delay-2P}$ is allowed.

Alert the PD designer that, in the case of PD-controlled inrush, headroom above DC load current is required to allow positive charging current into C_{Port}.

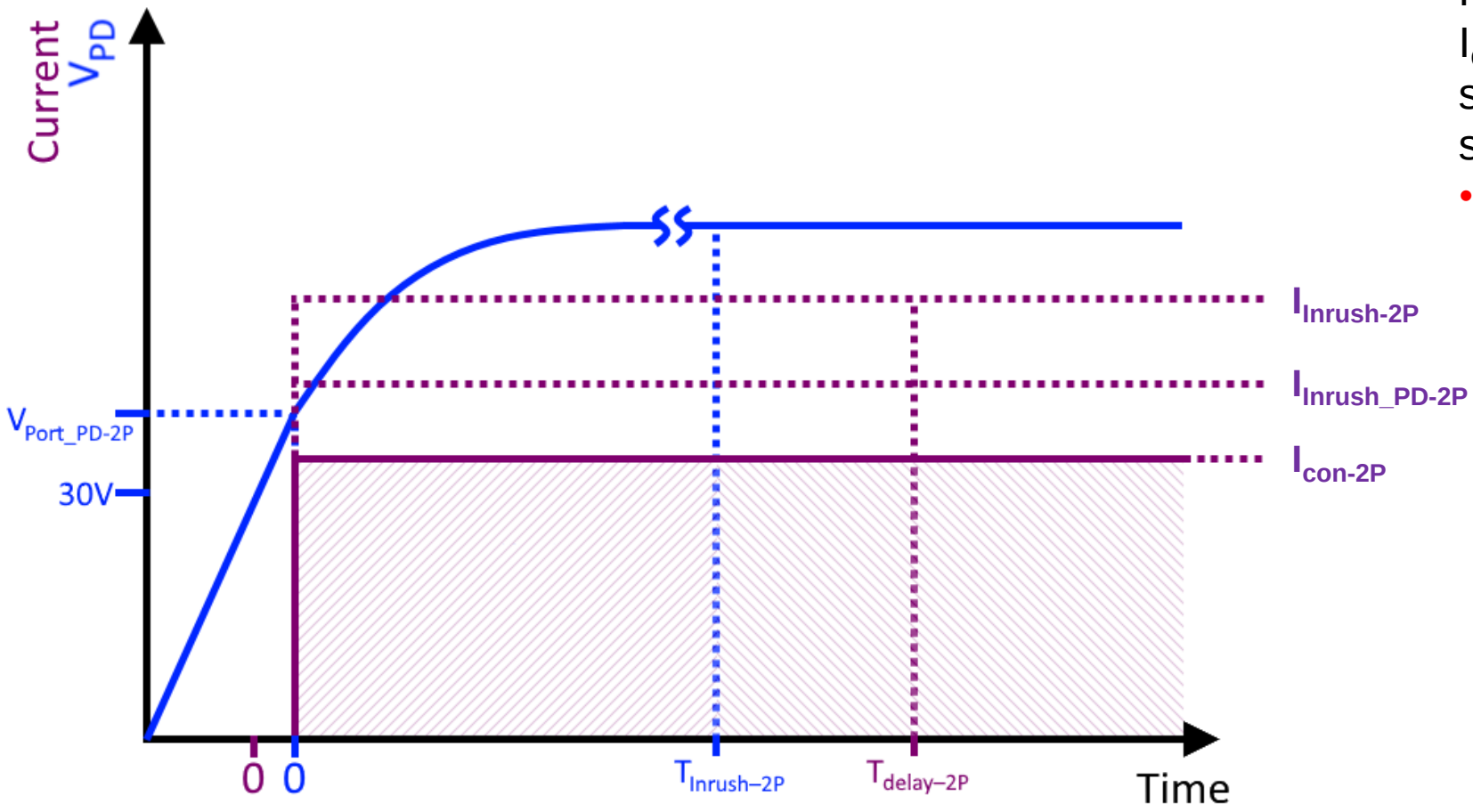
PD-controlled Inrush: “Whichever is lower”



Consider the example case of PD-controlled inrush where I_{Con-2P} is **greater than** $I_{Inrush-2P}$, such as a Class 6 single-signature PD.

- “…the PD shall limit the input inrush current to either I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, for $T_{delay-2P}$…”

PD-controlled Inrush: “Whichever is lower”



Consider the example case of PD-controlled inrush where I_{Con-2P} is **less than** $I_{Inrush-2P}$, such as a Class 1 single-signature PD.

- “…the PD shall limit the input inrush current to either I_{Inrush_PD} and I_{Inrush_PD-2P}, or I_{Con} and I_{Con-2P}, whichever is lower, for $T_{delay-2P}$…”

Questions?

Annex: Conflicting Power Requirements

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- Upon review of the requirements outlined in Paragraph #1, we see
  - Explicit requirement on the PD and PSE to limit based on a constant current requirement, $I_{Inrush\_PD\text{-}2P}$
    - These explicit requirements imply a symmetric power limit on the PSE and PD
  - Explicit constant power requirement on the PD (*"Shall consume a maximum of xyz power")*
    - This explicit requirement defines a unilateral maximum power threshold for the PD

Annex: Conflicting Power Requirements

- Constant current and constant power requirements are in conflict
  - In some cases, the PD is allowed more power than the PSE is guaranteed to provide
  - In many cases, the PD is denied power that the PSE is required to provide

802.3bt – PD Inrush Requirements: Breakdown

- Inrush current is drawn during the startup period beginning with the application of input voltage to the PI compliant with V_{port_PD-2P} requirements as defined in Table 33–28, and ending when C_{Port} has reached a steady state and is charged to 99% of its final value.
- This period shall be less than $T_{Inrush-2P}$ min per Table 33–17, with the PSE minimum inrush behavior defined in 33.2.8.5.
- Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay-2P}$ min. Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay-2P}$ min.
- This allows the PSE to properly complete inrush.

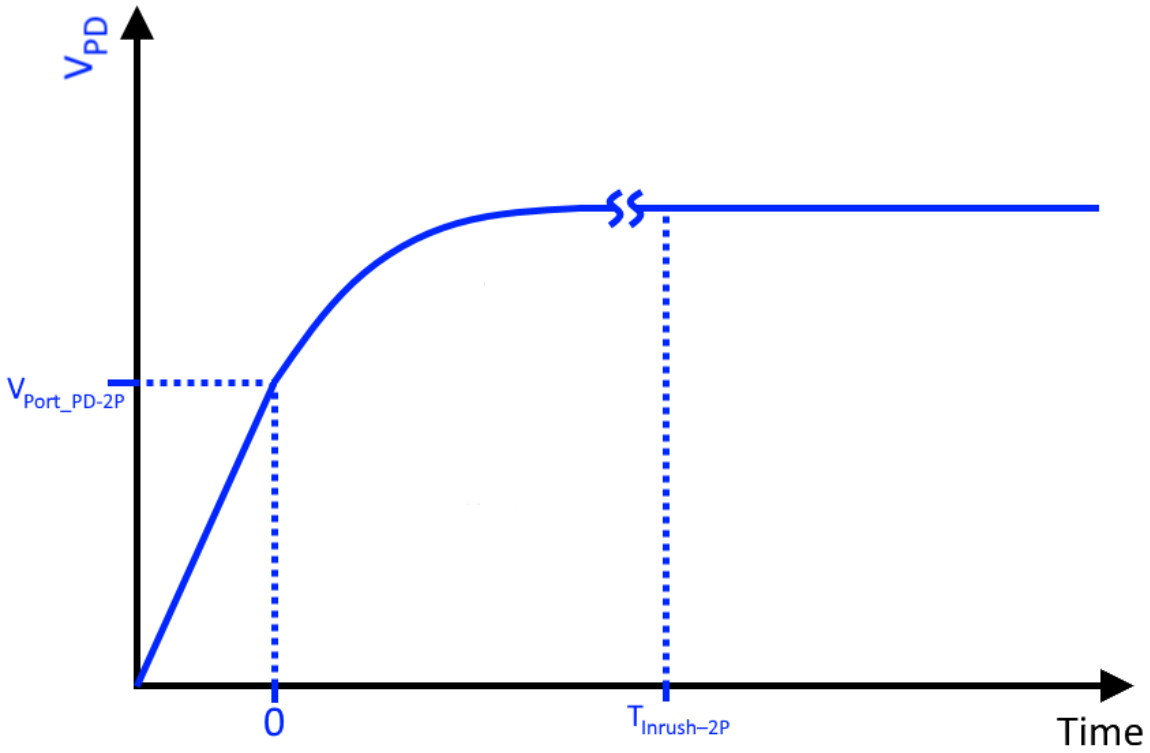
Legacy Text

$T_{delay-2P}$
(used before it is defined)

New text in 802.3bt

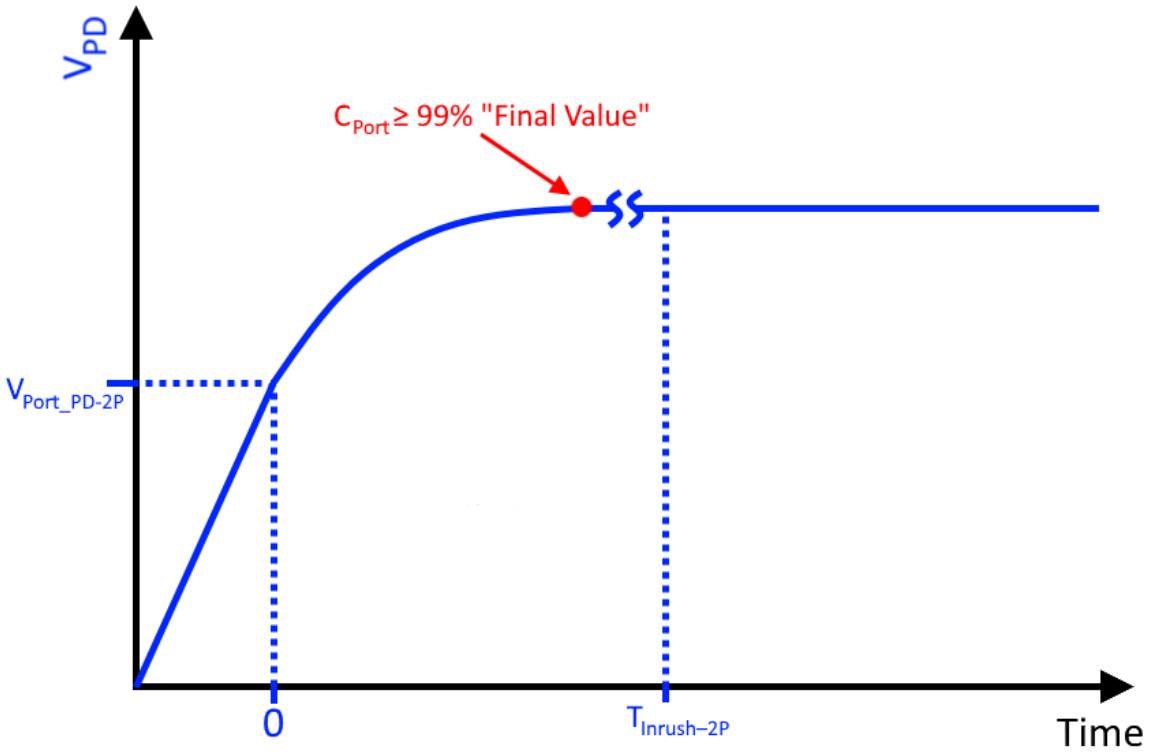
802.3bt – PD Inrush Requirements: Breakdown

- Inrush current is drawn during the startup period beginning with the application of input voltage to the PI compliant with $V_{port\_PD\text{-}2P}$ requirements as defined in Table 33–28, and ending when C_{Port} has reached a steady state and is charged to 99% of its final value.



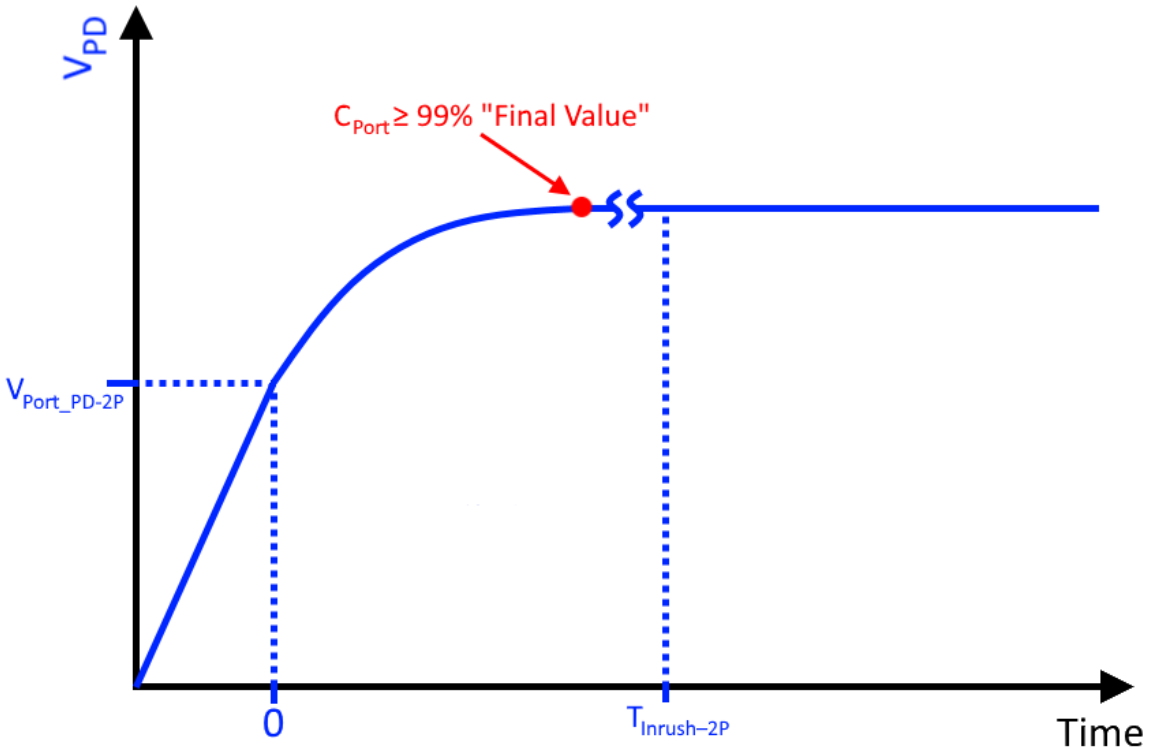
802.3bt – PD Inrush Requirements: Breakdown

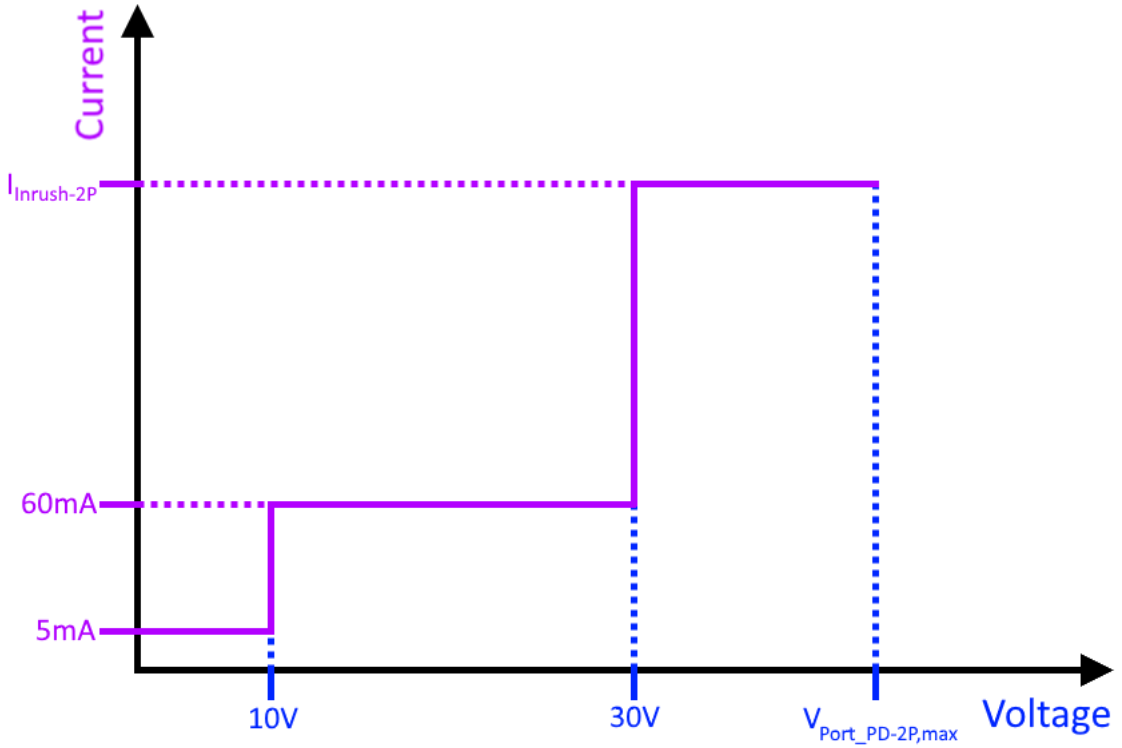
- **This period shall be less than $T_{Inrush-2P}$ min per Table 33–17...**



802.3bt – PD Inrush Requirements: Breakdown

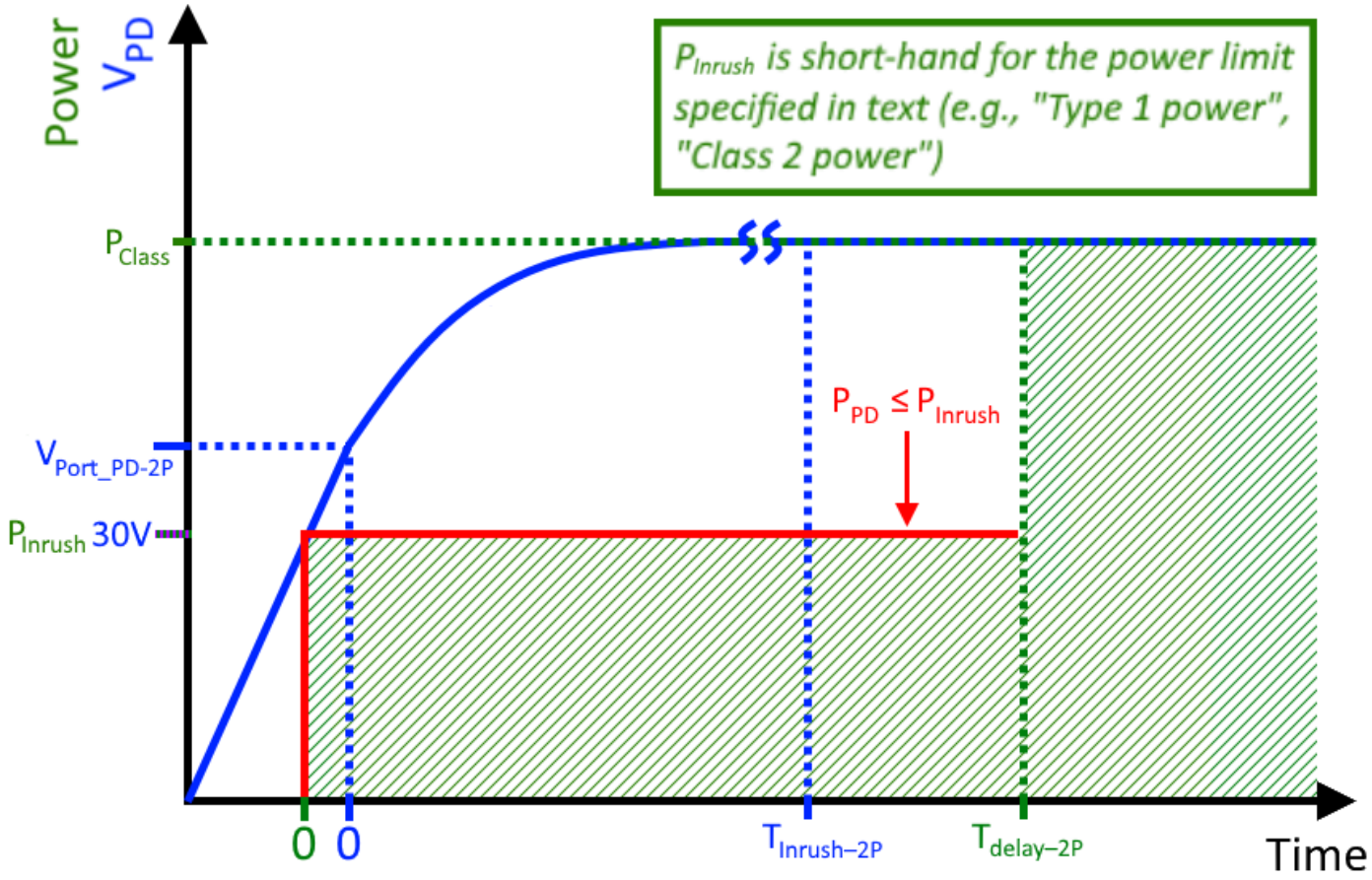
- This period **shall** be less than $T_{Inrush-2P}$ min per Table 33–17, **with the PSE minimum inrush behavior defined in 33.2.8.5.**





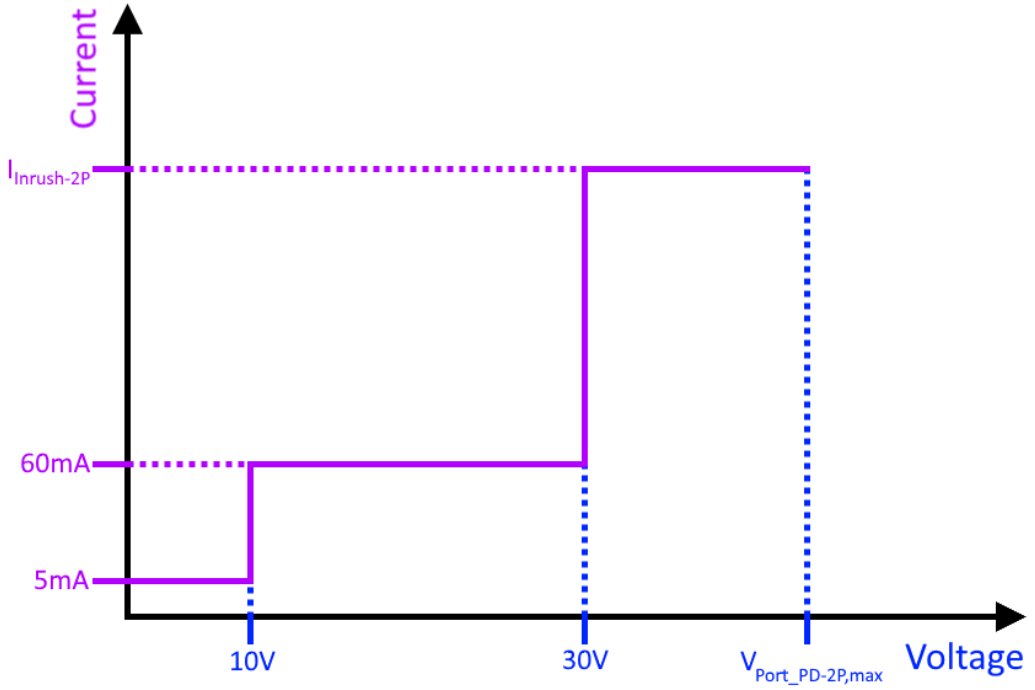
802.3bt – PD Inrush Requirements: Breakdown

- Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay-2P}$ min. Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay-2P}$ min.

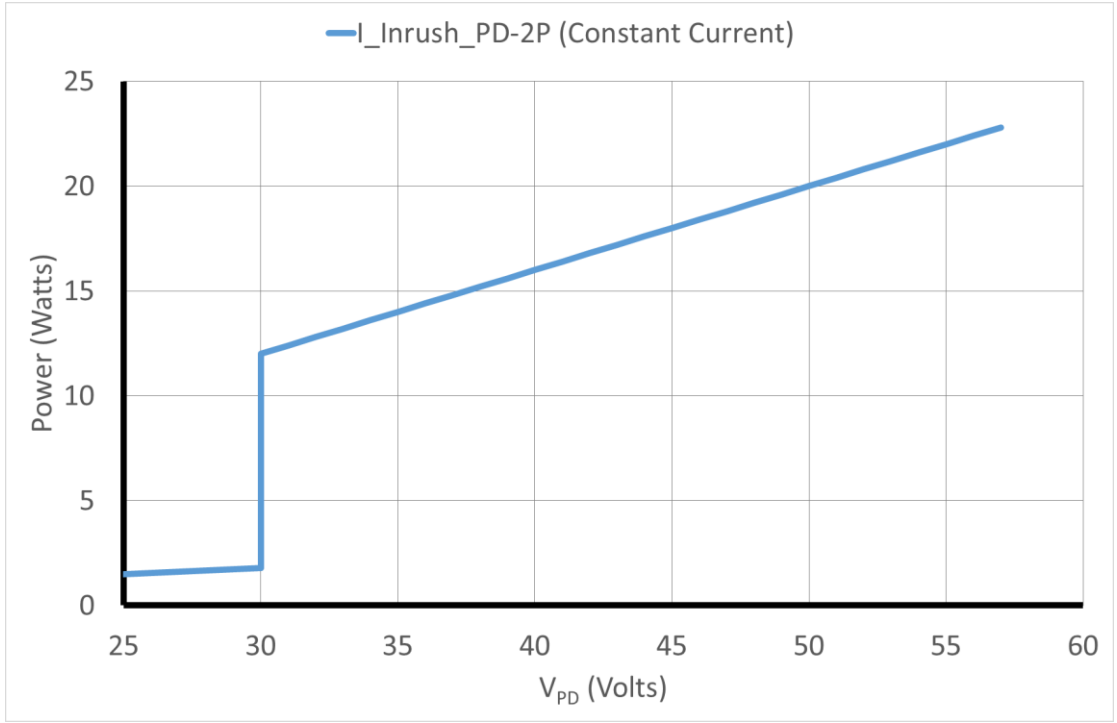


802.3bt – PD Inrush Requirements: Conflict

- This period **shall** be less than $T_{Inrush-2P}$ min per Table 33–17, **with the PSE minimum inrush behavior defined in 33.2.8.5.**
- Example case:
  - Type 3 PD
    - PSE Requirement: **$I_{Inrush-2P}$ min = 400mA**
    - PD Requirement (PD-controlled inrush): **I_{Inrush_PD-2P} max = 400mA**



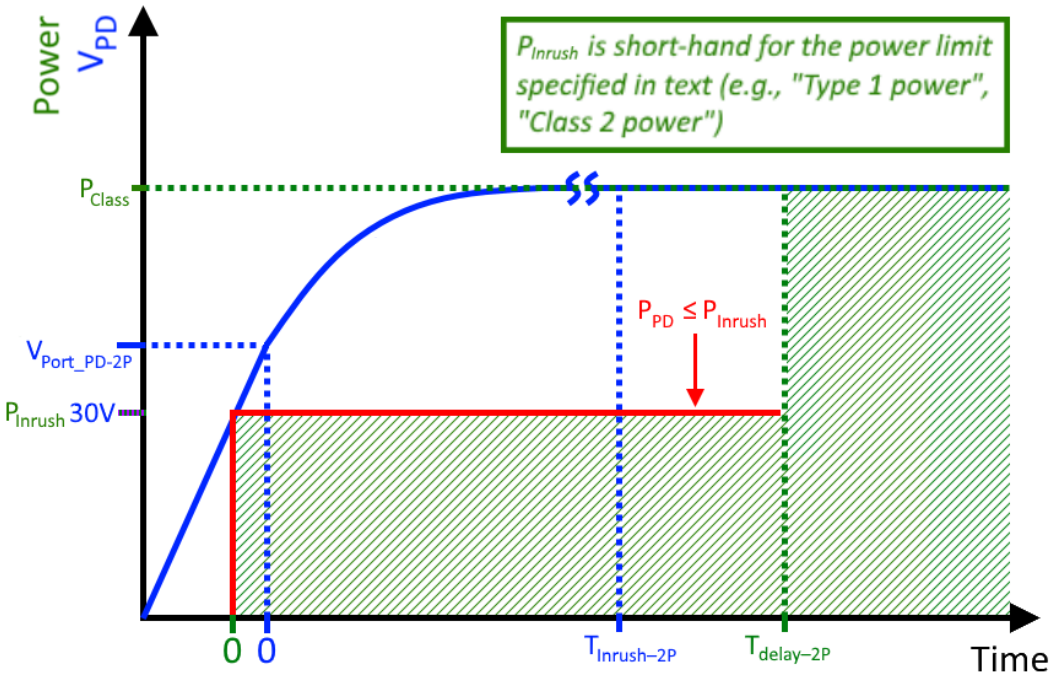
Explicit I/V Requirements

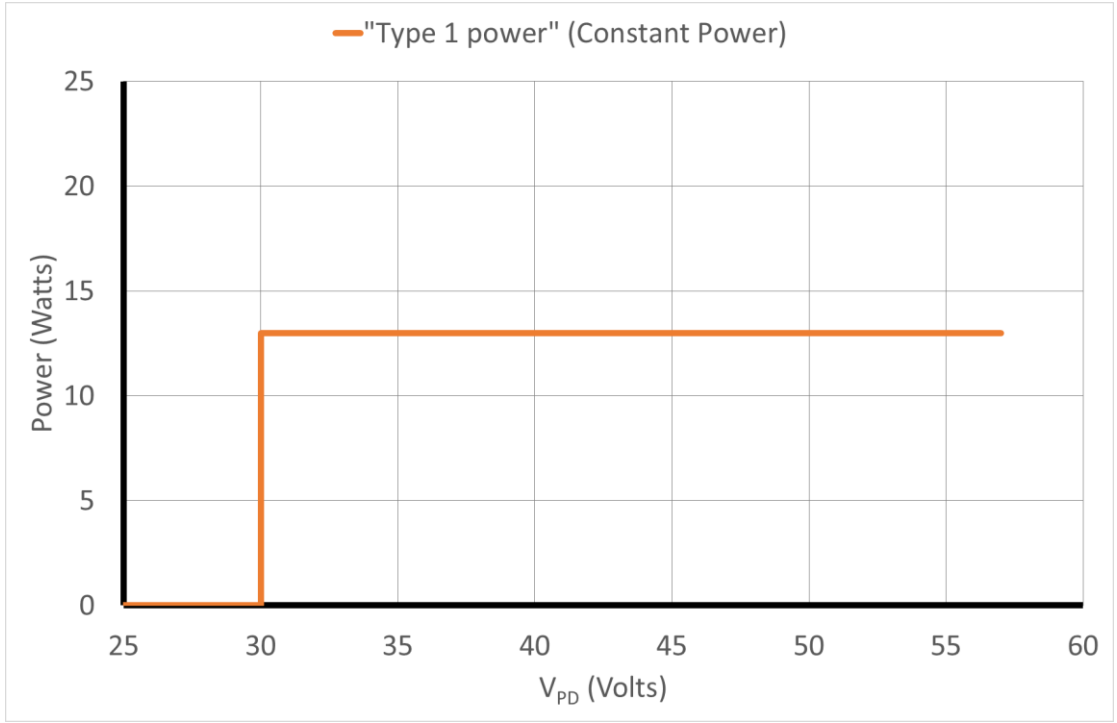


Implicit Power Requirements

802.3bt – PD Inrush Requirements: Conflict

- Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay-2P}$ min. Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay-2P}$ min.
- **Same example case:**
  - Type 3 PD
    - PD Requirement: **"Type 1 power" max = 13W**

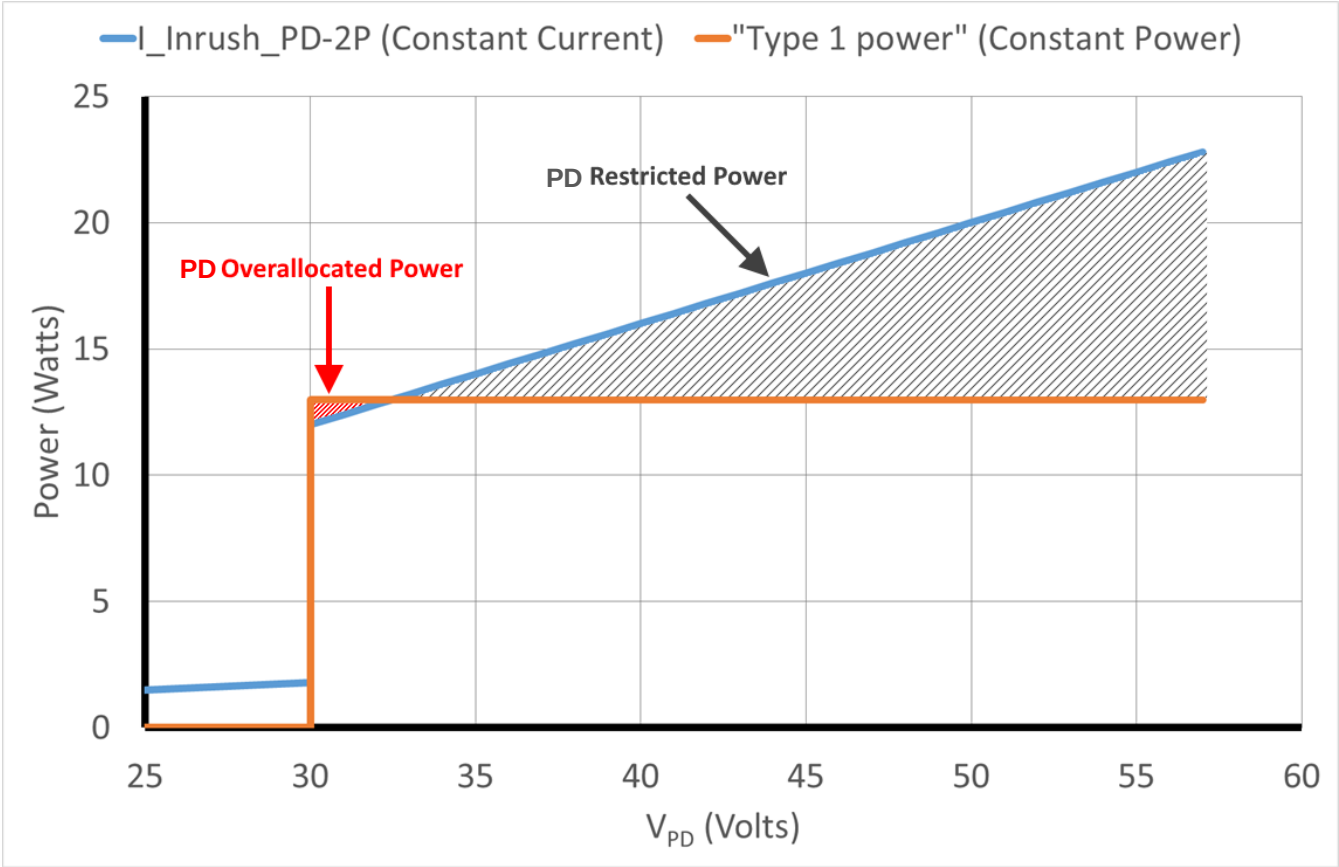




Explicit Power Requirements

802.3bt – PD Inrush Requirements: Combined

- "Type 1 power" requirement for our example case (Type 3 PD)
  - **Allocates PD power budget higher than PSE minimum at low voltage**
  - Restricts PD power budget beneath PSE guaranteed minimum and PD maximum ($I_{Inrush-2P}$, I_{Inrush_PD-2P}) at high voltage



802.3bt – PD Inrush Requirements: Combined

- "Class 2 power" requirement for another example case (Type 4 DS PD)
  - Restricts PD power budget deeply beneath $I_{Inrush-2P}$, I_{Inrush_PD-2P} at high voltage
  - Contrast with PSE requirement in 33.2.8.5.1 where Class 2 is power allocation to internal load component of PD
    - Here Class 2 power is specified for "total PD power consumption" i.e. at PD PI