Introduction text for the Clause 33 state diagrams v120

33.2.5 PSE state diagrams

Type 1 and Type 2 PSEs shall provide the behavior of the state diagrams shown in Figure 33–13 and Figure 33–14. Type 3 and Type 4 PSEs shall provide the behavior of the state diagrams shown in Figure 33–15 to Figure 33–23.

Editor's Note: Names used for state diagrams apply to the section where they are defined. Any names used in both, particularly names referenced in the text, should be checked for implications.

33.2.5.1.1 Type 3 and Type 4 specific overview and timing

Connection Check timing requirements are specified in Table 33–7. Detection timing requirements are specified in Table 33–8. Classification timing requirements are specified in Table 33–15. Autoclass timing requirements are specified in Table 33–16. Power turn-on timing requirements are specified in Table 33–17.

In the Type 3 and Type 4 state diagram, Alternative A and Alternative B are depicted as serving distinct roles during 4-pair operation. In any implementation, the behaviors of the Alternatives may be reversed as long as the roles are established in IDLE and shall be maintained in every other state. In the state diagram, the alternatives are named the Primary Alternative and the Secondary Alternative.

> **Info (not part of baseline)**
>
> The Figure numbering for the PSE state machine has become a bit confused. Here is how it would make sense:

Change Figure numbering as in Table below:

Description	D1.7 page	Updated Figure number
Top level	page 79	Figure 33–15
Top level	page 80	Figure 33–15 (continued)
Top level	page 81	Figure 33–15 (continued)
Primary Alt	page 82	Figure 33–16
Primary Alt	page 83	Figure 33–16 (continued)
Secondary Alt	page 84	Figure 33–17
Secondary Alt	page 85	Figure 33–17 (continued)
Single-signature classification	page 86	Figure 33–18
Dual-signature classification Primary Alt	page 87	Figure 33–19
Dual-signature classification Secondary Alt	page 88	Figure 33–20
MPS	page 89	Figure 33–21
Inrush	page 89	Figure 33–22

Remove the Editor's Note (D1.7, p57, line 1) and append the following at the end of 33.2.5.1.1:

The state diagram consists of multiple state diagrams that operate concurrently. Depending on the connected PD being identified as single-signature or dual-signature, the state diagram operates in a different manner. The top level state diagram consists of Figure 33–15.

If the connected PD is identified as single-signature, the top level state diagram, as defined in Figure 33–15, as well as the single-signature classification diagram in Figure 33–18 are active.

If the connected PD is identified as dual signature, the top level state diagram will proceed to the SISM_START state and remain in that state, at which point the semi-independent state diagrams for the Primary and Secondary pairset become active. The dual-signature semi independent state diagram is defined in Figure 33–16 and Figure 33–17 for the Primary and Secondary Alternative respectively. Dual signature classification is defined in Figure 33–19 and 33–20 for the Primary and Secondary Alternative respectively.

Monitoring of MPS and inrush is handled by Figure 33–21 and Figure 33–22 respectively.

33.2.5.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5. In addition a precedence order for operators is established in Table 33–N1. Operators of equal precedence are evaluated left-to-right. Operator precedence in qualifiers is a local convention for this Clause.

Insert Table 33–N1 as follows

Operator	Meaning
( )	Indicates precedence
$<,\leq,>,\geq,=,\neq$	Less than, less than or equal to, greater than, greater than or equal to, equals, not equals
!	Boolean NOT
*	Boolean AND
^	Boolean XOR
+	Boolean OR
$\Leftarrow$	Assignment operator

Table 1: Table 33–N1 — PSE state diagram operator precedence, highest precedence at the top

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in ~~21.5~~ 33.2.5.2.

33.6.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in ~~21.5~~ 33.2.5.2.

> **Info (not part of baseline)**
>
> The final page of this PDF contains the complete state overview of the D1.7 PSE state diagram. Branch logic is not shown. The colors denote on which Figure/Page the respective states are located. It is not baseline.