Dual-signature MPS state diagram v132

> **Info (not part of baseline)**
>
> The Type 3/Type 4 state diagram depends on tmpdo_timer_pri and _sec for dual-signature MPS operation, but these timers are never started or stopped. The state diagram duplicates the logic described in 33.2.10.1.2, there is no need for this. Both implementation options (monitoring the pairset with the highest current, or monitoring the total amount of current of both pairsets) are supported by mr_mps_valid.
>
> The state machine now only handles the timing aspect of MPS. Whether or not MPS is absent or present is handled by 33.2.10.1.2.

33.2.5.9 Type 3 and Type 4 variables

Remove variable 'mps_sum'.

mr_mps_valid

> The PSE monitors the Maintain Power Signature (MPS, see 33.2.10.1). This variable indicates the presence or absence of a valid MPS, when the connected PD is a single-signature PD, or the PSE is operating in 2-pair mode.
> Values:
>
> > FALSE: MPS is absent.
> > TRUE: MPS is present.

mr_mps_valid_pri

> The PSE monitors the Maintain Power Signature (MPS, see 33.2.10.1) on the Primary Alternative. This variable indicates the presence or absence of a valid MPS on the Primary Alternative, when the connected PD is a dual-signature PD.
> Values:
>
> > FALSE: MPS is absent.
> > TRUE: MPS is present.

mr_mps_valid_sec

> The PSE monitors the Maintain Power Signature (MPS, see 33.2.10.1) on the Secondary Alternative. This variable indicates the presence or absence of a valid MPS on the Secondary Alternative, when the connected PD is a dual-signature PD.
> Values:
>
> > FALSE: MPS is absent.
> > TRUE: MPS is present.

33.2.5.12 Type 3 and Type 4 state diagrams

Replace Figure 33–22 as follows:

!(pwr_app_pri + pwr_app_sec)

IDLE_MPS

stop tmpdo_timer

pwr_app_pri + pwr_app_sec

MONITOR_MPS

stop tmpdo_timer

!mr_mps_valid

DETECT_MPS
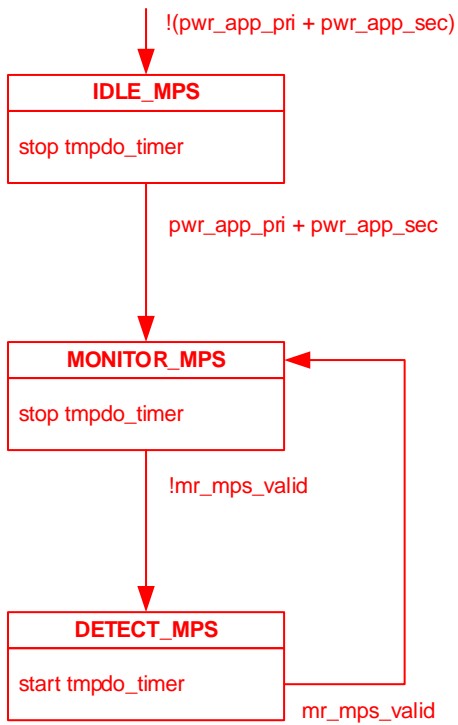
start tmpdo_timer

mr_mps_valid

Figure 33–22 — Type 3 and Type 4 PSE MPS monitor state diagram for single-signature PDs or 2-pair operation
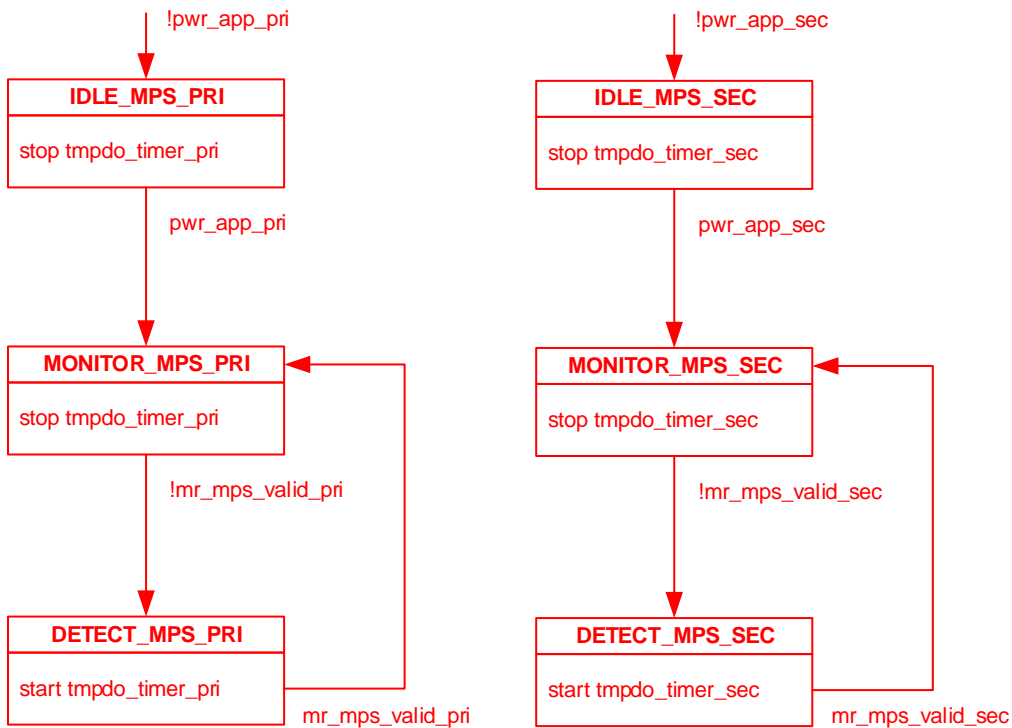
Insert new Figure after Figure 33–22 as follows:

!pwr_app_pri

IDLE_MPS_PRI

stop tmpdo_timer_pri

pwr_app_pri

MONITOR_MPS_PRI

stop tmpdo_timer_pri

!mr_mps_valid_pri

DETECT_MPS_PRI

start tmpdo_timer_pri

mr_mps_valid_pri

!pwr_app_sec

IDLE_MPS_SEC

stop tmpdo_timer_sec

pwr_app_sec

MONITOR_MPS_SEC

stop tmpdo_timer_sec

!mr_mps_valid_sec

DETECT_MPS_SEC

start tmpdo_timer_sec

mr_mps_valid_sec

Figure 33–23 — Type 3 and Type 4 PSE MPS monitor state diagram for dual-signature PDs

33.2.10.1.2 PSE DC MPS component requirements

> **Info (not part of baseline)**
>
> Let's specifically state in this section that MPS absence or presence is to be stored in mr_mps_valid, mr_mps_valid_pri and mr_mps_valid_sec. Also, Harvard comma.

A PSE, depending on the connected Type of PD, shall use the applicable I_{Hold} min, I_{Hold} max, $I_{Hold-2P}$ min, $I_{Hold-2P}$ max, T_{MPS}, and T_{MPDO} values as defined in Table 33–17. The specification for T_{MPS} in Table 33–17 applies only to the DC

...

A Type 3 or Type 4 PSE, when connected to a single-signature PD:

- ...

- shall set mr_mps_valid to True when the DC MPS component is present, and shall set mr_mps_valid to False when the DC MPS component is absent.

A Type 3 or Type 4 PSE, when connected to a dual-signature PD:

- ...

- shall set mr_mps_valid_pri to True when the DC MPS component is present on the Primary Alternative, and shall set mr_mps_valid_pri to False when the DC MPS component is absent on the Primary Alternative.

- shall set mr_mps_valid_sec to True when the DC MPS component is present on the Secondary Alternative, and shall set mr_mps_valid_sec to False when the DC MPS component is absent on the Secondary Alternative.