PD Transients (33.3.7.6) v120

Info (not part of baseline)

The PD transient requirements have gotten lengthy and repetitive. This baseline collapses the text into one, and refers to a new Table for the parameters. It also incorporates the remedy for comment #94. The original section is included at the end for reference.

. . . PDs that do not meet these requirements shall comply with the following:

a) . . .

Replace 33.3.7.6 from D1.7 page 145 line 35 down to page 146 line 40 as follows:

b) A Type 2, Type 3, or Type 4 PD shall meet both of the following:

- The PD input current spike shall not exceed I_{TR_LIM} and shall settle below the PD upperbound template (see Figure 33–38 and Figure 33–39), or the PD extended template if the PD is assigned to Class 6 or Class 8 (see Figure 33–38), within 4 ms. During this test, the PD PI voltage is driven from $V_{Port\_PSE\text{-}2P}$ min to $V_{Port\_PSE\text{-}2P}$ min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0A.
- The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw for the assigned Class under the following conditions. The input voltage source drives V_{PD} from $V_{Port\_PSE\text{-}2P}$ min to 56 Vat 2250 V/s, the source impedance within 2.5% of R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

The requirements apply to each pairset independently if the PD is a dual-signature PD.

Insert new Table at the end of 33.3.7.6:

Item	Parameter	Symbol	Unit	Min	Max	PD Type	PD signature	Assigned Class
1	Input spike current limit	I_{TR_LIM}	A		2.5	2		All
						3,4	Dual	All
						3	Single	< 5
					3.0	3,4	Single	≥ 5

Table 33–TBD — PD current parameters during transients at the PSE PI

where

t	is the duration in seconds that the PD sinks $I_{Port\text{-}2P}$
$P_{Peak\_PD\text{-}2P}$	is the peak operating power on a pairset as defined in Table 33–28
P_{Class_PD}-2P	is the maximum average input power on a pairset as defined in Table 33–25
$T_{CUT\text{-}2P}$ min	is $T_{CUT\text{-}2P}$ min, as defined in Table 33–17

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least $T_{LIM\text{-}2P}$ min as defined in Table 33–17.

33.3.7.6 PD behavior during transients at the PSE PI

Editor's Note: 1. Type 3 and Type 4 to be added (to parts other than the newly added first paragraph).

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8.2. A single-signature PD shall include C_{port} as defined in Table 33–28. A dual-signature PD shall include $C_{Port\text{-}2P}$ as defined in Table 33–28 on each pairset.

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 or single-signature Type 3 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A single-signature Type 4 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 360µF or less requires no special considerations with regards to transients at the PD PI. A dual-signature Type 3 or Type 4 PD with peak power draw that does not exceed $P_{Class\_PD\text{-}2P}$ max and has an input capacitance of 180 µF or less per pairset requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

a) A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–38) after T_{LIM} min (see Table 33–17 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–31) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 or single-signature Type 3 PD that demands less than Class 5 power levels shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–38) within 4 ms. During this test, the PD PI voltage is driven from $V_{Port\_PSE\ min}$ to $V_{Port\_PSE\ min}$+2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance within 2.5% of R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

A dual-signature Type 3 PD that demands less than Class 5 power levels over a pairset shall meet both of the following over that pairset:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–38) within 4 ms. During this test, the PD PI voltage is driven from $V_{Port\_PSE\ min}$ to $V_{Port\_PSE\ min}$+2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance within 2.5% of R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

A Type 3 single-signature PD that demands Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–38) within 4 ms. During the test, the voltage of both PD modes is driven from $V_{Port\_PSE\ min}$ to $V_{Port\_PSE\ min}$ + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.
b) The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from $V_{Port\_PSE\ min}$ to 56 V at 2250 V/µs, the source impedance within 2.5% of R_{Ch} as defined in Table 33–1, and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

A Type 4 dual-signature PD that demands Class 5 power levels over a pairset shall meet both of the following over that pairset:

a) The PD mode input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template value (see Figure 33–38) within 4 ms. During the test, the voltage of both PD modes is driven from $V_{Port\_PSE\ min}$ to $V_{Port\_PSE\ min}$ + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.
b) The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from $V_{Port\_PSE\ min}$ to 56 V at 2250 V/µs, the source impedance within 2.5% of R_{Ch} as defined in Table 33–1, and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

A single-signature Type 3 or Type 4 PD that demands more than Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 3.0 A and shall settle below the PD extended template value (see Figure 33–38) within 4 ms. During the test, the voltage of both PD modes is driven from V_{Port_PSE} min to V_{Port_PSE} min + 2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 Ω, and a source that supports a current greater than 5.0 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from V_{Port_PSE} min to 56 V at 2250 V/µs, the source impedance within 2.5% of R_{Ch} as defined in Table 33–1, and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33–31).

The current limit per pairset at the MDI (MDI $I_{LIM\text{-}2P}$) is defined by Equation (33–31):

$$\{pse_{\text{ILIM-2P min}}\}_{\text{mA}} < \{mdi_{\text{ILIM-2P}}\}_{\text{mA}} \leq \{pse_{\text{ILIM-2P min}}\}_{\text{mA}} + 5_{\text{mA}} \quad (33\text{–}31)$$

where

$pse_{\text{ILIM-2Pmin}}$ is the PSE $I_{LIM\text{-}2P}$ min as defined in Table 33–17
$mdi_{\text{ILIM-2P}}$ is the per pairset current limit at the MDI (MDI $I_{LIM\text{-}2P}$)

33.3.7.7 Ripple and noise

The specification for ripple and noise in Table 33–28 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of $V_{Port\_PD\text{-}2P}$, and over the range of input power of the device.