TDL for Comments 151,130

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Existing Content

145A.3 PSE resistance and current unbalance

End to end pair-to-pair resistance/current unbalance refers to current differences in powered pairs of the same polarity. Current unbalance can occur in positive and negative powered pairs when a PSE uses all four pairs to deliver power to a PD.

Current unbalance requirements ($R_{PSE_{min}}$, $R_{PSE_{max}}$ and $I_{Con-2P-unb}$) of a PSE is met with $R_{load_{max}}$ and $R_{load_{min}}$ as specified in Table 145–17.

•	•	•
•	•	•
•	•	•

There are two alternate verification methods for R_{PSE_max} and R_{PSE_min} and determining conformance to Equation (145–15) and to $I_{Con-2P-unb}$.

Measurement methods to determine $R_{PSE_{max}}$ and $R_{PSE_{min}}$ and $I_{Con-2P-unb}$ are defined in 145A.3.1 and 145A.3.2.

This TDL addresses the *second, alternate* method of measuring PSE effective resistances

145A.3.2 - Effective resistance RPSE measurement ...

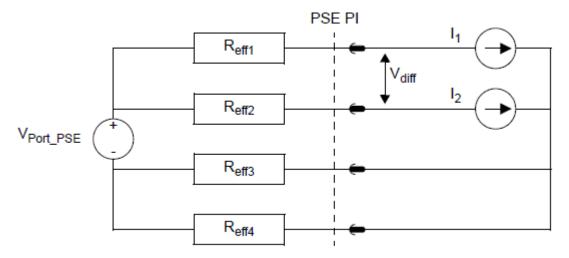


Figure 145A–3—Effective resistance verification circuit

The effective resistance verification procedure is described below:

1) With the PSE powered on, set the following current values

a. $10 \text{ mA} < I_2 < 50 \text{ mA}$

b.
$$I_1 = 0.5 \times (P_{max}/V_{port}) - I_2$$

Measure V_{diff}.

3) Reduce I1 by 20% (=I1'). Ensure I2 remains unchanged.

4) Measure Vdiff' in the same manner as Vdiff.

5) Calculate Reff1:

 $R_{eff1} = [(V_{diff}) - (V_{diff})] / (I_1 - I_1)$

7) Repeat procedure for Reff2, with I1, I2 values swapped.

8) Repeat procedure for Reff3, Reff4.

9) Evaluate compliance of R_{eff1} and R_{eff2} with Equation (145–15). Evaluate compliance of R_{eff3} , and R_{eff4} with Equation (145–15).

Validation Results

- Side 8 shows proof (by calculations) which validate the effective resistance measurement for *constant* effective resistances
- The technique can provide very close approximations of effective resistances which have negligible change
 - Current is held constant in one pair, so the effective resistance remains constant in that pair
 - In the other (measured) pair, current is near the maximum allowed, and is varied by a small relative percentage
 - thus remaining in a nearly constant effective resistance region for typical nonlinear components (eg. diodes, FETs)

Potential problems

- Will not work if any active balancing techniques are implemented in the PSE
 - Effective resistance becomes a variable
 - A tester may not be aware of active balancing in a DUT
- Temperature variations could change effective resistance results
 - May require long waiting for steady state (test time) and recalibration of the test fixture a few times during the test for each pair
 - The above is an implementation issue, however it requires detailed guidelines, which is outside the scope of the standard

Recommendation

- The measurement circuit should be omitted for the following reasons:
 - As a *second, alternate* method, it is not necessary to have it in the standard
 - Set-up and measurements don't provide a significant simplification vs the other methods
 - Potential problems have been identified (see previous slide)
- Proposed Changes to the Baseline are shown in the last 3 slides of this presentation

Overview of R_{eff1} Determination

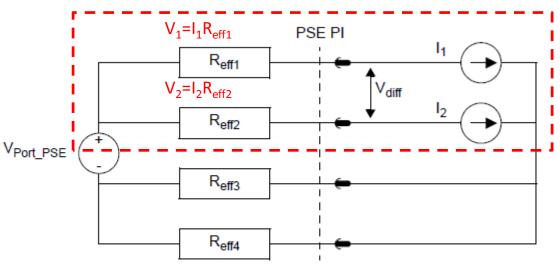


Figure 145A-2-Effective resistance verification circuit

 $\begin{aligned} &\mathsf{R}_{\mathsf{eff1}} = \mathsf{V}_1 / \mathsf{I}_1 \quad I_1 \text{ is known, } \mathsf{V}_1 \text{ is not known, however:} \\ &\mathsf{V}_1 = \mathsf{V}_{\mathsf{diff}} - \mathsf{V}_2 \quad and \, \mathsf{V}_{\mathsf{diff}} \, \textbf{can be measured.} \\ &\mathsf{The Solution is accomplished by:} \end{aligned}$

- 1) Holding V₂ constant (by holding I₂ constant), and
- 2) Performing a 2-step measurement to cancel V_2

similar to the technique used for Rdet to remove diode voltage bias

Where, $R_{eff1} = [V_{diff} - V'_{diff}]/[I_1 - I'_1]$

(The same steps can be performed for each Reff determination)

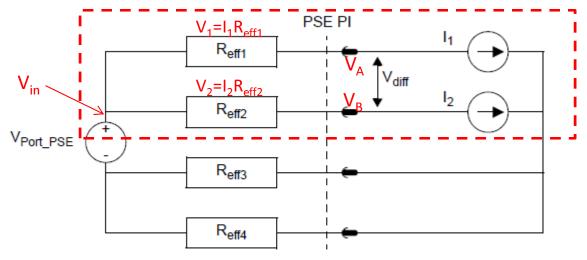


Figure 145A-2—Effective resistance verification circuit

•
$$V_{diff} = V_B - V_A = [V_{in} - V_2] - [V_{in} - V_1] = V_1 - V_2$$

•
$$V'_{diff} = V_B - V_A = [V'_{in} - V_2] - [V'_{in} - V'_1] = V'_1 - V_2$$

•
$$V_{diff} = I_1 R_{eff1} - V_2$$

•
$$V'_{diff} = I'_1 R'_{eff1} - V_2$$

•
$$V_{diff} - V'_{diff} = [I_1 R_{eff1} - V_2] - [I'_1 R'_{eff1} - V_2]$$

•
$$R_{eff1} \approx R'_{eff1} \lt$$

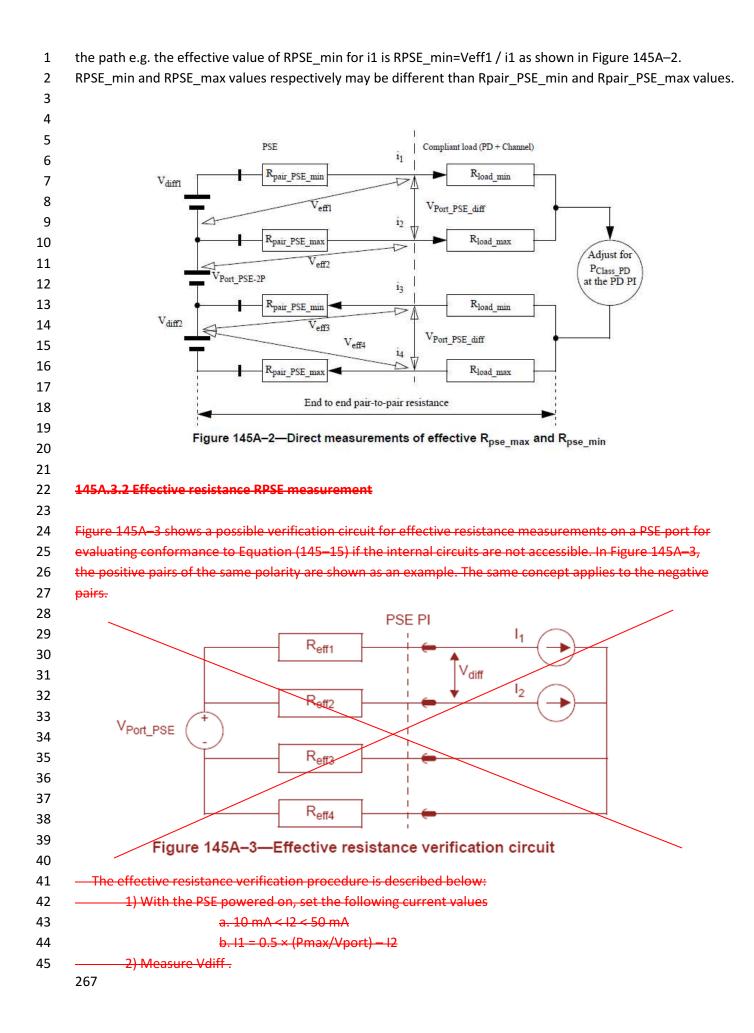
•
$$V_{diff} - V'_{diff} = I_1 R_{eff1} - I'_1 R_{eff1} = R_{eff1} [I_1 - I'_1]$$

•
$$R_{eff1} = [V_{diff1} - V'_{diff1}] / [I_1 - I'_1]$$

Resistive components will be constant. Active components have negligible change when operated within a narrow, nearly linear range

Baseline Changes

1	PSE PI Channel PD PI
2	R _{Ch_unb_min}
3	
4	R _{Ch_unb_max}
5	Rch_unb_min
6	
7	R _{ch_unb_max}
8	Figure 145A–1—Common mode pair-to-pair channel resistance unbalance
9	NOTE—Each conductor in this Figure is the equivalent of two conductors in parallel.
10	
11	145A.3 PSE resistance and current unbalance
12	
13	End to end pair-to-pair resistance/current unbalance refers to current differences in powered pairs of the
14	same polarity. Current unbalance can occur in positive and negative powered pairs when a PSE uses all four
15	pairs to deliver power to a PD.
16	
17	Current unbalance requirements (RPSE_min, RPSE_max and ICon-2P-unb) of a PSE is met with Rload_max and
18	Rload_min as specified in Table 145–17.
19	
20	A compliant unbalanced load, Rload_min and Rload_max, consists of the channel (cables and connectors) and
21	PD effective resistances, including the effects (or influence) of system end-to-end unbalance.
22	
23	Equation (145–15) is described in 145.2.8.5.1, specified for the PSE, assures that end to end pair-to-pair
24	resistance unbalance will be met in the presence of all compliant unbalanced loads (Rload_min and Rload_max)
25	attached to the PSE PI.
26	
27	Figure 145–22 illustrates the relationship between effective resistances at the PSE PI as specified by Equation
28	(145–15) and Rload_min and Rload_max as specified in Table 145–17.
29	
30	There are two is an alternate verification methods for RPSE_max and RPSE_min and determining conformance
31	to Equation (145–15) and to ICon-2P-unb.
32	
33	A Measurement methods to determine RPSE_max and RPSE_min and ICon-2P-unb are is defined in 145A.3.1
34	and 145A.3.2.
35	
36	If pair-to-pair balance is actively controlled in a manner that changes effective resistance to achieve balance,
37	then the current unbalance measurement method described in 145.2.8.5.1 should be used.
38	
39	145A.3.1 Direct RPSE measurement
40	
41	If there is access to internal circuits, effective resistance may be determined by sourcing current in each path
42	corresponding to maximum PClass operation, and measuring the voltage across all components that contribute
43	to the effective resistance, including circuit board traces and all components passing current to the PSE
44	PI output connection. The effective resistance is the measured voltage Veff, divided by the current through



1	
2	4) Measure Vdiff' in the same manner as Vdiff.
3	
4	Reff1 = [(Vdiff) – (Vdiff')] / (I1 – I1')
5	
6	
7	-9) Evaluate compliance of Reff1 and Reff2 with Equation (145–15). Evaluate compliance of Reff3,
8	and Reff4 with Equation (145–15).
9	
10	The effective resistance verification method applies to the general case. If pair-to-pair balance is actively
11	controlled in a manner that changes effective resistance to achieve balance, then the current unbalance
12	measurement method described in 145.2.8.5.1 may be used.
13	