DC Disconnect

Jean Picard, Texas Instruments

IEEE 802.3bt Task Force

November 2014

Supporters

- Kousalya Balasubramanian / Cisco
- Christian Beia / ST
- Yair Darshan / Microsemi
- Sesha Panguluri / Broadcom
- Fred Schindler / SeenSimply

Goal of this Presentation

The motivation of this work is to determine how DC disconnect will be applied by a “bt” PSE for 2- and 4-pair systems, from PD type 1 to type 4.

Topics covered will include the “Maintain Power Signature” (MPS) parameters and how they will be applied.

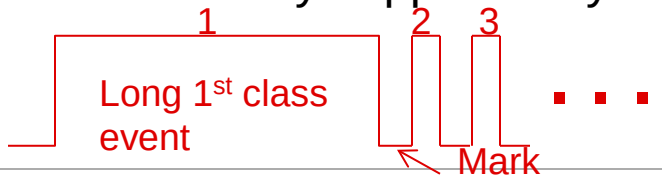
Backwards compatibility will be discussed as well.

PSE Configurations: Type 3 and 4

PSE Equipment Port Identification	PSE Type	Detailed Description
2- or 4-pair, 15W, “bt”	3	• New MPS timing is available • 1 x 2-pair or 2 x 2-pair with power “capability” of 15W
2- or 4-pair, 30W, “bt”	3	• New MPS timing is available • 1 x 2-pair or 2 x 2-pair with power “capability” of 30W
4-pair, 60W, “bt”	3	• New MPS timing is available • 2 x 2-pair with power “capability” of 60W
4-pair, < 100W, “bt”	4	• New MPS timing is available • 2 x 2-pair with power “capability” of < 100W • ***Note: Cable/channel requirements for type 4 operation still need to be defined.***

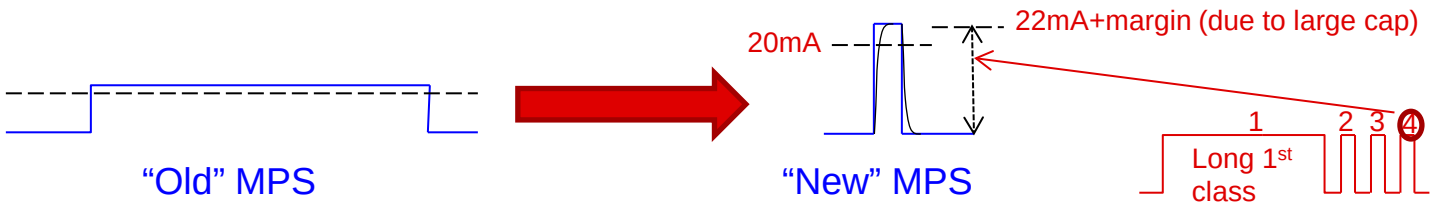
MPS Timing

- Type 3 and 4 PSEs will be required to support the “new” MPS timing, which includes a much shorter TMPS.
  - PSE TMPS = 6 ms maximum.
  - PD requirement at PSE PI (worst case cable impedance) ≥ 7 ms.
  - See Yseboodt and Abramson, “MPS Baseline Proposal”, Norfolk, May 2014.
- Hence, a Type 3 or 4 PD will have the option of using this feature to reduce standby system consumption.
- Such PD will determine if the “new” MPS timing can be used by measuring the duration of the first class event (~85 ms).
  - If connected to a type 1 or 2 PSE, the 1st class finger is shorter (75 ms or 30 ms max), and the PD “knows” the “new” MPS is not applicable.
  - Also, there shouldn’t be thermal concern since this is only ~13% longer than 802.3at Tpdc.
  - See Abramson, “IEEE P802.3bt Mutual Identification”, Ottawa, Sept. 2014.
- There is also no interoperability issue with type 1 and 2 PDs.
  - These PDs generate a much longer MPS pulse, and consequently they are automatically supported by a Type 3 or 4 PSE.



MPS Current Amplitude when Connected to a Type 3 Class 5 or 6, or Type 4 PD (Single Interface)

- We need to maintain the accuracy in disconnect sensing.
  - Picard, “An Optimum Approach to Apply DC Disconnect”, Beijing, March 2014.
- Hence, if class 5, 6 or 7, the PD required current draw to maintain power (I_{port_MPS}) should be ~2x for single interface PD.
  - I_{port_MPS} changes from 10 mA to 22 mA.
  - Once it receives a 4th class event (and the 1st class event is “long”), the PD “knows” the threshold is ~2x (i.e. 10mA per 2-pair in ideal case).



Current margin (see Annex) not necessarily needed

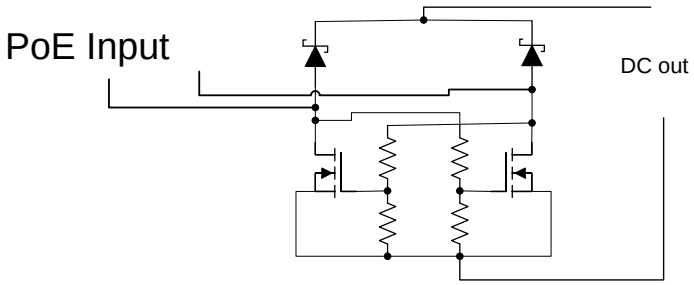
PD Type	Class	Max Power Sourced (@ PSE PI)	Event 1 (Class sig)	Event 2 (Class sig)	Event 3 (Class sig)	Event 4 (Class sig)	Event 5 (Class sig)
Power Level Indicated by Event			2/4-Pair 15W	2/4-Pair 30W	4-Pair 30W	4-Pair Up to 60W	4-Pair < 100W
3	5	45W	4	4	1	1	1
3	6	60W	4	4	2	2	2
4	7	< 100W (TBD)	4	4	3	3	3

PSE I_{HOLD} Definition and Current Imbalance with Single PD Interface

- "Per 2-pair" approach is a preferred solution for DC disconnect.
  - It provides a flexible & modular PSE solution to handle 2P and 4P applications.
  - It provides a much better coverage of fault handling and diagnostics.
- 2-pair DC disconnect requires acceptable P2P current balance (~+/-25% max) in the "return path", for a range of 10-20mA.
- Potential issues if PDs are using discrete diode bridges.
  - "Matched" Vf or tight Vf tolerance characteristics needed.
- Imbalance is an issue mostly for class 5-6 Type 3 PDs, where power schottky diodes can be acceptable. Not really a problem for other classes.
  - If Class 0-4 PD, the PSE could turn off one channel to do a "2P" DC disconnect verification. Imbalance does not matter in this case, schottky diodes are OK.
  - Class 7 PD are expected to use integrated FET bridge. Minimal impact on imbalance.
- Also, what really matters here is the imbalance for the **return path**.
- Simple and reasonable cost solutions can be implemented for Class 5-6 PD (see next page).

Current Imbalance and PSE I_{HOLD} Definition with Single PD Interface

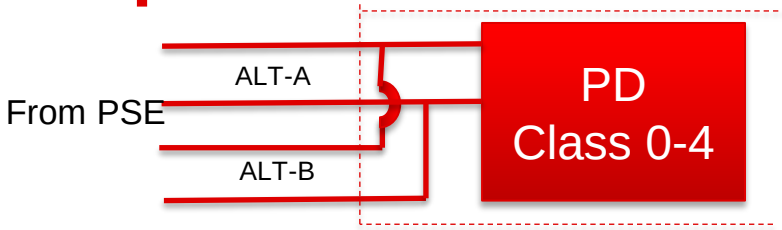
- In order to make this work for class 5-6-7, we need a current imbalance of **less than +/-15%** for the return path. This means less than +/- ~1.5 mA.
- This can be, for example, combined with a slightly lower PSE I_{HOLD} range "per 2P" (**4.5-9.5mA** instead of 5-10mA) if connected to class 5 to 7 PD.
  - I_{port_MPS} being 2 x 11 mA, we get the 1.5 mA margin needed.
- The input bridge below is an example on how to solve the imbalance issue for class 5-6 at minimal costs. Two of the 4 diodes are replaced with FETs.
  - And, for minimal FET cost, we just need Rdson x $I_{full\ load} \leq Vf\_diode$.



Return Path Balance Circuit

  - At 10 mA, voltage drop is ~**100x smaller** than a schottky diode Vf.
  - Calculations show **< 15%** imbalance (extreme WC) for return path since only resistive elements (PD, PSE, cables, conn.) are defining the imbalance.

MPS Current Amplitude if PD is Class 0-4



- If class 0-4 PD, the DC disconnect threshold is same for type 1, 2 and 3 PSEs.
  - Same as AT ⇒ 5 – 10 mA.
  - Imbalance requirement does not apply here, as discussed previously.
- A Type 3 PSE cannot know if the class 0-3 PD is type 1 or 3, or if a class 4 PD is type 2 or 3.
- Note that since it is class 0-4, a 2-channel PSE can still maintain its accuracy by turning off its 2nd switch while doing DC disconnect check with 1st switch.

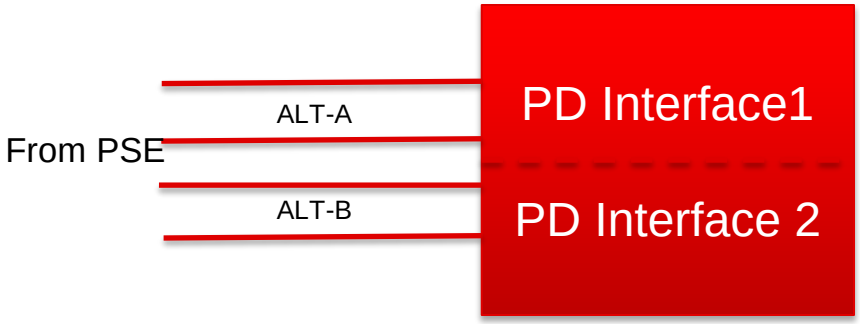
"Old" MPS

"New" MPS class 0-4

Current margin (see Annex) not necessarily needed

PD Type	Class	Max Power Sourced (@ PSE PI)	Event 1 (Class)	Event 2 (Class)	Event 3 (Class)	Event 4 (Class)	Event 5 (Class)
Power Level Indicated by Event			2/4-Pair 15W	2/4-Pair 30W	4-Pair 30W	4-Pair Up to 60W	4-Pair < 100W
1,3	0-3	< 15W	0-3	0-3	0-3	0-3	0-3
2,3	4	30W	4	4	4	4	4

The Case of Dual PD Interface

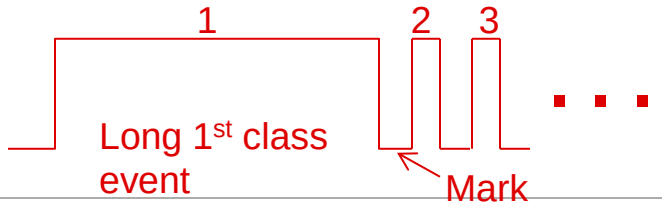


- There are two cases:
  1. Up to 25.5W PD input power each 2-pair. This is type 3.
  2. Up to ~35W (TBD) PD input power each 2-pair. This is type 4, since the power per 2-pair exceeds 25.5W.
- Since there is one PD interface per 2-pair, the DC disconnect is independently applied per 2-pair.
- For same reasons, the PSE DC disconnect threshold is maintained at same nominal threshold as type 2.
- Both power channels are required to support the “new” MPS timing.

Current margin (see Annex) not necessarily needed

PD Configurations Summary

PD Type	Class	PD interface	PSE Type	Class 1st Finger Duration	PSE MPS Timing/Current thresh.	2 or 4 Pairs	PD Input Power
1	0-3	Single	1,2	Short	Old/Old	2	≤ 13W
			3	Long	New/Old	2	
2	4	Single	1,2	Short	Old/Old	2	≤ 13W or 25.5W
			3	Long	New/Old	2	25.5W
3	0-4	Single	1,2	Short	Old/Old	2	≤ 13W or 25.5W
			3	Long	New/Old	2	3.84W-25.5W
						2 x 2	
	5	Single	3, 4	Long	New/New	2 x 2	40W
	6						51W
	4 (each)	Dual	3, 4	Long	New/Old (each)	2 x 2	2 x 25.5W
4	7	Single	4	Long	New/New	2 x 2	~71W (TBD)
	5 (each)	Dual	4	Long	New/Old (each)	2 x 2	2 x ~35W (TBD)



New MPS timing: Short (~ 6 ms) TMPS

New MPS PSE Current threshold: 2 x 10 mA max

Old MPS PSE Current threshold: 10 mA max

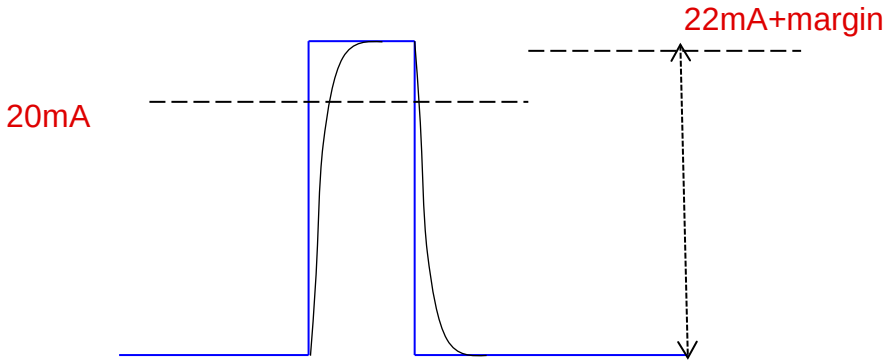
Summary

- The Concept proposed meets the following goals
  - Covers 2-pair and 4-pair configurations.
  - Covers Type 1 to Type 4 PSE and PD.
  - Covers single and dual PD interface applications.
  - Provides a simple means to allow the use of the new MPS timing and amplitude.
  - Provides backwards compatibility.
  - Maintains DC disconnect accuracy while minimizing cost impacts at both ends of the cable.
- What's next:
  - Complete the definition of the DC MPS Current parameters (I_{HOLD} , I_{port_MPS}) for a 4-pair type 3 and 4 PSE, as well as the PD return path current imbalance.
    - PD class 0-4 versus PD class 5-7.

Annex: Margin and Impact of Large Capacitance on MPS Current Waveform

Impact of Large Capacitance on MPS Current Waveform

- Large PD capacitance can effectively shorten an MPS pulse by “stealing” the current from the PSE. There are many possible solutions to address this.
  - For example, adding margin (ex: 1-2 mA) between the PD pulsed current amplitude and PSE threshold.
  - Or by increasing the pulse width of PD current (the 7 ms is only a minimum requirement).
  - Another approach is by inserting a blocking diode (FET’s body diode).
  - See Yseboodt, “MPS Baseline Proposal”, Norfolk, May 2014



MPS Pulse Example if Class 5, 6 or 7