Power Matters

Microsemi

IEE802.3 4P Task Force

Figure 33-17.1 - PSE-PD simplified Cport interpretation model

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Comment [clause 33.3.7.3 page 132 line 11]

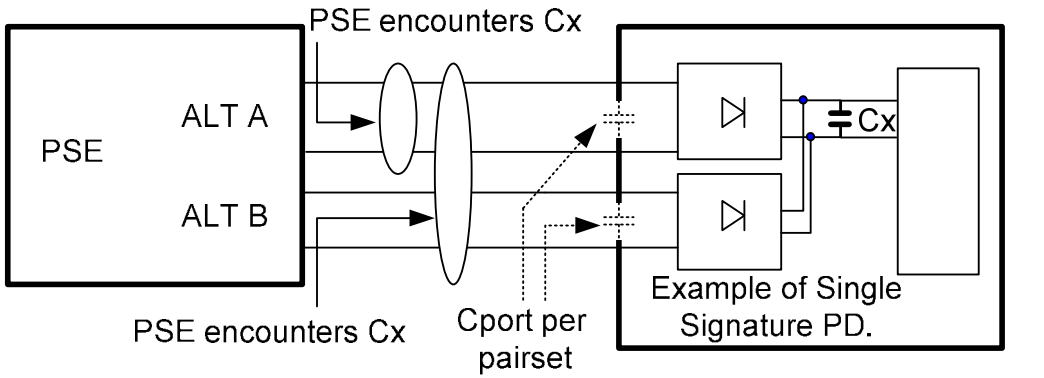
This is the response to the remedy of comment # 150 in D1.3 which says:
To delete the text "See PSE-PD simplified Cport implementation model in Annex TBD."
From:
"Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6.
"Yair is invited to provide figure and new text (no Annex)".

Suggested Remedy

1. Change from:
"Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6."

To:
Cport in Table 33-18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when operating one or both pairsets, when connected to a single-signature PD. ~~over a pairset or both pairsets.~~ When PSE is connected to dual-signature PDs, Cport value requirements are specified in 33.3.7.6."
See Figure 33-17.1 for PSE-PD simplified Cport interpretation model."

2. Add figure 33-17.1 after the above text as described in page 3 of darashan_02_1115.pd.



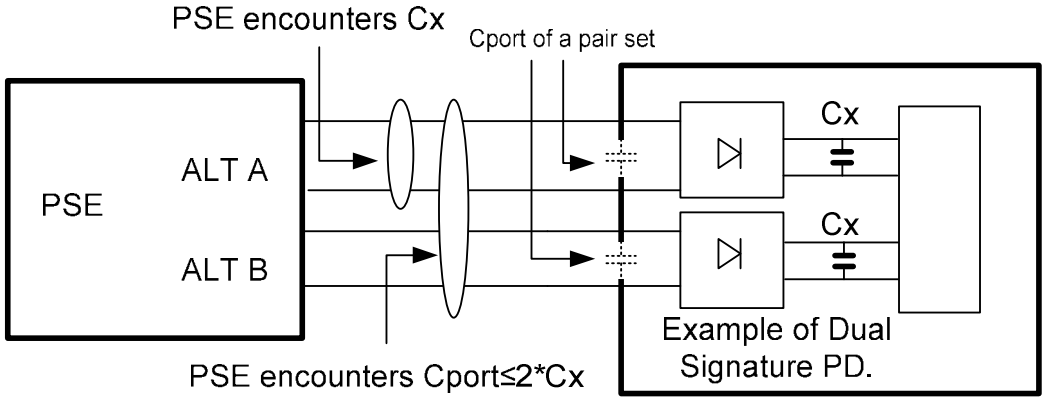


Figure 33-17.1 - PSE-PD simplified Cport interpretation model. Yair Darshan. Rev 001 November 2015.