Addressing the changes in Table 33-1 for supporting Type 3 and 4 PSEs Inrush.

- All PSEs connected to Type 1 and 2 PDs – Changed to Class 0-4 PDs to include all PD Types with class 0-4.

For Type 3 and 4, PSE can choose between the two following options

- Option 1: Type 3 and 4 PSE when connected to Type 3 and 4 PDs: Iinrush-2P=0.2A min 0.45A max. Iinrush= 0.4A to 0.9A. PSE has to meet both requirements for Iinrush-2P and for Iinrush. Inrush-2P with P2PUnb effect is addressed in 33.2.7.5. PSE needs to meet PD model to guarantee stability (when implementing foldback current limit circuitry that must starts with lower current than 0.4A min per pairset) and finishing Tinrush within 50msec for Cport and class 3 load in parallel during POWER_UP.

- Option 2: 4 PSE when connected to 4 PDs: Iinrush-2P=0.4A min, inrush= 0.8A to 0.9A. PSE has to meet both requirements for Iinrush-2P and for Iinrush. Inrush-2P with P2PUnb effect is addressed in 33.2.7.5.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

#	Parameter	Symbol	Units	Min	Max	PSE Type	Additional Information
5	Output current in POWER_UP state	Iinrush	A	0.4	~~See Info~~ 0.45	~~1,2,3,4~~ All	For class 0-4 single signature PDs. *For dual signature PDs with different class over each pairset, this requirement applies over each pairset.* See 33.2.7.5. See max value definition in Figure 33-13.
5a	Output current in POWER_UP state	Iinrush	A	0.4	0.9	3,4	For ≥ class 5 single signatures PD. For dual signature PD with the same class per pairset. Total current for both pairsets. See 33.2.7.5. See max value definition in Figure 33-13.
5b	Output current per pairset in POWER_UP state	Iinrush-2P	A	0.150	0.6	3,4	For ≥ class 5 single signatures PD. For dual signature PD with the same class per pairset. See 33.2.7.5. See max value definition in Figure 33-13.
5c	Output current in POWER_UP state	Iinrush	A	0.8	0.9	4	For class 7 and 8 PDs For dual signature PD with the same class per pairset. Total current for both pairsets See 33.2.7.5. See max value definition in Figure 33-13.
5d	Output current per pairset in POWER_UP state	Iinrush-2P	A	0.4	0.6	4	For class 7 and 8 For dual signature PD with the same class per pairset. See 33.2.7.5. See max value definition in Figure 33-13

New option

Modified current Spec

Addressing Iinrush-2P unbalance.

- 0.4A is preferred per original spec. Iinrush is controlled per pairset so we can meet it.
- If we use 0.386x Inrush_min of item 5c as proposed in rev 005 of this document, we may not be able to powerup dual signature same class PD if turn ON time is not about the same.

33.2.7.5 Output current in POWER_UP mode

Editor's Note: Timing requirements for 4-pair power to be added to this section.

Editor Notes:

1. To verify that in dual signature PD with same class i.e. same load, the PD startup is guaranteed if one of the pairsets has Inrush-2P_minz and the 2nd has the rest of the current. If both pairsets are turned on as the same time, there is no issue at all.
2. To update the definition of dual signature PD with the same class signature that it is a single load PD as opposed to dual signature PD with different class that has isolated different loads and hence end to end pair to pair resistance unbalance is zero. This will simplify the spec and make it clearer.
3. Table 33-11 item 5a -5d: to verify that PSE is allowed to do inrush limit with 2P mode.

Change the text of 33.2.7.5 as follows:

POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of $T_{Inrush-2P}$ or, for Type 1 and Type 2 PSEs that make use of legacy powerup, the conclusion of PD inrush currents on that pairset (see 33.3.7.3).

Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a single-signature PD shall reach POWER_ON state on both pairsets within $T_{Inrush-2P}$ max, starting with the first pairset transitioning into the POWER_UP state. See legacy_powerup variable in section 33.2.4.4 for more information on the POWER_UP to POWER_ON transition.

Addressing the effect of E2EP2PRunb on Iinrush-2P and linking Iinrush requirements for all PSE types to Table 33-11

Figure 33-13 was modified to address the effect of end to end pair to pair resistance unbalance on the maximum limit of Iinrush-2P which by simulation found to be 0.556A adding margin ➔ 0.6Amax. This value will be updated in Figure 33-13 as well to cover requirements below 1msec.

Addressing the effect of E2EP2PRunb on Iinrush-2P with dual signature PD with the same class over each pairset.

The requirements for Iinrush-2P E2EP2PRunb are the same for all Single Signature PDs at class 5 and above operating at 4-pairs and dual signature PD with the same class over each pairset. For dual signature different class the requirements are as for Type 1/2 per pairset.

The PSE shall limit the maximum current sourced per pairset (Inrush-2P) and the total inrush current (Iinrush) during POWER_UP per the requirements of Table 33-11 item 5 or items 5a and item 5b or items 5c and item 5d. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset PSE inrush template in Figure 33–13 and Equation (33–5) when operating class 0-4 PDs and Figure 33-13 and equation (33-5a) when operating single signature PDs with class 5 and above or when operating dual signature PDs with the same class over each pairset.

The minimum value of Iinrush-2P includes the effect of end to end pair to pair resistance unbalance.

Addressing the requirements for the new Iinrush option (covered by Table 33-11 items 5a and 5b) for Type 3 and 4 PSE in which we allow per pairset current to be 0.15A to 0.6A (to cover unbalance too) AND total of 0.4A to 0.9A.
In this use case PSE will have to be tested with a worst case PD load containing in its input 360uF for Type 4 and 180uF for Type 3 with parallel load of 13W or 350mA during POWER_UP phase and make sure that the PD input cap is charged to a steady state at Vport_PSE within 50msec for all PSE and PD operating conditions without startup oscillations. This test is required to ensure interoperability since in this use case PSE behavior is depend in PD worst case load and make it equivalent to the current spec in option 5c and 5d that its minimum Iinrush energy is sufficient to charge worst case load under all PDs operating

Type 4 PSEs supporting Class 7 and 8 when implementing Iinrush-2P and Inrush requirements per Table 33-11 items 5a and 5b and when connected to single signature PD through channel resistance of 0.1Ω to 12.5Ω per pairset, shall successfully power up within 50msec without startup oscillations a PD with Cport per pairset as defined in 33.3.7.3 in parallel to a Class 2 load during POWER_UP period in addition to the other requirements of 33.3.7.

a) During POWER_UP, for pairset voltages between 0 V and 10 V, the minimum $I_{Inrush-2P}$ requirement is 5 mA.
b) During POWER_UP, for pairset voltages between 10 V and 30 V, the minimum $I_{Inrush-2P}$ requirement is 60 mA.
c) During POWER_UP for class 4 and below, for pairset voltages above 30 V, the minimum $I_{Inrush-2P}$ requirement is as specified in Table 33–11item 5.
During POWER_UP for class 5 and above, for pairset voltages above 30 V, the minimum $I_{Inrush-2P}$ and I_{Inrush} requirement are as specified in Table 33–11item 5a and item 5b or as specified in Table 33-11 items 5c and 5d.

d) For Type 1 PSE, measurement of minimum $I_{Inrush-2P}$ requirement to be taken after 1ms to allow startup transients. A Type 2 PSE that uses Single-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a Class 4 PD as if it used Multiple-Event Physical Layer classification.

Replace Figure 33-13 with the following:

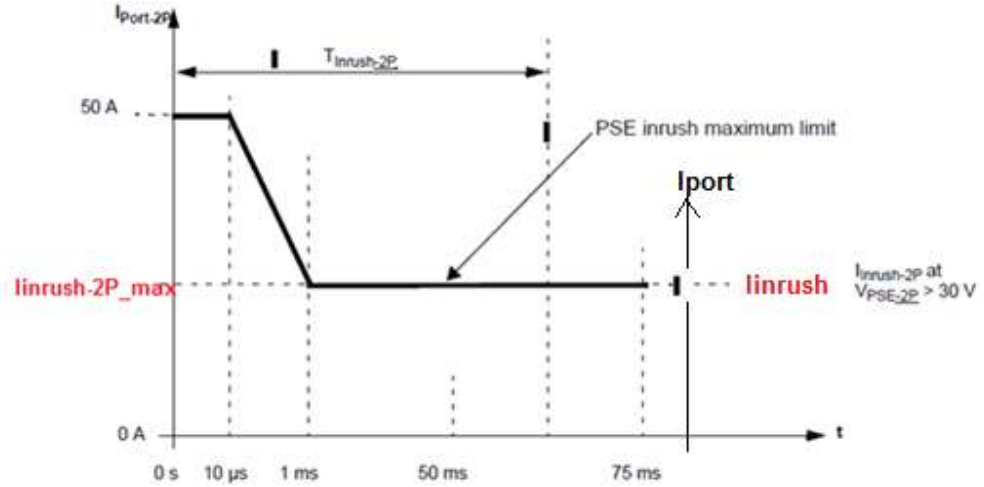

Figure 33–13—$I_{Inrush-2P}$ current and timing limits, per pairset in POWER_UP

The PSE inrush maximum limit, $I_{PSEIT-2P}$, is defined by the following segments:

$$I_{PSEIT-2P}(t) = \begin{cases} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ \text{TBD=function of (t, Iinrush-2P\_max)} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ \text{Iinrush-2P\_max} & 0.001 \le t < 0.075 \end{cases}_{A} \qquad (33\text{–}5)$$

Editor Note: To update the TBD in equation 33-5. Add Equation 33-5a after equation 33-5 to describe the template of figure 33-13 for Iinrush.

where t is the time in seconds

Table 33–18—PD power supply limits

1. Table 33-18: All PD classes and dual and single signature
2. Addressing the effect of E2EP2PRunb on Iinrush-PD-2P

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
5	Input Inrush current ~~per pairset~~	Iinrush-PD~~_2P~~	A		0.4	~~1,2.~~ All	Peak value see 33.3.7.3 For single signature PD class 0-4.
	Input Inrush current per pairset	Inrush-PD-2P			0.4		For dual signature PDs with different class over each pairset, this requirement applies over each pairset.
5a	Total Inrush current	Iinrush-PD			0.4	3,4	Peak value see 33.3.7.3 Single Signature PDs Class 5-6 Dual Signature PDs with the same class.
5b	Total Inrush current	Iinrush-PD_2P			0.3/ TBD	3,4	Peak value see 33.3.7.3 Single Signature PDs Class 5-6 Dual Signature PDs with the same class.
5c	Total Inrush current	Iinrush-PD			0.8	4	Peak value see 33.3.7.3 Single Signature PDs Class 7-8. Dual Signature PDs with the same class.
5d	Input Inrush current per pairset	Iinrush-PD_2P			0.6	4	Peak value see 33.3.7.3 Single Signature PDs Class 7-8. Dual Signature PDs with the same class.

33.3.7.3 Input inrush current

Replace first paragraph of Section 33.3.7.3 with the ~~followin~~following g:

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with Vport_PD-2P requirements as defined in Table 33–16a, and ending when CPort has reached a steady state and is charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33–11. All PDs shall consume a maximum of Class 3 power for at least Tdelay-2P min. This allows the PSE to properly ~~compete~~ complete inrush.

Editor's Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277.

Change second, third and fourth paragraph of Section 33.3.7.3 as follows:

Tdelay-2P for each pairset starts when VPD-2P crosses the PD power supply turn on voltage, VOn_PD. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from IInrush-2P to ILIM-2P.

Addressing Cport for single and dual PDs

For PDs operating at class 0 to 6:
Input inrush current at startup is limited by the PSE if CPort per pairset < 180 µF, as specified in Table 33–11.
If CPort per pairset ≥ 180 µF, input inrush current shall be limited by the PD so that IInrush_PD and Iinrush-PD-2P ~~per pairset~~ max is satisfied.

For Type 3 and 4 PDs operating class 1–5 dual signature PDs:
Input inrush current at startup is limited by the PSE if CPort per pairset< 180 µF, as specified in Table 33–11.
If CPort per pairset ≥180 µF, input inrush current shall be limited by the PD so that IInrush_PD and Iinrush-PD-2P max is satisfied.

For Type 4 PDs operating class 7 and 8 single signature PDs:
Input inrush current at startup is limited by the PSE if CPort per pairset < 360 µF, as specified in Table 33–11.
If CPort per pairset ≥360 µF, input inrush current shall be limited by the PD so that IInrush_PD and Iinrush-PD-2P max is satisfied.

Insert the following note at the end of section 33.3.7.3 as follows:

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after Tinrush-2p min. See 33.2.7.4 for details.

CPort in Table 33–18 is the total PD input capacitance during POWER_UP and POWER_ON states that a PSE ~~sees~~ encounters when operating one or both pairsets, when connected to a single-signature PD. ~~over a pairset or both pairsets.~~ When PSE is connected to dual-signature PDs, CPort value requirements are specified in 33.3.7.6.

---------- End of Baseline text ----------

Annex A- Calculations.

Item 5b Iinrush-2P and Iinrush-2P_max

For Iinrush total of 0.4A min and 0.9A max per Table 33-15 item 5a, Iinrush-2Pmin and max are given per the following calculations for Table 33-11 item 5b:

The simulated unbalance on those pairs is ~23% rounded to 25%. So the minimum current on that pairs of the same polarity is 0.4A*(1-0.25)/2=0.15A when we take Iinrush_min..

The result for Iinrush_max, will be 0.9*(1+0.25)/2=0.5625A and so in that way we get the range for all possibilities. I have rounded this number from 0.5625 to 0.600.

Please note that PoE cannot have Inirush=2x0.6A because row 5b forbids it. The max is 0.9A. Therefore PSE has to meet both rows of Iinrush and Iinrush-2P per option.

Regarding Item 5c and 5d:

We can choose Iinrush-2Pmin =0.4A or Iinrush_min*(1-0.25)/2=0.386* Iinrush_min.

The reason that I choose 0.4A is because this value is <0.4 and may create difficulties to operate DS PD signature PD if PSE wants to POWER it UP completely independent. I am not fully sure that it is the case but right now I am careful so I am assuming the worst case.

The reason why we can work with 0.4A is because we are regulating each per set for 0.4A to 0.45a precisely so there are no unbalance issues on those pairs.

On the other pairs there is the limit off 0.6A max which is the important issue and sufficient to limits those pairs current.