PD Transient Sections 33.3.8.5, 33.3.8.6 (TDL 2.0 #50, 51) Rev 01

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The following content shows the proposed changes for Comment #34.
(TDL Draft 2.0 Comments 50, 51 will be "OBE" by these changes.)

33.3.8.5 Peak transient current

When the input voltage at the PI is static and in the range of $V_{Port\_PD\text{-}2P}$ defined by Table 33–31, the transient current drawn by a single-signature PD shall not exceed $I_{transient}$, defined in Table 33–31, in either polarity. A dual-signature PD shall not exceed $I_{transient}$ in either polarity per pairset under the same conditions. This limitation applies after inrush has completed (33.3.8.3) and before the PD has disconnected.

~~Under normal operating conditions when there are no transients applied at the PD PI, single-signature PDs, with the exception of those described in 33.3.8.2.1 and 33.3.8.4.1, shall operate below the PD upperbound template defined in Figure 33–36.~~

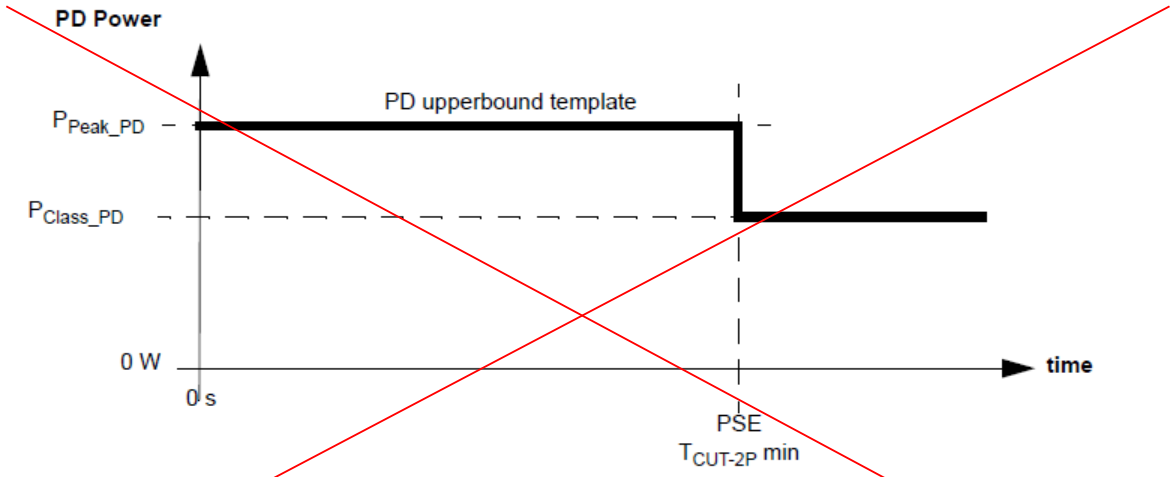

Figure 33–36—Type 1, Type 2, and single-signature PD static operating mask

NOTE—PDs are required to meet Equation (33–2) which results in a slightly lower power and current than results from Figure 33–36, Figure 33–37, Figure 33–38, Equation (33–28), Equation (33–29) and Equation (33–31).

~~The PD upperbound template in Figure 33–36, P_{SSUT}, is described by Equation (33–29):~~

$$P_{SSUT}(t) = \begin{cases} P_{Peak\_PD} & \text{for } (0 \le t < T_{CUT\text{-}2P}\ \text{min}) \\ P_{Class\_PD} & \text{for } (T_{CUT\text{-}2P}\ \text{min} \le t) \end{cases} \text{ W} \qquad (33\text{–}29)$$

~~where t is the duration in seconds that the PD sinks I_{Port} P_{Peak_PD} is the maximum peak operating power, as defined in Table 33–31 P_{Class_PD} is the maximum power, as defined in Table 33–27 $T_{CUT\text{-}2P}$ min is $T_{CUT\text{-}2P}$ min, as defined in Table 33–19~~

~~Dual-signature PDs shall operate below the PD upperbound template defined in Figure 33–37.~~

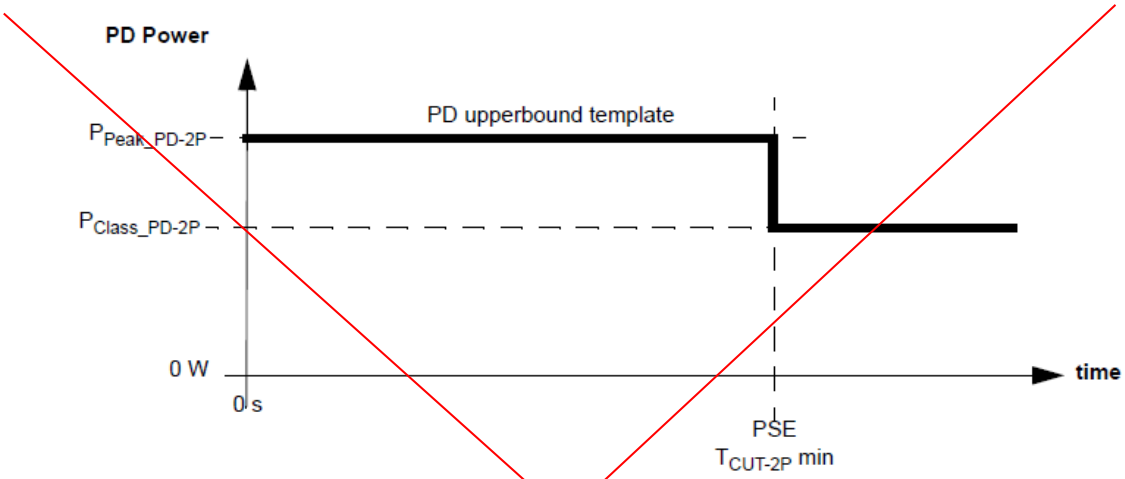

Figure 33–37—Dual-signature PD static operating mask

NOTE—PDs are required to meet Equation (33–2) which results in a slightly lower power and current than results from Figure 33–36, Figure 33–37, Figure 33–38, Equation (33–28), Equation (33–29) and Equation (33–31).

The PD upperbound template in Figure 33–37, P_{DSUT}, is described by Equation (33–30):

$$P_{DSUT}(t) = \left\{ \begin{array}{l} P_{Peak\_PD\text{-}2P} \text{ for } (0 \le t < T_{CUT\text{-}2P} \text{ min}) \\ P_{Class\_PD\text{-}2P} \text{ for } (T_{CUT\text{-}2P} \text{ min} \le t) \end{array} \right\}_{W} \quad (33\text{–}30)$$

where

t	is the duration in seconds that the PD sinks $I_{Port\text{-}2P}$
$P_{Peak\_PD\text{-}2P}$	is the peak operating power on a pairset as defined in Table 33–31
$P_{Class\_PD\text{-}2P}$	is the maximum average input power on a pairset as defined in Table 33–28
$T_{CUT\text{-}2P}$ min	is $T_{CUT\text{-}2P}$ min, as defined in Table 33–19

~~PDs described in 33.3.8.2.1 and 33.3.8.4.1 shall operate below the PD extended template defined in Figure 33–38.~~

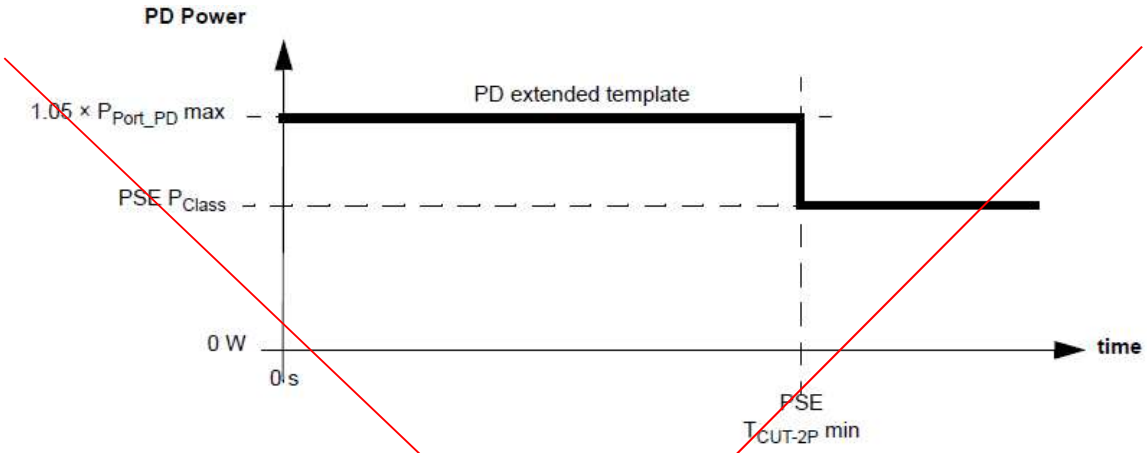

Figure 33–38—Class 6 and Class 8 PDs described in 33.3.8.2.1 and 33.3.8.4.1

NOTE—PDs are required to meet Equation (33–2) which results in a slightly lower power and current than results from Figure 33–36, Figure 33–37, Figure 33–38, Equation (33–28), Equation (33–29) and Equation (33–31).

The PD extended template in Figure 33–38, P_{SSET}, is described by Equation (33–31):

$$P_{SSET}(t) = \left\{ \begin{array}{ll} I_{Peak} \times V_{PSE} & \text{for } (0 \le t < T_{CUT\text{-}2P}\ \text{min}) \\ P_{Class} & \text{for } (T_{CUT\text{-}2P}\ \text{min} \le t) \end{array} \right\}_{W} \quad (33\text{–}31)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
I_{Peak}	is the peak operating current, I_{Peak} max, as defined in Equation (33–10)
V_{PSE}	is the voltage at the PSE as defined in 33.1.4.
P_{Class}	is the minimum power output by the PSE, as defined in Table 33–13, and 33.2.7.
$T_{CUT\text{-}2P}$ min	is $T_{CUT\text{-}2P}$ min, as defined in Table 33–19

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least $T_{LIM\text{-}2P}$ min as defined in Table 33–19.

33.3.8.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8. A single-signature PD ~~shall~~ includes Cport as defined in Table 33–31. A dual-signature PD ~~shall~~ includes CPort-2P as defined in Table 33–31 on each pairset.

~~— A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.~~

~~— A Type 2 or single-signature Type 3 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.~~

~~— A single-signature Type 4 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 360µF or less requires no special considerations with regards to transients at the PD PI.~~

~~— Type 4 single-signature PDs that draws more than Class 8 P_{Class_PD}, as defined in 33.3.8.2, shall meet these requirements for all values of input capacitance.~~

~~— A dual-signature Type 3 PD with peak power draw that does not exceed $P_{Class\_PD\ 2P}$ max and has an input capacitance of 110 µF or less per pairset requires no special considerations with regard to transients at the PD PI.~~

~~— A dual-signature Type 4 PD with peak power draw that does not exceed $P_{Class\_PD\text{-}2P}$ max and has an input capacitance of 180 µF or less per pairset requires no special considerations with regard to transients at the PD PI.~~ *(The above paragraph is organized below to improve readability. The 4th statement above is omitted because it doesn't fit in a list of "excluded" PDs, and the 3rd and last items make it redundant.)*

The following PD configurations do not require any further consideration with regard to PSE transients:

1) Type 1 PD with an input capacitance of 180 µF or less.
2) Type 2 and single-signature Type 3 PDs with peak power not exceeding PClass_PD, and with an input capacitance of 180 µF or less.
3) Single-signature Type 4 PDs with peak power not exceeding PClass_PD, and with an input capacitance of 360µF or less.
4) Dual-signature Type 3 PDs with peak power draw not exceeding PClass_PD-2P, and with an input capacitance of 110 µF or less per pairset.
5) Dual-signature Type 4 PDs with peak power draw that does not exceed PClass_PD-2P and with an input capacitance of 180 µF or less per pairset.

~~PDs that do not meet these requirements~~ A PD which is not described in the above list shall comply with the ~~following:~~ requirements set forth in the remainder of this section.

Table 33-32 defines three PSE transient test conditions and PD Types to which the conditions apply.

Table 33-32 Transient Test Conditions

PD Type	Transient Condition	Initial Voltage	Final Voltage	Vport-PSE-2P dv/dt	Source Resistance	Source Current
1	TR-1	VPort_PSE-2P min.	VPort_PSE-2P max.	2250V/s	Rch	Limited by Eq. 33-29
2,3,4	TR-2	VPort_PSE-2P min.	56V	2250V/s	Rch +/- 2.5%	
2,3,4	TR-3	VPort_PSE-2P min.	VPort_PSE-2P min. + 2.5V	3.5V/us	1.5 Ω +/- 2.5%	≥ 5A Capability

Fig. 33-36 shows operating bounds for the transients in table 33-32. The shaded regions begin with the application of the transient test and end at the times indicated in the figure. These shaded regions can exceed normal operating limits and are not included in the average and peak operating power requirements set forth in table 33-31.

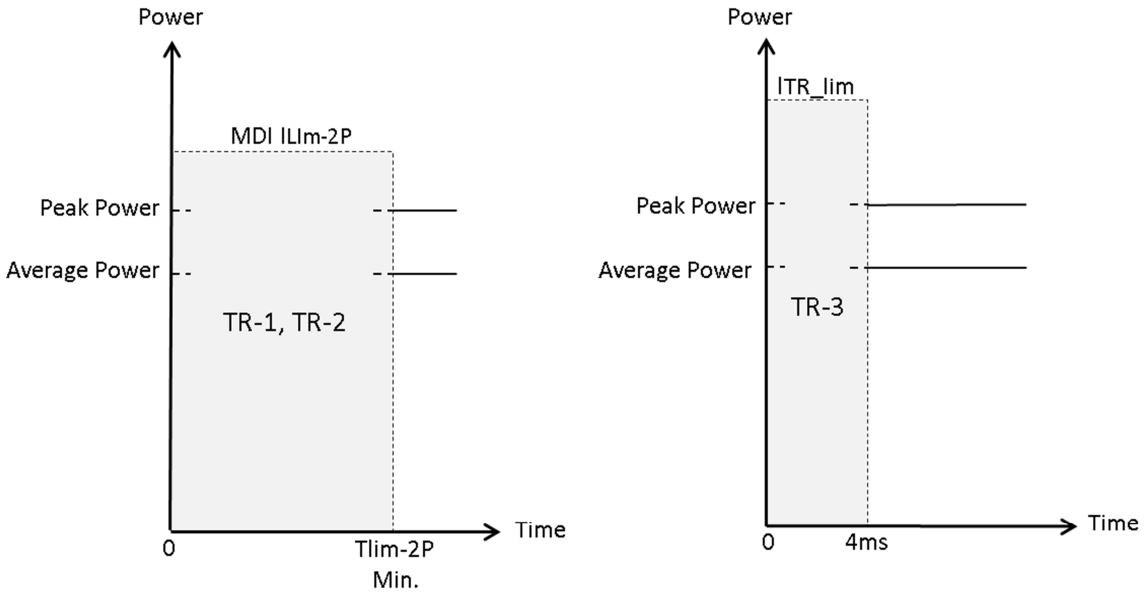

Fig. 33–36—Transient Test Conditions Operating Bounds

Fig. 33-36 shows transient test condition operating bounds, where:

Average Power — is PClass_PD or PClass_PD-2P as specified in Table 33-31 and section 33.3.8.2, or the average power limit specified in 33.3.8.2.1, if the applicable conditions for that section are met.

Peak Power — is Ppeak_PD or Ppeak_PD-2P, as specified in Table 33-31 and section 33.3.8.4, or the peak power limit specified in 33.3.4.1 if the conditions for that section are met.

TR-n — shows the operating bounds of the transient test condition, where n is the number of the test condition. These are not subject to the normal average and peak power limits.

Tlim-2P min. — is the minimum Tlim-2P value for the PD class, defined in table 33-19.

MDI Ilim-2P — is the limited source current defined in Eq. 33-29.

ITR_lim — is the maximum allowed PD current defined in table 33-33.

~~a) A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–36) after $T_{LIM\ 2P}$ min (see Table 33–19 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–32) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.~~

Type 1 PDs shall comply as follows:

When transient TR-1 is applied, the PD shall meet its normal average and peak operating power limits after TLIM-2P min (see Fig. 33-36).

~~b) A Type 2, Type 3, or Type 4 PD shall meet both of the following:~~

~~— The PD input current spike shall not exceed I_{TR_LIM}, as defined in Table 33–32, and shall settle below the PD upperbound template (see Figure 33–36 and Figure 33–37), or the PD extended template if the PD is assigned to Class 6 or Class 8 (see Figure 33–38), within 4 ms. During this test, the PD PI voltage is driven from $V_{Port\_PSE\ 2P}$ min to $V_{Port\_PSE\ 2P}$ min + 2.5 V at greater than 3.5 V/ µs, a source impedance within 2.5 % of 1.5 Ω, and a source that supports a current greater than 5.0 A.~~

~~— The PD shall not exceed the PD upperbound template beyond $T_{LIM\text{-}2P}$ min under worst-case current draw for the assigned Class under the following conditions. The input voltage source drives V_{PD} from $V_{Port\_PSE\ 2P}$ min to 56 V at 2250 V/s, the source impedance within 2.5 % of R_{Ch}, as defined in Table 33–1, and the voltage source limits the current to MDI $I_{LIM\text{-}2P}$ per Equation (33– 32).~~

Type 2, 3, and 4 PDs shall comply with both of the following:

When the PD is operating under its worst-case current draw for its assigned Class and transient TR-2 is applied, the PD shall meet its normal operating power limits after TLIM-2P min (see Fig. 33-36).

When transient TR-3 is applied, the peak current shall not exceed ITR_lim, as defined in Table 33-32, and the PD shall meet its normal operating power limits after 4ms (see Fig. 33-36).

These requirements apply to each pairset individually if the PD is a dual-signature PD.

Table 33–~~32~~33—PD current parameters during transients at the PSE PI

Parameter	Symbol	Unit	Min	Max	PD Type	PD signature	Assigned Class
Input spike current limit	I_{TR_LIM}	A		2.5	2		All
					3, 4	dual-signature	All
					3	single-signature	< 5
				3.0	3, 4	single-signature	≥ 5

The current limit per pairset at the MDI (MDI $I_{LIM\text{-}2P}$) is defined by Equation (33–~~32~~29):

$$\{pse_{\text{ILIM-2P min}}\}_{\text{mA}} < \{mdi_{\text{ILIM-2P}}\}_{\text{mA}} \leq \{pse_{\text{ILIM-2P min}}\}_{\text{mA}} + \ddot{5}_{\text{mA}} \qquad \text{(33–~~32~~29)}$$

where

pse$I_{LIM\text{-}2Pmin}$ is the PSE $I_{LIM\text{-}2P}$ min as defined in Table 33–19

mdi$I_{LIM\text{-}2P}$ is the per pairset current limit at the MDI (MDI $I_{LIM\text{-}2P}$)

The following shows the resulting content after the changes

33.3.8.5 Peak transient current

When the input voltage at the PI is static and in the range of $V_{Port\_PD\text{-}2P}$ defined by Table 33–31, the transient current drawn by a single-signature PD shall not exceed $I_{transient}$, defined in Table 33–31, in either polarity. A dual-signature PD shall not exceed $I_{transient}$ in either polarity per pairset under the same conditions. This limitation applies after inrush has completed (33.3.8.3) and before the PD has disconnected.

33.3.8.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.8. A single-signature PD includes Cport as defined in Table 33–31. A dual-signature PD includes CPort-2P as defined in Table 33–31 on each pairset.

The following PD configurations do not require any further consideration with regard to PSE transients:

1) Type 1 PD with an input capacitance of 180 µF or less.
2) Type 2 and single-signature Type 3 PDs with peak power not exceeding PClass_PD, and with an input capacitance of 180 µF or less.
3) Single-signature Type 4 PDs with peak power not exceeding PClass_PD, and with an input capacitance of 360µF or less.
4) Dual-signature Type 3 PDs with peak power draw not exceeding PClass_PD-2P, and with an input capacitance of 110 µF or less per pairset.
5) Dual-signature Type 4 PDs with peak power draw that does not exceed PClass_PD-2P and with an input capacitance of 180 µF or less per pairset.

A PD which is not described in the above list shall comply with the requirements set forth in the remainder of this section.

Table 33-32 defines three PSE transient test conditions and PD Types to which the conditions apply.

Table 33-32 Transient Test Conditions

PD Type	Transient Condition	Initial Voltage	Final Voltage	Vport-PSE-2P dv/dt	Source Resistance	Source Current
1	**TR-1**	VPort_PSE-2P min.	VPort_PSE-2P max.	2250V/s	Rch	Limited by Eq. 33-29
2,3,4	**TR-2**	VPort_PSE-2P min.	56V	2250V/s	Rch +/- 2.5%	
2,3,4	**TR-3**	VPort_PSE-2P min.	VPort_PSE-2P min. + 2.5V	3.5V/us	1.5 Ω +/- 2.5%	> 5A Capability

Fig. 33-36 shows operating bounds for the transients in table 33-32. The shaded regions begin with the application of the transient test and end at the times indicated in the figure. These shaded regions can exceed normal operating limits and are not included in the average and peak operating power requirements set forth in table 33-31.

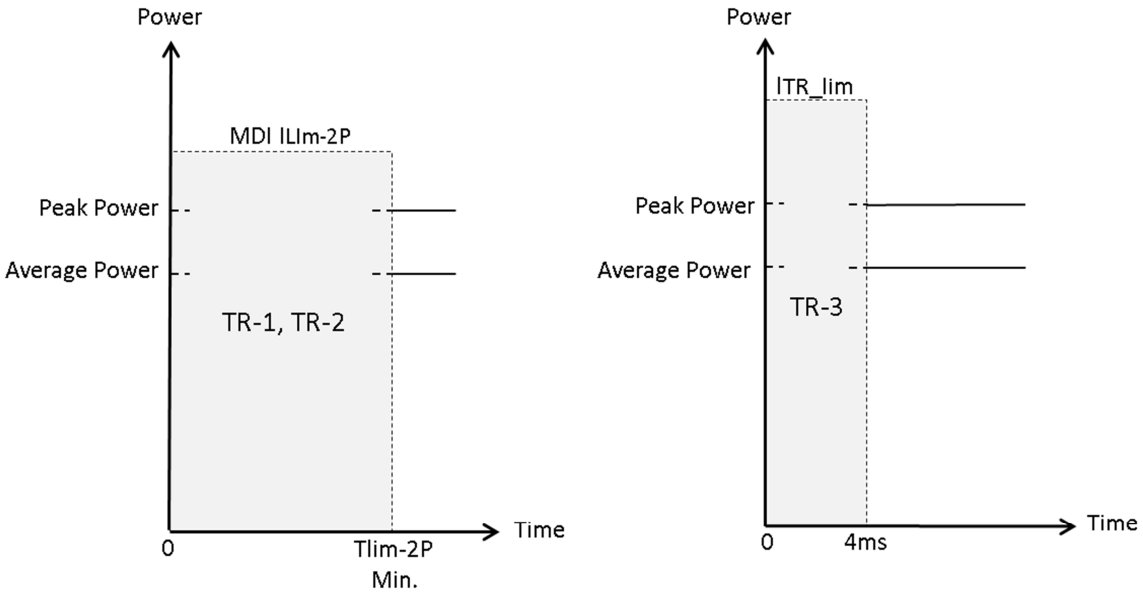

Fig. 33–36—Transient Test Conditions Operating Bounds

Fig. 33-36 shows transient test condition operating bounds, where:

Average Power	is PClass_PD or PClass_PD-2P as specified in Table 33-31 and section 33.3.8.2, or the average power limit specified in 33.3.8.2.1, if the applicable conditions for that section are met.
Peak Power	is Ppeak_PD or Ppeak_PD-2P, as specified in Table 33-31 and section 33.3.8.4, or the peak power limit specified in 33.3.4.1 if the conditions for that section are met.
TR-n	shows the operating bounds of the transient test condition, where n is the number of the test condition. These are not subject to the normal average and peak power limits.
Tlim-2P min.	is the minimum Tlim-2P value for the PD class, defined in table 33-19.
MDI Ilim-2P	is the limited source current defined in Eq. 33-29.
ITR_lim	is the maximum allowed PD current defined in table 33-33.

Type 1 PDs shall comply as follows:

When transient TR-1 is applied, the PD shall meet its normal average and peak operating power limits after TLIM-2P min (see Fig. 33-36).

Type 2, 3, and 4 PDs shall comply with both of the following:

When the PD is operating under its worst-case current draw for its assigned Class and transient TR-2 is applied, the PD shall meet its normal operating power limits after TLIM-2P min (see Fig. 33-36).

When transient TR-3 is applied, the peak current shall not exceed ITR_lim, as defined in Table 33-32, and the PD shall meet its normal operating power limits after 4ms (see Fig. 33-36).

These requirements apply to each pairset individually if the PD is a dual-signature PD.

Table 33–33—PD current parameters during transients at the PSE PI

Parameter	Symbol	Unit	Min	Max	PD Type	PD signature	Assigned Class
Input spike current limit	I_{TR_LIM}	A		2.5	2		All
					3, 4	dual-signature	All
					3	single-signature	< 5
				3.0	3, 4	single-signature	≥ 5

The current limit per pairset at the MDI (MDI I_{LIM-2P}) is defined by Equation (33–29):

$$\{pse_{\text{ILIM-2P min}}\}_{\text{mA}} < \{mdi_{\text{ILIM-2P}}\}_{\text{mA}} \leq \{pse_{\text{ILIM-2P min}}\}_{\text{mA}} + \ddot{5}_{\text{mA}} \quad (33\text{–}29)$$

where

pse$I_{LIM-2Pmin}$ is the PSE I_{LIM-2P} min as defined in Table 33–19
mdiI_{LIM-2P} is the per pairset current limit at the MDI (MDI I_{LIM-2P})

PICS Notes:

Remove PD62, PD63, PD64: These pertain to the removed graphs, and are redundant to PICS covering table 33-31 and the average power/peak power sections.

PD62	Specifications for P_{SSUT}	33.3.8.5	Operate below upperbound template defined in Figure 33–36	PDT1:M PDT2:M PDSS:M	Yes [ ] N/A [ ]
PD63	Specifications for P_{DSUT}	33.3.8.5	Operate below upperbound template defined in Figure 33–37	PDDS:M	Yes [ ] N/A [ ]
PD64	Specifications for P_{SSET}	33.3.8.5	Operate below extended upperbound template defined in Figure 33–38	WXYZ:M	Yes [ ] N/A [ ]

Remove PD68: It is already included as a subset of PD69.

PD68	Type 4 single-signature PDs that draw more than Class 8 P_{Class_PD}	33.3.8.6	Meet the requirements described in 33.3.8.6 for all values of input capacitance	PDT4*PDSS:M	Yes [ ] N/A [ ]
PD69	Behavior during transients at the PSE PI	33.3.8.6	As specified in 33.3.8.6	M	Yes [ ]