The following changes are made to D2.1 for differentiating between single-signature and dual-signature PDs.

1. Change 33.3.8.2.1 page 157 lines 37-40 as follows:

33.3.8.2.1 Input average power ~~for Class 6 and Class 8 PDs~~ exceptions

For Class 6 and Class 8 single-signature PDs, when additional information is available to the PD regarding actual channel DC resistance between the PSE PI and the PD PI, the PD may consume greater than P_{Class_PD} but shall not consume greater than P_{Class} at the PSE PI.

For Class 5 dual-signature PDs, when additional information is available to the PD regarding actual channel DC resistance between the PSE PI and the PD PI, the PD may consume greater than $P_{Class\_PD\text{-}2P}$ but shall not consume greater than $P_{Class\text{-}2P}$ at the PSE PI.

2. Change 33.3.8.4 page 158 lines 43-54 and page 159 lines 25-54 as follows.

33.3.8.4 Peak operating power

$V_{Overload\text{-}2P}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD} for single-signature PD or $P_{peak\text{-}2P\_PD}$ for dual-signature.

The following changes in lines 14-21 are covered by the approved comment #512 from D2.0 that was not implemented in D2.1.

At any static voltage at the PI, and any PD operating condition, with the exception described in 33.3.8.4.1, the peak power for single-signature PD shall not exceed P_{Class_PD} max for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–19 and 5% duty cycle for a single-signature PD. Peak operating power shall not exceed P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, with the exception described in 33.3.8.4.1, the peak power shall not exceed $P_{Class\_2P\_PD}$ max for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–19 and 5% duty cycle for a dual-signature PD. Peak operating power shall not exceed $P_{Peak\_2P\_PD}$.

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

For single-signature PDs, Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if P_{Peak_PD} requirements are met and the total input power is less than or equal to P_{Class_PD} max.

For dual-signature PDs, Ripple current content ($I_{Port\_2P\_ac}$) superimposed on the DC current level ($I_{Port\_2P\_dc}$) is allowed if $P_{Peak\_2P\_PD}$ requirements are met and the input power is less than or equal to $P_{Class\_2P\_PD}$ max.

The RMS, DC and ripple current shall be bounded by Equation (33–26):

$$I_{port\_RMS\_\max} = \begin{Bmatrix} \sqrt{\left(I_{Port\_dc}\right)^2 + \left(I_{Port\_ac}\right)^2} & for\ \sin gle-signature\ PD \\ \sqrt{\left(I_{Port\_2P\_dc}\right)^2 + \left(I_{Port\_2P\_ac}\right)^2} & for\ dual-signature\ PD \end{Bmatrix} \quad (33\text{-}26)$$

where

I_{Port_dc} is the DC component of the input current for a single-signature PD.
I_{Port_ac} is the RMS value of the AC component of the input current for a single-signature PD.
$I_{Port\_2P\_dc}$ is the DC component of the input current for a dual-signature PD.
$I_{Port\_2P\_ac}$ is the RMS value of the AC component of the input current for a dual-signature PD.

The maximum I_{Port_RMS} value for all PDs except those described in 33.3.8.2.1 and 33.3.8.4.1, over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (33–26):

3. Update Equation 33-27 as follows:

$$I_{port\_RMS\_max} = \left\{ \begin{array}{ll} \dfrac{P_{Class\_PD}}{V_{Port\_PD-2P}} & for\ single-signature\ PD \\ \dfrac{P_{Class\_2P\_PD}}{V_{Port\_PD-2P}} & for\ dual-signature\ PD \end{array} \right\} \quad \text{(33-27)}$$

where

*V*Port_PD-2P is the minimum specified input voltage at a PD pairset
*P*Class_PD is the maximum power, *P*Class_PD max, as defined in Table 33–28
*P*Class_2P_PD is the maximum power, *P*Class_2P_PD max, as defined in Table 33–28

The following changes in lines 45-50 are covered by the approved comment #512 from D2.0 that was not implemented in D2.1.

Peak power is defined in Table 33–28 and depends on the Class assigned by the PSE. The equations in Table 33–28 are used to approximate the ratiometric peak powers of Class 0 through Class 8. These equations may be used to calculate PPeak_PD or PPeak_PD-2P for Data Link Layer classification by substituting PClass_PD or PPeak_PD-2P with PDMaxPowerValue and for Autoclass by substituting PClass_PD with PAutoclass_PD.

4. Change 33.3.8.4.1 page 160 lines 2-23 as follows:

33.3.8.4.1 Peak operating power ~~for Class 6 and Class 8 PDs~~ exceptions

The following changes in lines 54-82 are covered by the approved comment #512 from D2.0 that was not implemented in D2.1 but now it is proposed with shorter wording.

For Class 6 and Class 8 single-signature PDs and for Class 5 dual-signature PDs, when additional information is available to the PD regarding actual channel DC resistance between the PSE PI and the PD PI, in any operating condition with any static voltage at the PI, the peak power shall not exceed PClass for single-signature PDs and Pclass-2P for dual-signature PDs at the PSE PI for more than TCUT-2P min, as defined in Table 33–19 and with 5% duty cycle. Peak operating power shall not exceed 1.05 × PPort_PD max.

For single-signature PDs, ~~R~~ripple current content (*I*Port_ac) superimposed on the DC current level (*I*Port_dc) is allowed if PPeak_PD requirements are met and the total input power is less than or equal to PClass at the PSE PI.

The maximum *I*Port_RMS value over the operating *V*Port_PD-2P range shall be defined by Equation (33–28):

$$I_{port\_RMS\_max} = \left\{ \frac{P_{Class}}{V_{PSE}} \right\}_A \quad \text{(33-28)}$$

where

*P*Class is the allocated Class power as defined in 33.2.7 and Equation (33–2)
*V*PSE is the voltage at the PSE PI as defined in 33.1.4

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

For dual-signature PDs, ripple current content (*I*Port_2P_ac) superimposed on the DC current level (*I*Port_2P_dc) is allowed if PPeak_2P_PD requirements are met and the total input power is less than or equal to PClass-2P at the PSE PI.

The maximum *I*Port_2P_RMS value over the operating *V*Port_PD-2P range shall be defined by Equation (33–27a):

$$I_{port\_2P\_RMS\_max} = \left\{ \frac{P_{Class-2P}}{V_{PSE}} \right\}_A \quad \text{(33-28a)}$$

where

*P*Class-2P is the allocated Class power as defined in 33.2.7 and Equation (33–3)
*V*PSE is the voltage at the PSE PI as defined in 33.1.4

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.