33.8.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT2	Type 2 PD implementation	33.3.2	PD is Type 2	O	Yes [ ] No [ ]
*PDT3	Type 3 PD implementation	33.3.2	PD is Type 3	O	Yes [ ] No [ ]
*PDT4	Type 4 PD implementation	33.3.2	PD is Type 4	O	Yes [ ] No [ ]
*PDSS	Single-signature PD	33.3.2	PD is single-signature	O	Yes [ ] No [ ]
*PDDS	Dual-signature PD	33.3.2	PD is dual-signature	O	Yes [ ] No [ ]
*PDCL	PD Classification	33.3.6	PD supports classification	PDT2:M	Yes [ ] No [ ]
*PDAC	Autoclass implementation	33.3.6.3	PD supports Autoclass	O	Yes [ ] No [ ]
*PDS-MPS	Short MPS implementation		PD supports short MPS	O	Yes [ ] No [ ]
*PDCLM2	Implementation supports 2Multiple-Event class signature	33.3.6	PD supports 2Multiple-Event class signature	PDT2:M PDT3:M PDT4:M	Yes [ ] No [ ]
*WXYZ	Implementation supports WXYZ	33.3.8.2.1, 33.3.8.4.1	PD supports behavior described in 33.3.8.2.1 and 33.3.8.4.1	PDT3:O PDT4:O	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PD supports Data Link Layer classification	PDT2:M PDT3:M PDT4:M	Yes [ ] No [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET1	Type 1 PSE implementation	33.1.3	Optional	O	Yes [ ] No [ ]
*PSET2	Type 2 PSE implementation	33.1.3	Optional	O	Yes [ ] No [ ]
*PSET3	Type 3 PSE implementation	33.1.3	Optional	O	Yes [ ] No [ ]
*PSET4	Type 4 PSE implementation	33.1.3	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.2	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	33.2.3	Midspan PSE implements Alternative A	MID:O~~2~~	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.5	Optional	O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	33.2.7	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*S~~1~~EPLC	Implementation supports Single-Event Physical Layer classification	33.2.7.1	Optional	O	Yes [ ] No [ ]
*M~~2~~EPLC	Implementation supports Multiple~~2~~-Event Physical Layer classification	33.2.7.2	Optional	PDT1:O PDT2:O PDT3:M PDT4:M	Yes [ ] No [ ]
*PSEAC	Autoclass implementation	33.2.7.3	PSE implements Autoclass	O	Yes [ ] No [ ]
*PA	Power Allocation	33.2.9	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.5.1.1.6	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.10.1.1	PSE monitors for AC MPS	PSET1:O.2~~3~~ PSET2:O.2	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.10.1.2	PSE monitors for DC MPS	PSET1:O.2~~3~~ PSET2:O.2 PSET3:M PSET4:M	Yes [ ] No [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3 PICS proforma tables for DTE Power via MDI

33.8.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.1	PDs and PSEs compatible at their PIs	M	Yes [ ]
COM2	Type 2 operation cabling	33.1.3.1	DC loop resistance 25 Ω or less. Requirement satisfied by category 5e components (cables, cords, and connectors)	M	Yes [ ]
COM3	Resistance unbalance	33.1.3.2	~~3 % or less~~Comply with requirements for twisted pair cabling as specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2	M	Yes [ ]

33.8.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.2	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	PSE permitted polarity configurations	33.2.4	To be associated with Alternative A or Alternative B listed in Table 33-4 corresponding with their Type	M	Yes [ ]
PSE3	Alternative A and Alternative B for Type 1, Type 2, or Type 3 PSEs	33.2.4	Implement Alternative A, Alternative B, or both	PSET1: M PSET2: M PSET3: M	Yes [ ] N/A [ ]
PSE4	Alternative A and Alternative B for Type 3 PSEs providing Class 5 or Class 6 power levels and Type 4 PSEs	33.2.4	Implement Alternative A and Alternative B	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE5	Alternative A and Alternative B for Type 1 and Type 2 PSEs	33.2.4	Not to operate on both Alternative A and Alternative B simultaneously	PSET1: M PSET2: M	Yes [ ] N/A [ ]
~~PSE2~~	~~Alternative A and Alternative B~~	~~33.2.4~~	~~Implement either Alternative A or Alternative B or both but not operate on same link segment simultaneously~~	~~M~~	~~Yes [ ] N/A [ ]~~
PSE6	PSE behavior for Type 1 and Type 2 PSEs	33.2.5	In accordance with state diagrams shown in Figure 33-13 and Figure 33-14	PSET1: M PSET2: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE7	PSE behavior for Type 3 and Type 4 PSEs	33.2.5	In accordance with state diagrams shown in Figure 33-15 to Figure 33-23	PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE3~~	~~PSE behavior~~	~~33.2.5~~	~~In accordance with state diagrams shown in Figure 33-13, Figure 33-13 continued, and Figure 33-20~~	~~M~~	~~Yes [ ]~~
~~PSE4~~	~~Detection, classification, and turn on timing~~	~~33.2.5.1~~	~~In accordance with Table 33-9, Table 33-15, and Table 33-17~~	~~M~~	~~Yes [ ]~~
PSE8	PSE performing detection only on Alternative B fails to detect a valid PD detection signature	332.5.1	Back off for at least T_{dbo} as specified in Table 33-17 before attempting another detection, except in the case of an open circuit as specified in 33.2.6.6	M	Yes [ ]
PSE9 ~~PSE5~~	Backoff voltage	33.2.5.1	Not greater than V_{Off}	M	Yes [ ]
PSE10	Alternative roles during 4-pair operation	33.2.5.1.1	Reversible provided that the roles established in IDLE are maintained in every other state	PSET3: O PSET4: O	Yes [ ] No [ ] N/A [ ]
PSE11 ~~PSE6~~	PSE variable definition permutations	33.2.5.4	Meet at least one allowable definition described in Table 33-6~~Table 33-7~~	M	Yes [ ]
PSE12 ~~PSE7~~	Type 2 PSE mutual identification	33.2.5.6	When powering a Type 2 PD, assigns a value of '2' to parameter_type if mutual identification is complete	PSET2: M	Yes [ ] N/A [ ]
PSE13 ~~PSE8~~	Type 2 PSE powering a Type 1 PD	33.2.5.6	Meets the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type}	PSET2: M	Yes [ ] N/A [ ]
PSE14	Type 3 and Type 4 PSE variable definition permutations	33.2.5.9	Meet at least one allowable definition described in Table 33-7	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE15	Type 1 and Type 2 PSE Class events	33.2.5.9	Issue no more than the Class they are capable of supporting	PSET1: M PSET2: M	Yes [ ] N/A [ ]
PSE16	Type 3 and Type 4 PSE Class events	33.2.5.9	Issue no more than the Class they are capable of supporting between the most recent time V_{PSE} was at V_{Reset} and a transition to POWER_UP	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE17	PD requests higher class than PSE can support	33.2.5.11	Assign the PD Class 3, 4, or 6, whichever is the highest that it can support	PSET3: M PSET4: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE18	PD requests higher class than PSE can support for Primary Alternative	33.2.5.11	Assign the PD Class 3, or 4, whichever is the highest that it can support	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE19	PD requests higher class than PSE can support for Secondary Alternative	33.2.5.11	Assign the PD Class 3, or 4, whichever is the highest that it can support	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE20 ~~PSE9~~	Applying power to a pairset	33.2.6	~~Not until a PD requesting power has been successfully detected.~~ Not until a valid signature has been successfully detected on that pairset, except as specified in 33.2.8.1	M	Yes [ ]
~~PSE10~~	~~Power pairs~~	~~33.2.6~~	~~Power supplied on the same pairs as those used for detection~~	~~M~~	~~Yes [ ]~~
PSE21	Connection check	33.2.6.1	Determine if both pairsets are connected to a single-signature PD or if the pairsets are connected to a dual-signature PD	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE22	Open circuit voltage and short circuit voltage during connection check	33.2.6.1	Meet the specifications in Table 33-9	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE23	Determining between single-signature and dual-signature PDs	33.2.6.1	Only for tests that result in a voltage at the PSE PI that is below V_{valid} max as specified in Table 33-9	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE24	Voltage on either pairset rises above V_{valid} max during connection check	33.2.6.1	Reset the PD by bringing the voltage at the PI below V_{off} max for at least T_{Reset}, before performing classification	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE25 ~~PSE11~~	Detecting PDs	33.2.6.2	Performed via the PSE PI	M	Yes [ ]
PSE26 ~~PSE12~~	PSE presents non-valid signature	33.2.6.2	As defined in Table 33–22	M	Yes [ ]
PSE27 ~~PSE13~~	Open circuit voltage and short circuit current	33.2.6.2	Meet specifications for V_{oc} and I_{sc} in Table 33–9	M	Yes [ ]
PSE28 ~~PSE14~~	Backdriven current	33.2.6.2	Not be damaged by up to 5 mA over the range of V_{Port_PSE}	M	Yes [ ]
PSE29 ~~PSE15~~	Output capacitance	33.2.6.2	C_{out} in Table 33–17	M	Yes [ ]
PSE30 ~~PSE16~~	Detection voltage with a valid PD signature connected	33.2.6.3	Meets V_{valid} in Table 33–9	M	Yes [ ]
PSE31 ~~PSE17~~	Detection voltage measurements	33.2.6.3	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE32 ~~PSE18~~	Control slew rate when switching detection voltages	33.2.6.3	Less than V_{slew} in Table 33–9	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE33 ~~PSE19~~	Accept as a valid signature	33.2.6.4	~~R_{good} and C_{good}, with up to V_{os} max and I_{os} max as defined in Table 33–10~~From a pairset with all of the characteristics specified in Table 33-10	M	Yes [ ]
PSE34 ~~PSE20~~	Reject as an invalid signature	33.2.6.5	Resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min	M	Yes [ ]
PSE35	Applying power to both pair-sets	33.2.6.7	Not until it is determined whether the attached PD is a candidate to receive power on both pairsets	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE36	4PID	33.2.6.7	A logical function of the detection state of both pairsets, the result of connection check, mutual identification, and of the Power via MDI TLV	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE37	4PID variable	33.2.6.7	Stored in PD_4pair_cand, defined in 33.2.5.9	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE38	PD_4pair_cand default value	33.2.6.7	Default value of FALSE	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE39	PSE provides V_{Class} with a current limitation of I_{Class_LIM}	33.2.7	Only for a pairset with a valid detection signature	M	Yes [ ]
PSE40	Polarity	33.2.7	Defined the same as V_{Port_PSE-2P} as shown in 33.2.4	M	Yes [ ]
PSE41	Timing specifications	33.2.7	Defined in Table 33-15	M	Yes [ ]
~~PSE21~~	~~Classification permutations~~	~~33.2.7~~	~~Meet one allowable permutation in Table 33–13~~	~~M~~	~~Yes [ ]~~
PSE42 ~~PSE22~~	Type 1 PSE does not implement Physical Layer classification	33.2.7	Assign all PDs to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE43	Type 2 PSE successful detection	33.2.7	Subsequently perform classification using at least one of the following: Multiple-Event Physical Layer classification; Multiple-Event Physical Layer classification and Data Link Layer classification; or Single-Event Physical Layer classification and Data Link Layer classification	PSET2: M	Yes [ ] N/A [ ]
PSE44	Type 3 and Type 4 PSE successful detection	33.2.7	Subsequently perform classification using at least one of the following: Multiple-Event Physical Layer classification; Multiple-Event Physical Layer classification and Data Link Layer classification	PSET3: M PSET4: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE45	Type 3 and Type 4 PSEs that will deliver 4-pair power attached to dual-signature PD	33.2.7	Classify both pairsets	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE46 ~~PSE23~~	Type 1 PSE failure to complete classification	33.2.7	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
~~PSE24~~ PSE47	Type 2-, Type3, and Type4 PSEs-that fail~~ure~~ to complete classification	33.2.7	Return to IDLE state	PSET2: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE48	PSE connected to dual-signature PD	33.2.7	Treat the requested power over each pairset independently	PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE25~~ PSE49	Provide V_{Class} for Single-Event Physical Layer classification	33.2.7.1	Limited to I_{Class_LIM} as defined by Table 33–15	S~~1~~EPLC:M	Yes [ ] N/A [ ]
~~PSE26~~ PSE50	Classification polarity for Single-Event Physical Layer classification	33.2.7.1	Same as V_{Port_PSE}	S~~1~~EPLC:M	Yes [ ] N/A [ ]
~~PSE27~~ PSE51	Classification timing for Single-Event Physical Layer classification	33.2.7.1	In accordance with T_{pdc} in Table 33–15	S~~1~~EPLC:M	Yes [ ] N/A [ ]
~~PSE28~~ PSE52	Measurement result of Single-Event Physical Layer classification I_{Class}	33.2.7.1	Classify PD according to observed current based on Table 33–14	S~~1~~EPLC:M	Yes [ ] N/A [ ]
~~PSE29~~ PSE53	Measurement timing of Single-Event Physical Layer classification I_{Class}	33.2.7.1	Measurement taken after the minimum relevant class event timing in Table 33–15	S~~1~~EPLC:M	Yes [ ] N/A [ ]
~~PSE30~~ PSE54	Class 4 result for Single-Event Physical Layer classification with a Type 1 PSE	33.2.7.1	Assign the PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
~~PSE31~~ PSE55	Type 1 PSE Single-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.7.1	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
~~PSE32~~ PSE56	Type 2 PSE Single-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.7.1	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE57	Type 2 PSE class and mark events	33.2.7.2	Provide a maximum of two class events and two mark events	MEPLC: M PSET2: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE58	Type 3 PSE class and mark events	33.2.7.2	Provide a maximum of four class events and four mark events for single-signature PDs and a maximum of three class events and three mark events on each pairset for dual-signature PDs unless a class reset event clears the class and mark event counts	MEPLC: M PSET3: M	Yes [ ] N/A [ ]
PSE59	Type 4 PSE class and mark events	33.2.7.2	Provide a maximum of five class events and five mark events for single-signature PDs and a maximum of four class events and four mark events on each pairset for dual-signature PDs unless a class reset event clears the class and mark event counts	MEPLC: M PSET4: M	Yes [ ] N/A [ ]
PSE60	Classification timing in the CLASS_EV1 state for Type 1 PSEs	33.2.7.2	In accordance with T_{pdc}	MEPLC: M PSET1: M	Yes [ ] N/A [ ]
PSE61	Classification timing in the CLASS_EV1 state for Type 2 PSEs	33.2.7.2	In accordance with T_{CLE1}	MEPLC: M PSET2: M	Yes [ ] N/A [ ]
PSE62	Classification timing in the CLASS_EV1_LCE_PRI, CLASS_EV1_LCE_SEC, CLASS_EV1_LCE_RESET_PRI, or CLASS_EV1_LCE_RESET_SEC states for Type 3 and Type 4 PSEs	33.2.7.2	In accordance with T_{LCE}	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE63	Total timing in the CLASS_EV1_LCE and CLASS_EV1_AUTO states for Type 3 and Type 4 PSEs	33.2.7.2	In accordance with T_{LCE}	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE64	Measure I_{Class} in the CLASS_EV1_AUTO state	33.2.7.2	After T_{Class_ACS}, referenced from the application of the first class event, to determine if the PD will perform Autoclass	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE65	In the CLASS_EV2, CLASS_EV2_PRI, or CLASS_EV2_SEC states	33.2.7.2	Provide V_{Class} to the PI or pairset, subject to the T_{CLE2} timing specification	MEPLC: M	Yes [ ] N/A [ ]
PSE66	In the CLASS_EV3, CLASS_EV3_PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_PRI, CLASS_EV4_SEC, or CLASS_EV5 states,	33.2.7.2	Provide V_{Class} to the PI or pairset, subject to the T_{CLE3} timing specification	MEPLC: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE67	Measure I_{Class} in all CLASS states except CLASS_EV1_AUTO	33.2.7.2	After T_{Class}	MEPLC: M	Yes [ ] N/A [ ]
PSE68	In the MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2_PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_PRI, MARK_EV3_SEC, or MARK_EV4 states	33.2.7.2	Provide V_{Mark} to the PI or pair-set, subject to the T_{ME1} timing specification	MEPLC: M	Yes [ ] N/A [ ]
PSE69	In the MARK_EV2 state for Type3 or Type 4 PSEs	33.2.7.2	Provide V_{Mark} to the PI or pair-set, subject to T_{ME1} timing specifications	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE70	In the MARK_EV2 state for Type 2 PSEs	33.2.7.2	Provide V_{Mark} to the PI or pair-set, subject to T_{ME2} timing specifications	MEPLC: M PSET2: M	Yes [ ] N/A [ ]
PSE71	In the MARK_EV_LAST, MARK_EV_LAST_PRI, or MARK_EV_LAST_SEC for Type 3 or Type 4 PSEs	33.2.7.2	Provide V_{Mark} to the PI or pair-set, subject to T_{ME2} timing specifications	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE72	I_{Class} measured equal to or greater than I_{Class_LIM} min for Type 2, Type3, or Type 4 PSEs	33.2.7.2	Return to the IDLE state	MEPLC: M PSET2: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE73	Class event currents	33.2.7.2	Limit to I_{Class_LIM}	MEPLC: M PSET2: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE74	Mark event currents	33.2.7.2	Limit to I_{Mark_LIM}	MEPLC: M PSET2: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE75	Class event and mark event voltages polarity	33.2.7.2	Same as defined for V_{Port_PSE-2P} in 33.2.4	MEPLC: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE76	Transition to the POWER_ON state after completion of Multi-ple-Event Physical Layer classification	33.2.7.2	Without allowing the voltage at the PI or pairset to go below V_{Mark} min, unless in the CLASS_RESET_PRI or CLASS_RESET_SEC states	MEPLC: M	Yes [ ] N/A [ ]
PSE77	PSE returns to IDLE state	33.2.7.2	Maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting new detection cycle	MEPLC: M	Yes [ ] N/A [ ]
PSE78	In the CLASS_RESET_PRI or CLASS_RESET_SEC state	33.2.7.2	Maintain the PI or pairset voltage at V_{Reset} for a period of at least T_{Reset} min	MEPLC: M	Yes [ ] N/A [ ]
PSE79	Type 3 or Type 4 PSE connected to a dual-signature PD, implementing 4PID based on classification and enabled for only one class event	33.2.7.2	Issue an initial three classification events to determine the Type of the connected PD, then transition to either the CLASS_RESET_PRI or CLASS_RESET_SEC state	MEPLC: M PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE33~~	~~In the CLASS_EV1 and CLASS_EV2 states, provide V_{Class}~~	~~33.2.7.2~~	~~As defined in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE34~~	~~Classification timing in CLASS_EV1 state~~	~~33.2.7.2~~	~~In accordance with T_{CLE1} in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE35~~	~~In the CLASS_EV1 and CLASS_EV2 states, measurement result I_{Class}~~	~~33.2.7.2~~	~~Classify PD according to Table 33–14~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE36~~	~~In the MARK_EV1 and MARK_EV2 states, provide V_{Mark}~~	~~33.2.7.2~~	~~In accordance with Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE37~~	~~Classification timing in MARK_EV1~~	~~33.2.7.2~~	~~In accordance with T_{ME1} in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE38~~	~~Classification timing in CLASS_EV2 state~~	~~33.2.7.2~~	~~In accordance with T_{CLE2} in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE39~~	~~Classification timing in MARK_EV2 state~~	~~33.2.7.2~~	~~In accordance with T_{ME2} in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE40~~	~~Type 2 PSE 2-Event Physical Layer classification if I_{Class} is greater than or equal to I_{Class_LIM} min~~	~~33.2.7.2~~	~~Returns to IDLE state~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE41~~	~~Current limitation during class events~~	~~33.2.7.2~~	~~Meet I_{Class_LIM}~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE42~~	~~Current limitation during mark events~~	~~33.2.7.2~~	~~Meet I_{Mark_LIM}~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE43~~	~~Measurement timing of 2-Event Physical Layer classification I_{Class}~~	~~33.2.7.2~~	~~Taken after the minimum relevant class event timing in Table 33–15~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE44~~	~~Class event and mark event voltages polarity~~	~~33.2.7.2~~	~~Same as V_{Port_PSE}~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
~~PSE45~~	~~Voltage level at PI when transition to POWER_ON state~~	~~33.2.7.2~~	~~Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to V_{Mark} min~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
~~PSE46~~	~~Return to IDLE state~~	~~33.2.7.2~~	~~Maintains PI voltage at V_{Reset} for at least T_{Reset} min before starting new detection cycle~~	~~2EPLC: M~~	~~Yes [ ] N/A [ ]~~
PSE80	Connected PD requests Auto-class during classification	33.2.7.3	Measure $P_{Autoclass}$	PSEAC: M	Yes [ ] N/A [ ]
PSE81	Power consumption	33.2.7.3	Defined as the highest average power measured throughout the period bounded bt T_{AUTO_PSE1} and T_{AUTO_PSE2}	PSEAC: M	Yes [ ] N/A [ ]
~~PSE47~~ PSE82	Power supply output	33.2.8	When the PSE provides power to the PI, conforms with Table 33–17	M	Yes [ ]
~~PSE48~~ PSE83	Load regulation	33.2.8.1	Met with (I_{Hold} max × V_{Port_PSE-2P} min) to ~~P_{Type} min~~maximum power per the PSE's assigned Class load step at a rate of change of at least 15 mA/µs max	M	Yes [ ]
~~PSE49~~ PSE84	Voltage transients	33.2.8.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE85	Type 3 or Type 4 PSE that has assigned Class 5 to 8 to a single-signature PD	33.2.8.1	Apply power to both pairsets while in the POWER_ON state	PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE50~~ PSE86	Voltage transients (30 µs to 250 µs) for Type 2, Type 3, and Type4 PSEs	33.2.8.2	No less than K_{Tran_lo} below V_{Port_PSE-2P} min and meet requirements of 33.2.8.7.	PSET2: M PSET3: M PSET4: M	Yes [ ]
~~PSE51~~ PSE87	Voltage transients (greater than 250 µs)	33.2.8.2	Meet V_{Port_PSE-2P} specification	M	Yes [ ]
~~PSE52~~ PSE88	Power feeding ripple and noise	33.2.8.3	Met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to ~~P_{Type} min~~the maximum power per the PSE's assigned Class for PSEs at static operating V_{Port_PSE-2P}	M	Yes [ ]
PSE89	PSE to source	33.2.8.4	I_{Con-2P} as specified in Equation 33-7	M	Yes [ ]
~~PSE53~~ PSE90	AC current waveform parameters	33.2.8.4	I_{Peak} minimum ~~equals Equation (33–12)~~(Equation 33-9), IPeak-2P-unb (Equation 33-10), and IPeak-2P (Equation 33-13) minimum for T_{CUT} minimum and 5% duty cycle minimum.	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE91	R_{PSE_max} and R_{PSE_min}	33.2.8.4.1	To conform with Equation 33-14	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE92	Measuring R_{PSE_max}, R_{PSE_min}, and $I_{Con-2P-unb}$	33.2.8.4.1	According to tests described in the normative Annex33B	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE93	Reach POWER_ON state on both pairsets for Type 3 and Type 4 PSEs that have assigned Class 5 to 8 to a single-signature PD	33.2.8.5	Within Tinrush-2P max, starting with the first pairset transitioning into the POWER_UP state, and where the second pairset transitions to POWER_UP anytime within this time period	PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE54~~ PSE94	~~Inrush current limit~~ $I_{Inrush-2P}$ and I_{Inrush} limits during POWER_UP state	33.2.8.5	~~PSE limits the maximum current sourced at the PI~~Per the requirements of Table 33-17	M	Yes [ ]
~~PSE55~~ PSE95	Inrush current template	33.2.8.5	Current sourced does not exceed the ~~PSE~~per-pairset inrush template in Figure 33–26 and Equation 33-15	M	Yes [ ]
PSE96	Minimum Inrush requirements for Type 4 PSEs connected to a single-signature PD	33.2.8.5.1	As specified in 33.2.8.5.1	PSET4: O	Yes [ ] N/A [ ]
PSE97	Minimum Inrush requirements for Type 4 PSEs connected to a dual-signature PD	33.2.8.5.1	As specified in 33.2.8.5.1	PSET4: O	Yes [ ] N/A [ ]
~~PSE56~~ PSE98	Short circuit condition	33.2.8.7	Remove power from ~~PI before I_{PSEUT} is exceeded. Equation (33–17) and Figure 33–14.~~a pairset of the PSE before the pairset current exceeds the "PSE upper-bound template" in Figure 33-27, Figure 33-28, and Figure 33-29	M	Yes [ ]
~~PSE57~~ PSE99	Short circuit current and time	33.2.8.7	In accordance with I_{LIM-2P} and T_{LIM-2P} in Table 33–17	M	Yes [ ]
~~PSE58~~ PSE100	Short circuit power removal	33.2.8.7	Begins within T_{LIM-2P} in Table 33–17	M	Yes [ ]
~~PSE59~~ PSE101	Turn off time	33.2.8.8	Applies to the discharge time from V_{Port_PSE-2P} to V_{Off} with a test resistor of 320 kΩ attached to the ~~PI~~pariset.	M	Yes [ ]
~~PSE60~~ PSE102	Turn off voltage	33.2.8.9	Applies to the PI voltage in the IDLE state	M	Yes [ ]
~~PSE61~~ PSE103	~~Current~~Intra-pair current unbalance	33.2.8.11	Applies to the two conductors of a power pair over the current load range in accordance with I_{unb} in Table 33–17.	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
~~PSE62~~ PSE104	Type 2, ~~-~~Type 3, and Type 4 Endpoint PSEs transmitting 100BASE-TX in the presence of (I_{unb} / 2)	33.2.8.11	Meet the requirements of 25.4.5	PSET2: M PSET3: M PSET4: M	Yes [ ]
PSE105	Type 4 PSE source power	33.2.8.12	Not more than PType max as specified in Table 33-17 calculated with a sliding window with a width of up to 4 seconds	PSET4: M	Yes [ ] N/A [ ]
PSE106	Reach POWER_ON state when connected to a single-signature PD for Type 3 and Type 4 PSEs	33.2.8.13	Within T_{pon} after completing detection on the last pairset	PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE107	PSE with less than Class 3 power available and connected to PD requesting more than the available power	33.2.9	Not to initiate power provision to one or both pairsets	M	Yes [ ]
~~PSE63~~ PSE108	Power allocation	33.2.9	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]
PSE109	MPS for Type1 and Type 2 PSEs	33.2.10.1	Monitor DC MPS component, AC MPS component, or both	PSET1: M PSET2: M	Yes [ ] N/A [ ]
PSE110	MPS for Type3 and Type 4 PSEs	33.2.10.1	Monitor only DC MPS component	PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE64~~ PSE111	PSE monitoring AC MPS component	33.2.10.1.1	Meets “AC Signal parameters” and “PSE PI voltage during AC disconnect detection” parameters in Table 33–18	AC:M	Yes [ ] N/A [ ]
~~PSE65~~ PSE112	PSE AC MPS component present	33.2.10.1.1	When AC impedance at the PI is equal to or lower than $\|Z_{ac1}\|$ in Table 33–18	AC:M	Yes [ ] N/A [ ]
~~PSE66~~ PSE113	PSE AC MPS component absent	33.2.10.1.1	When AC impedance at the PI equal to or greater than $\|Z_{ac2}\|$ in Table 33–18	AC:M	Yes [ ] N/A [ ]
~~PSE67~~ PSE114	Power removal	33.2.10.1.1	When AC MPS has been absent for a time duration greater than T_{MPDO}	AC:M	Yes [ ] N/A [ ]
PSE115	PSE DC MPS component requirements	33.2.10.1.2	Use the applicable IHold, IHold-2P, TMPS, and TMPDO values as defined in Table 33-17 depending on the connected PD’s Type and whether it is single-signature or dual-signature	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
~~PSE68~~ PSE116	~~PSE~~ DC MPS component present for a PSE powering a PD over a single pairset	33.2.10.1.2	I_{Port} is greater than or equal to $I_{Hold\text{-}2P}$ max for at least T_{MPS} min as specified in Table 33–17	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE69~~ PSE117	~~PSE~~ DC MPS component absent for a PSE powering a PD over a single pairset	33.2.10.1.2	I_{Port} is less than or equal to $I_{Hold\text{-}2P}$ min as specified in Table 33–17	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE70~~ PSE118	Power removal for a PSE powering a PD over a single pairset	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
~~PSE71~~ PSE119	Not remove power for a PSE poweing a PD over a single pairset	33.2.10.1.2	When the DC ~~current is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every~~ MPS has been present within the $T_{MPS} + T_{MPDO}$ window	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE120	DC MPS component present for Type 3 or Type 4 PSEs powering a single-signature PD over both pairsets	33.2.10.1.2	$I_{Port\text{-}2P}$ of the pairset with the highest current is greater than or equal to $I_{Hold\text{-}2P}$ max and the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity is greater than or equal to I_{Hold} max continuously for a minimum of T_{MPS}	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE121	DC MPS component absent for Type 3 or Type 4 PSEs powering a single-signature PD over both pairsets	33.2.10.1.2	$I_{Port\text{-}2P}$ of the pairset with the highest current is less than or equal to $I_{Hold\text{-}2P}$ min and the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity is less than or equal to I_{Hold} min	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE122	Power removal for Type 3 or Type 4 PSEs powering a single-signature PD over both pairsets	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE123	Not remove power for Type 3 or Type 4 PSEs powering a single-signature PD over both pairsets	33.2.10.1.2	When the DC MPS has been present within the $T_{MPS} + T_{MPDO}$ window	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE124	DC MPS component for Type 3 and Type 4 PSEs powering a dual-signature PD	33.2.10.1.2	Considered to be present or absent on each pairset independently	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE125	DC MPS component present on a pairset for Type 3 and Type 4 PSEs powering a dual-signature PD	33.2.10.1.2	$I_{Port\text{-}2P}$ is greater than or equal to $I_{Hold\text{-}2P}$ max continuously for a minimum of T_{MPS}	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSE126	DC MPS component absent for Type 3 and Type 4 PSEs powering a dual-signature PD	33.2.10.1.2	$I_{Port-2P}$ is less than or equal to $I_{Hold-2P}$ min	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE127	Power removal for Type 3 and Type 4 PSEs powering a dual-signature PD	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]
PSE128	Not remove power for Type 3 and Type 4 PSEs powering a dual-signature PD	33.2.10.1.2	When the DC MPS has been present on both pairsets within the T_{MPS} + T_{MPDO} window	DC:M PSET3: M PSET4: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power for Type 1 and Type 2 PDs	33.3.1	On either ~~set of PI conductor s~~pairset	PDT1:M PDT2:M	Yes [ ] N/A [ ]
PD2	Accept power for Type 3 and Type 4 PDs	33.3.1	On either pairset and on both	PDT3:M PDT4:M	Yes [ ] N/A [ ]
PD3 ~~PD2~~	Polarity insensitive for single-signature PDs with a power demand lower or equal to Class 4	33.3.1	Both Mode A and Mode B per Table 33–19	M	Yes [ ]
PD4 ~~PD3~~	Source power	33.3.1	The PD does not source power on its PI	M	Yes [ ]
PD5 ~~PD4~~	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
~~PD5~~	~~Underpowered Type 2 PD~~	~~33.3.2~~	~~If PD does not successfully observe 2-Event Physical Layer classification or Data Link Layer classification, conforms to Type 1 PD power restrictions and provides the user with an active indication if underpowered~~	~~PDT2:M~~	~~Yes [ ] N/A [ ]~~
~~PD6~~	~~Current unbalance~~	~~33.3.2~~	~~Type 2 PDs meet the requirements of 25.4.5 in presence of (I_{unb}/2)~~	~~PDT2:M~~	~~Yes [ ] N/A [ ]~~
PD6 ~~PD7~~	Type 1 and Type 2 PD behavior	33.3.3	According to state diagram shown in Figure 33-31~~Figure 33–32~~	PDT1:M PDT2:M	Yes [ ] N/A [ ]
PD7	Single-signature Type 3 and Type 4 PD behavior	33.3.3	According to state diagram shown in Figure 33-32	PDT3*PDSS:M PDT4*PDSS:M	Yes [ ] N/A [ ]
PD8	Dual-signature Type 3 and Type 4 PD behavior	33.3.3	According to state diagram shown in Figure 33-33	PDT3*PDDS:M PDT4*PDDS:M	Yes [ ] N/A [ ]
PD9 ~~PD8~~	Valid and non-valid detection signatures	33.3.4	Presented between positive V_{PD} and negative V_{PD} on each set of pairs defined in 33.3.1	M	Yes [ ]
PD10 ~~PD9~~	~~Non-valid detection signature~~ Type 1, Type 2, or single-signature Type 3 or Type 4 PD powered over only one pairset	33.3.4	~~When powered, present an invalid signature on the set of pairs not drawing power~~Present a nonvalid detection signature on the unpowered pairset	PDT1:M PDT2:M PDT3*PDSS:M PDT4*PDSS:M~~M~~	Yes [ ] N/A [ ]~~Yes [ ]~~
PD11	Type 3 and Type 4 dual signature PD powered over only one pairset	33.3.4	Present a valid detection signature over the unpowered pairset	PDT3*PDDS:M PDT4*PDDS:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD12 ~~PD10~~	Valid detection signature	33.3.4	Characteristics defined in Table 33–21	M	Yes [ ]
PD13 ~~PD11~~	Non-valid detection signature	33.3.4	Exhibit one or both of the characteristics described in Table 33–22	M	Yes [ ]
PD14	Type 3 and Type 4 dual-signature PD presents valid detection signature	33.3.5	As defined in Table 33-21 on: Mode A regardless of any voltage applied to Mode B between 0Vand 57V, and Mode B regardless of any voltage applied to Mode A between 0V and 57V	PDT3*PDDS:M PDT4*PDDS:M	Yes [ ] N/A [ ]
PD15	Present valid detection signature on Mode A for single-signature PDs	33.3.5	When no voltage or current is applied to Mode B	PDSS:M	Yes [ ] N/A [ ]
PD16	Present invalid detection signature on Mode A for single-signature PDs	33.3.5	When any voltage between 10.1V and 57V is applied to Mode B	PDSS:M	Yes [ ] N/A [ ]
PD17	Maximum power drawn across all input voltages and operational modes for Type 3 and Type 4 PDs	33.3.6	In accordance with the advertised Class during Physical Layer classification of the PD	PDT3:M PDT4:M	Yes [ ] N/A [ ]
PD18	Physical Layer classification	33.3.6	Mandatory for PDs	M	Yes [ ]
PD19	Multiple-Event classification	33.3.6	Mandatory for Type 2, Type 3, and Type 4 PDs	PDT2:M PDT3:M PDT4:M	Yes [ ] N/A [ ]
PD20	DLL classification	33.3.6	Mandatory for Type 2, Type 3 Class 4 to 6, Type 4, and dual-signature PDs	PDT2:M PDT3:M PDT4:M PDDS:M	Yes [ ] N/A [ ]
PD21	Underpowered Type 2, Type 3, and Type 4 PDs	33.3.6	If PD does not successfully observe a Multiple-Event Physical Layer classification or Data Link Layer classification, conform to Type 1 PD power restrictions and provide the user with an active indication if underpowered	PDT2:M PDT3:M PDT4:M	Yes [ ] N/A [ ]
~~PD12~~	~~PD classifications~~	~~33.3.6~~	~~Meets at least one permutation listed in Table 33–13~~	~~PDCL:M~~	~~Yes [ ]~~
PD22 ~~PD13~~	PD implementing ~~2 Event~~Multiple-Event-class signature	33.3.6.1	Returns ~~Class 4~~ class_sig_A in accordance with the maximum power draw, P_{Class_PD}, as specified in Table 33-24 and thte responses specified in Table 33-24	~~PDCL2:M~~ PDCLM:M	Yes [ ] N/A [ ]
PD23 ~~PD14~~	Type 2 PD classification behavior	33.3.6.1	Conforms to electrical specifications in Table 33–26	PDT2:M	Yes [ ] N/A [ ]
PD24 ~~PD15~~	Classification signature	33.3.6.1	As defined in Table 33–23	PDCL:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD25 ~~PD16~~	Classification signature	33.3.6.1	One classification signature during classification	PDCL:M PDT1:M PDT2:M	Yes [ ] N/A [ ]
~~PD17~~	~~2-Event class signature~~	~~33.3.6.2~~	~~Class 4 in accordance with the maximum power draw as specified in Table 33–28~~	~~PDCL2:M~~	~~Yes [ ] N/A [ ]~~
PD26	Multiple-Event Physical Layer classification during DO_-CLASS_EVENT1 and DO_-CLASS_EVENT2 states	33.3.6.2	Present class_sig_A as defined in Table 33-24 and Table 33-25	PDCLM: M	Yes [ ] N/A [ ]
PD27	Multiple-Event Physical Layer classification during the DO_-CLASS_EVENT3, DO_-CLASS_EVENT4, DO_CLASS_EVENT5, and DO_CLASS_EVENT6 states	33.3.6.2	Present class_sig_B as defined in Table 33-24 and Table 33-25	PDCLM: M	Yes [ ] N/A [ ]
PD28	Multiple-Event Physical Layer classification during DO_-CLASS_EVENT_AUTO state	33.3.6.2	Present class_sig_0 as defined in 33.3.6.3	PDCLM: M	Yes [ ] N/A [ ]
PD29 ~~PD18~~	~~2-Event~~Multiple-Event-class signature behavior	33.3.6.2	As defined in Table 33–26	~~PDCL2:M~~ PDCLM: M	Yes [ ] N/A [ ]
PD30 ~~PD19~~	Type 2,-Type 3, and Type 4 PD electrical requirements	33.3.6.2	As defined by Table 33–28 of the Type defined in its pse_power_~~type~~level state variable	PDT2:M PDT3:M PDT4:M	Yes [ ] N/A [ ]
PD31	Class signature for dual-signature PDs	33.3.6.2	Advertise on each pairset corresponding with Class 1, 2, 3, 4, or 5 as defined in Table 33-25	PDDS:M	Yes [ ] N/A [ ]
PD32	Type 3 or Type 4 dual-signature PD powered over only one pairset	33.3.6.2	Present a valid classification signature on the unpowered pairset	PDT3*PDDS:M PDT4*PDDS:M	Yes [ ] N/A [ ]
PD33	Short MPS PD	33.3.6.2	Set short_mps to TRUE if the first class event is longer than T_{LCE_PD} max	PDS-MPS:M	Yes [ ] N/A [ ]
PD34 ~~PD20~~	Mark event current and ~~2-Event~~Mulitple-Event class signature	33.3.6.2.1	Draw I_{Mark} and present a non-valid detection signature as defined in Table 33–22	~~PDCL2:M~~ PDCLM: M	Yes [ ] N/A [ ]
PD35 ~~PD21~~	Mark event current limits	33.3.6.2.1	Not exceed I_{Mark} when voltage at the PI enters V_{Mark} as defined in Table 33–26	~~PDCL2:M~~ PDCLM: M	Yes [ ] N/A [ ]
PD36 ~~PD22~~	PD current draw	33.3.6.2.1	I_{Mark} ~~until the PD transitions from~~when-in DO_MARK_EVENT state ~~to the IDLE state~~	~~PDCL2:M~~ PDCLM: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD37	Responding to Physical Layer Classification for Autoclass PDs	33.3.6.3	As specified in 33.3.6.1 and 33.3.6.2 with the exception that the PD shall change its current during the first class event to class signature '0' no earlier than T_{ACS} min and no later than T_{ACS} max, as defined in Table 33-27	PDAC:M	Yes [ ] N/A [ ]
PD38	After power up for Autoclass PDs	33.3.6.3	Draw its highest required power, $P_{Autoclass\_PD}$, subject to P_{Class_PD}, throughout the period bounded by T_{AUO_PD1} and T_{AUTO_PD2}, measured from when V_{Port_PD} rises above V_{Port_PD} min	PDAC:M	Yes [ ] N/A [ ]
PD39	Power draw for Autoclass PDs	33.3.6.3	Not more than the power consumed during the time from T_{AUO_PD1} to T_{AUTO_PD2} at any point until V_{Port_PD} falls below V_{Reset_th}, unless the PD successfully negotiates a higher power level, up to the advertised Physical Layer classification, through Data Link Layer classification as define in 33.6	PDAC:M	Yes [ ] N/A [ ]
PD40 ~~PD23~~	PSE identification	33.3.7	Identify as ~~Type 1 or Type 2~~ a Type lower or equal to its own Type~~(see Figure 33–32)~~	~~PDT2:M~~ M	Yes [ ]
PD41 ~~PD24~~	PD power supply	33.3.8	Operate within the characteristics in Table 33–28	M	Yes [ ]
PD42 ~~PD25~~	PD turn on voltage	33.3.8.1	PD turns on at a voltage less than or equal to V_{On_PD}	M	Yes [ ]
PD43 ~~PD26~~	PD stay on voltage	33.3.8.1	Stay on for all voltages in the range of $V_{Port\_PD\text{-}2P}$	M	Yes [ ]
PD44 ~~PD27~~	PD turn off voltage	33.3.8.1	Turn off at a voltage less than $V_{Port\_PD\text{-}2P}$ min and greater than $V_{Off\_PD\text{-}2P}$	M	Yes [ ]
PD45 ~~PD28~~	Startup oscillations	33.3.8.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD46	Input average power for certain Class6 and Class 8 PDs	33.3.8.2.1	Not to consume power greater than P_{Class} at the PSE PI	WXYZ:M	Yes [ ] N/A [ ]
PD47 ~~PD29~~	P_{Port_PD} definition for Type 1, Type 2, Type 3 single-signature, and Type 4 single-signature PDs	33.3.8.2.2	When PD is ~~fed by~~supplied with $V_{Port\_~~PD~~PSE\text{-}2P}$ min to $V_{Port\_~~PD~~PSE\text{-}2P}$ max with R_{Ch} (as defined in Table 33–1) in series	~~M~~PDT1: M PDT2:M PDT3*PDSS:M PDT4*PDSS:M	Yes [ ] N/A [ ]
PD48	$P_{Port\_PD\text{-}2P}$ definition for dual-signature PDs	33.3.8.2.2	When PD is supplied with $V_{Port\_PSE\text{-}2P}$ min to $V_{Port\_PSE\text{-}2P}$ max with R_{Ch} (as defined in Table 33–1) in series	PDDS:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD49 ~~PD30~~	~~Type 2~~ PD input inrush current	33.3.8.3	~~With pse_power_type state set to 2 prior to power on, operate as a Type 1 PD for at least T_{delay} min~~Draw less than I_{Inrush_PD} and I_{Inrush_PD-2P} from $T_{Inrush-2P}$ min until $T_{delay-2P-min}$	M~~PDT2: M~~	Yes [ ] ~~N/A [ ]~~
PD50	P_{Class_PD} and P_{Peak_PD} for single-signature PDs assigned to Class 1, 2, or 3	33.3.8.3	Within $T_{Inrush-2P}$ min as defined in Table 33-17	PDSS:M	Yes [ ] N/A [ ]
PD51	P_{Class_PD-2P} and P_{Peak_PD-2P} for dual-signature PDs assigned to Class 1, 2, or 3	33.3.8.3	Within $T_{Inrush-2P}$ min as defined in Table 33-17 on that pairset	PDDS:M	Yes [ ] N/A [ ]
PD52	PD inrush requirements	33.3.8.3	with the PSE behavior described in 33.2.8.5	M	Yes [ ]
PD53 ~~PD31~~	Input inrush current	33.3.8.3	Limited by the PD if C_{port} or CPort-2P is greater than or equal to 180 µF so that I_{Inrush_PD} max and I_{Inrush_PD-2P} max are met~~is satisfied.~~	M	Yes [ ]
PD54 ~~PD32~~	Peak power for any PD opearting condition, with the exception described in33.3.8.4.1	33.3.8.4	Not to exceed P_{Class_PD} max for more than T_{CUT-2P} min and 5% duty cycle	M	Yes [ ]
PD55 ~~PD33~~	Peak operating power	33.3.8.4	Not to exceed $P_{Peak-PD}$ ~~max~~	M	Yes [ ]
PD56 ~~PD34~~	RMS, DC, and ripple current	33.3.8.4	Bounded by Equation (33–25)	M	Yes [ ]
PD57 ~~PD35~~	Maximum I_{Port_RMS} for all PDs except those described in 33.3.8.2.1 and 33.3.8.4.1 over the operating V_{Port_PD-2P}	33.3.8.4	Defined by Equation (33–26)	~~M~~!WXYZ:M	Yes [ ]
PD58	Peak power for certain Class 6 and Class 8 PDs	33.3.8.4.1	Not to exceed P_{Class} at the PSE PI for more than T_{CUT-2P} min as defined in Table 33-17 and with 5% duty cycle	WXYZ:M	Yes [ ] N/A [ ]
PD59	Maximum I_{Port_RMS} value over the operating V_{Port_PD-2P} range	33.3.8.4.1	Defined by Equation 33-27	WXYZ:M	Yes [ ] N/A [ ]
PD60 ~~PD36~~	Peak transient current	33.3.8.5	Not to exceed 4.70 mA/µs in either polarity	~~M~~PDSS:M	Yes [ ] N/A [ ]
PD61	Peak transient current for dual-signature PDs	33.3.8.5	Not to exceed 4.70 mA/µs in either polarity per pairset	PDDS:M	Yes [ ] N/A [ ]
PD62 ~~PD37~~	Specifications for P~~I~~$_{~~PD~~SSUT}$	33.3.8.5	Operate below upperbound template defined in Figure 33–37	PDT1:M PDT2:M PDSS:M	~~Yes [ ]~~ Yes [ ] N/A [ ]
PD63	Specifications for P_{DSUT}	33.3.8.5	Operate below upperbound template defined in Figure 33-38	PDDS:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD64	Specifications for P_{SSET}	33.3.8.5	Operate below extended upperbound template defined in Figure 33-39	WXYZ:M	Yes [ ] N/A [ ]
PD65	Presence of transients at the PSE PI	33.3.8.6	Continue to operate without interruption	M	Yes [ ]
PD66	C_{Port} for single-signature PDs	33.3.8.6	Defined in Table 33-28	PDSS:M	Yes [ ] N/A [ ]
PD67	$C_{Port-2P}$ for dual-signature PDs	33.3.8.6	On each pairset as defined in Table 33-28	PDDS:M	Yes [ ] N/A [ ]
PD68	Type 4 single-signature PDs that draw more than Class 8 P_{Class_PD}	33.3.8.6	Meet the requirements described in 33.3.8.6 for all values of input capacitance	PDT4*PDSS:M	Yes [ ] N/A [ ]
PD69 ~~PD38~~	Behavior during transients at the PSE PI	33.3.8.6	As specified in 33.3.8.6	M	Yes [ ]
PD70 ~~PD39~~	Ripple and noise	33.3.8.7	As specified in Table 33–28 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD71 ~~PD40~~	Ripple and noise specification	33.3.8.7	For all operating voltages in the range defined by V_{Port_PD-2P} in Table 33–28	M	Yes [ ]
PD72 ~~PD41~~	Ripple and noise presence	33.3.8.7	Operates in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD73 ~~PD42~~	Classification stability	33.3.8.8	Class signature valid within T_{Class_PD} and remains valid for the duration of the classification period	M	Yes [ ]
PD74 ~~PD43~~	Backfeed voltage	33.3.8.9	Mode A and Mode B per 33.3.8.9	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PD75	Pair-to-pair unbalance for single-signature PDs assigned Class 5 or higher	33.3.8.10	Not to exceed $I_{Con-2P-unb}$ for longer than T_{CUT-2P} min as described in 33.3.8.10	PDSS:M	Yes [ ] N/A [ ]
PD76	Pair-to-pair unbalance for dual-signature PDs	33.3.8.10	Not to exceed I_{Con-2P} for longer than T_{CUT-2P} min as described in 33.3.8.10	PDDS:M	Yes [ ] N/A [ ]
PD77 ~~PD44~~	~~Maintain power signature~~PD that requires power from the PI	33.3.9~~33.3.8.10~~	~~PD provides~~Provide a valid MPS at the PI ~~as defined in 33.3.8.10~~	M	Yes [ ]
PD78	MPS for single-signature PDs	33.3.9	Consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD} measured at the PI	PDSS:M	Yes [ ] N/A [ ]
PD79	MPS for dual-signature PDs	33.3.9	Consist of current draw equal to or above I_{Port_MPS-2P} on each powered pairset independently for a minimum duration of T_{MPS_PD} measured at the PI	PDDS:M	Yes [ ] N/A [ ]
PD80	Show input impedance for Type 1, Type 2, or connected to Type 1 or Type 2 PSE PDs	33.3.9	With resistive and capacitive components defined in Table 33-31	PDT1:M PDT2:M	Yes [ ] N/A [ ]
PD81	T_{MPS} measurement for Type 3 and Type 4 PDs	33.3.9	With a series resistance representing the worst case cable resistance between the measurement point and the PD PI	PDT3:M PDT4:M	Yes [ ] N/A [ ]
PD82	MPS for Autoclass PDs	33.3.9	Use I_{Port_MPS} associated with the PD Class asigned by the PSE during Physical Layer classification	PDAC:M	Yes [ ] N/A [ ]
PD83 ~~PD45~~	Powered PDs that n~~N~~o longer require power, and identify the PSE as Type 1 or Type 2	33.3.8.10	Remove both ~~components of the Maintain Power Signature~~the current draw and impedance components of the MPS	M	Yes [ ]
PD84	Powered PDs that no longer require power and identify the PSE as Type 3 or Type 4		Remove the current draw component of the MPS	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	33.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Insulation breakdown	33.4.1	No breakdown of insulation during electrical isolation tests	M	Yes [ ]
EL4	Isolation resistance	33.4.1	At least 2 MΩ, measured at 500 Vdc after electrical isolation tests	M	Yes [ ]
EL5	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ] N/A [ ]
EL8	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL9	Environment B requirements for PSE that supports 4-pair power	33.4.1.1.2	Switch more negative conductor		Yes [ ] N/A [ ]
EL10 ~~EL9~~	Fault tolerance for PIs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL11 ~~EL10~~	Fault tolerance for PSE PIs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ] N/A [ ]
EL12 ~~EL11~~	Common-mode fault tolerance	33.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL13 ~~EL12~~	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value)	M	Yes [ ]
EL14 ~~EL13~~	Common-mode to differential-mode impedance balance for transmit and receive pairs	33.4.3	Exceeds value in Table 33–32 for all supported PHY speeds	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
EL15 ~~EL14~~	Common-mode AC output voltage	33.4.4	Magnitude while transmitting data and with power applied does not exceed ~~50 mV peak when operating at 10 Mb/s and 50 mV peak-to-peak when operating at 100 Mb/s or greater~~the values in Table 33-33 while operating at the specified speed, when measured over the specified bandwidth	M	Yes [ ]
~~EL15~~	~~Frequency range for common-mode AC output voltage measurement~~	~~33.4.4~~	~~From 1 MHz to 100 MHz~~	~~M~~	~~Yes [ ]~~
EL16	Common-mode AC output voltage measurement	33.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL17	Noise from an operating 10/100/1000 Mb/s PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4	M	Yes [ ]
EL18	Noise from an operating 2.5GBASE-T, 5GBASE-T, or 10GBASE-T PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed the requirements Equation 33-33 under the conditions specified in 33.4.4	M	Yes [ ]
EL19 ~~EL18~~	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]
EL20 ~~EL19~~	100BASE-TX Type 2, Type 3, and Type 4 Endpoint PSE and PD channel unbalance	33.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	33.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current	33.4.2	Does not exceed I_{LIM} max	M	Yes [ ]
PSEEL3	Limitation of electromagnetic interference.	33.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL4	Alternative A Type 2 Midspan PSEs that support 100BASE-TX	33.4.8	Enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–17) or meet 33.4.9.2.	MIDA: M	Yes [ ] N/A [ ]
PSEEL5	Insertion of Midspan at FD	33.4.9	Comply with the guidelines specified in 33.4.9 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE	33.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL8	DC continuity in power injecting pairs	33.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan PSE inserted as a “connector” or “telecom outlet”	33.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE NEXT when operating with 10/100/1000 Mb/s or 2.5GBASE-T	33.4.9.1.1	Meet values detemined by Equation (33–34) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT when operating with 5GBASE-T	33.4.9.1.1	Meet the values determined by Equation 33-34 from 1 MHz to 250 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE NEXT when opearting with 10GBASE-T	33.4.9.1.1	Meet the values determined by Equation 33-35 from 1 MHz to 500 MHz, but not greater than 75 dB	MID:M	Yes [ ] N/A [ ]
PSEEL13 ~~PSEEL11~~	Midspan PSE Insertion Loss when operating with 10/100/1000 Mb/s or 2.5GBASE-T	33.4.9.1.2	Meet values determined by Equation (33–36) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL14	Midspan PSE Insertion Loss when operating at 5GBASE-T	33.4.9.1.2	Meet values determined by Equation (33–36) from 1 MHz to 250 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL15	Midspan PSE Insertion Loss when operating at 10GBASE-T	33.4.9.1.2	Meet values determined by Equation (33–36) from 1 MHz to 500 MHz	MID:M	Yes [ ] N/A [ ]
PSEEL16 ~~PSEEL12~~	Midspan PSE Return Loss	33.4.9.1.3	Meet or exceed values in Table 33–34 ~~for transmit and receive pairs from 1 MHz to 100 MHz~~	MID:M	Yes [ ] N/A [ ]
PSEEL17 ~~PSEEL13~~	Work area or equipment cable Midspan PSE	33.4.9.1.4	Meet the requirements of this clause and the specifications for a ~~Category 5~~ (jumper) cord ~~as specified in ISO/IEC 11801-2002 or ANSI/TIA-568-C.2-ANSI/TIA/EIA-568-A:1995~~ for insertion loss, NEXT, and return loss for transmit and receive pairs, as defined in Table 33-35	MID:M	Yes [ ] N/A [ ]
PSEEL18	Midspan PSE maximum link delay	33.4.9.1.5	Not to exceed 2.5 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL19	Midspan PSE maximum link delay skew	33.4.9.1.5	Not to exceed 1.25 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL20	Midspan PSE PSANEXT loss for 2.5G/5G/10GBASE-T	33.4.9.1.8	Meet or exceed the values determined using the equations shown in Table 33-36a for all specified frequencies	MID:M	Yes [ ] N/A [ ]
PSEEL21	PSANEXT loss values greater than 67 dB	33.4.9.1.8	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]
PSEEL22	Midspan PSE PSAFEXT loss for 2.5G/5G/10GBASE-T	33.4.9.1.8	Meet or exceed the values determined using the equations shown in Table 33-37b for all specified frequencies	MID:M	Yes [ ] N/A [ ]
PSEEL23	PSAFEXT loss values greater than 67 dB	33.4.9.1.8	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]
PSEEL24 ~~PSEEL14~~	Alternative A Midspan PSE signal path requirements	33.4.9.2	Exceed transfer function gain expressed in Equation (33–38) from 0.10 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL25 ~~PSEEL15~~	Alternative A Midspan PSE signal path requirements bias current	33.4.9.2	Met with DC bias current between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	33.4.4	The PIs that require power terminated as illustrated in Figure 33–44	M	Yes [ ]

33.8.3.7 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.5	Access to register definitions defined in 33.5.1 via interface described in 22.2.4 or 45.2 or equivalent	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.5.1	Register address 11 for control functions and register address 12 for status functions	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.5.1	Remain high until read via the management interface	MAN:M	Yes [ ] N/A [ ]
MF4	Latching register bit after read	33.5.1	Assumes a value based on the current state of the condition it monitors	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:~~6~~8)	33.5.1.1.1	Not affected by writes and return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF6	Data Link Layer classification not supported	33.5.1.1.3	Ignore writes to bit 11.5 and return a value of zero when read	MAN* !DLLC:M	Yes [ ] N/A [ ]
MF7	Data Link Layer classification supported	33.5.1.1.3	Ignore writes to bit 11.5 and return a value of one when function cannot be disabled	MAN* DLLC:M	Yes [ ] N/A [ ]
MF8	Enable/disable Data Link Layer classification capability	33.5.1.1.3	Capability enabled by setting bit 11.5 to one and disabled by setting bit 11.5 to zero	MAN* DLLC:M	Yes [ ] N/A [ ]
MF9	Physical Layer classification not supported	33.5.1.1.4	Ignore writes to bit 11.4 and return a value of zero when read	MAN* !CL:M	Yes [ ] N/A [ ]
MF10	Physical Layer classification supported	33.5.1.1.4	Ignore writes to bit 11.4 and return a value of one when function cannot be disabled	MAN* CL:M	Yes [ ] N/A [ ]
MF11	Enable/disable Physical Layer classification	33.5.1.1.4	Function enabled by setting bit 11.4 to one and disabled by setting bit 11.5 to zero	MAN* CL:M	Yes [ ] N/A [ ]
MF12	Pair Control Ability not supported	33.5.1.1.5	Ignore writes to bits 11.3:2	MAN* !PCA:M	Yes [ ] N/A [ ]
MF13	Writes to 11.3:2 when Pair Control Ability not supported	33.5.1.1.5	Return the value that reports the supported PSE Pinout Alternative	MAN* !PCA:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
MF14	Bits 11.3:2 set to '01'	33.5.1.1.5	Forces the PSE to use Alternative A	MAN* PCA:M	Yes [ ] N/A [ ]
MF15	Bits 11.3:2 set to '10'	33.5.1.1.5	Forces the PSE to use Alternative B	MAN* PCA:M	Yes [ ] N/A [ ]
MF16	Pair control ability bit (12.0)	33.5.1.1.5	A value of one sets the mr_pse_alternative variable	MAN* PCA:M	Yes [ ] N/A [ ]
MF17	PSE function disabled	33.5.1.1.6	Setting PSE Enable bits 11.1:0 to a '00', also the MDI shall function as it would if it had no PSE function	MAN:M	Yes [ ] N/A [ ]
MF18	PSE function enabled	33.5.1.1.6	Setting PSE Enable bits 11.1:0 to a '01'	MAN:M	Yes [ ] N/A [ ]
MF19	PSE enable bits (11.1:0)	33.5.1.1.6	Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power	MAN:M	Yes [ ] N/A [ ]
MF20	PSE Type electrical parameters bit (12.15)	33.5.1.2.1	Set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. Set to one when set_parameter_type is set to 2	MAN:M	Yes [ ] N/A [ ]
MF21	Data Link Layer classification enabled bit (12.14)	33.5.1.2.2	Set to one when the PSE state diagram sets true pse_dll_enabled. Set to zero when the PSE state diagram sets false pss_dll_enabled	MAN:M	Yes [ ] N/A [ ]
MF22	Power denied bit (12.12)	33.5.1.2.4	A value of one indicates power has been denied or removed due to an error condition	MAN:M	Yes [ ] N/A [ ]
MF23	Power denied bit implementation	33.5.1.2.4	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF24	Valid signature bit (12.11)	33.5.1.2.5	One indicates a valid signature has been detected. Set to one when mr_valid_signature transitions from FALSE to TRUE.	MAN:M	Yes [ ] N/A [ ]
MF25	Valid signature bit implementation	33.5.1.2.5	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF26	Invalid signature bit (12.10)	33.5.1.2.6	One indicates an invalid signature has been detected. Set to one entering SIGNATURE_INVALID state	MAN:M	Yes [ ] N/A [ ]
MF27	Invalid signature bit implementation	33.5.1.2.6	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

Item	Feature	Subclause	Value/Comment	Status	Support
MF28	Short circuit bit (12.9)	33.5.1.2.7	Bit indicates a short circuit condition has been detected. Set to one entering ERROR_DELAY state.	MAN:M	Yes [ ] N/A [ ]
MF29	Short circuit bit implementation	33.5.1.2.7	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF30	Overload bit (12.8)	33.5.1.2.8	Bit indicates an overload condition has been detected. Set to one when entering the ERROR_DELAY_OVER state	MAN:M	Yes [ ] N/A [ ]
MF31	Overload bit implementation	33.5.1.2.8	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF32	MPS absent bit (12.7)	33.5.1.2.9	Bit indicates an MPS Absent condition has been detected. Set to one when transitions directly from POWER_ON to IDLE state when MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.10	MAN:M	Yes [ ] N/A [ ]
MF33	MPS Absent bit implementation	33.5.1.2.9	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.8 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	33.6	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	33.6.1	Meet mandatory parts of IEEE Std 802.1AB-2009	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	33.6.1	Meet requirements for Type, Length, and Value (TLV) defined in 79.3.2 and the Power via MDI Measurements TLV in 79.3.7	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	33.6.1	Meet state diagrams defined in 33.6.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	Type 2, Type 3, and Type 4 PSE LLDPDU	33.6.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL6	Type 1 PSE LLDPDU	33.6.2	Transmitted when Data Link Layer classification is ready as indicated by pse_dll_ready	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD Data Link Layer classification ready	33.6.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL8	PD requested power value change	33.6.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE allocated power value change	33.6.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL10	PSE power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–49	DLLC:M	Yes [ ] N/A [ ]
DLL11	PD power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–50	DLLC:M	Yes [ ] N/A [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.

33.8.3.9 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.7.1	Conforms to IEC 60950-1:2001	M	Yes [ ]
ES2	PSE classified as a limited power source	33.7.1	In accordance with IEC 60950-1:2001	M	Yes [ ]
ES3	Safety	33.7.1	Comply with all applicable local and national codes	M	Yes [ ]
ES4	Telephony voltages	33.7.5	Application thereof described in 33.7.5 not result in any safety hazard	M	Yes [ ]
ES5	Limitation of electromagnetic interference	33.7.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

33.8.3.10 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.7.1	Limited Power Source in accordance with IEC 60950-1:2001	M	Yes [ ]

Annex 33B PICS

Item	Feature	Subclause	Value/Comment	Status	Support
A33B1	Current unbalance requirements (R_{PSE_min}, R_{PSE_max}, and $I_{Con-2P-unb}$	33B	Met with R_{Load_max} and R_{Load_min} as specified by Table 33B-1	M	Yes [ ]
A33B2	Pair-to-pair balance actively controlled and changes effective resistance	33B.2	Use current unbalance measurement method described in 33B.3	M	Yes [ ]
A33B3	Current Unbalance requirement	33B.3	Met for any pairs of the same polarity and with the load resistances per Table 33B-1	M	Yes [ ]
A33B4	Channel common mode resistance less than 0.1 ohm	33B.4	PSE tested with (R_{load_min} - R_{chan}) and (Rl_{oad_max} - R_{chan}) to meet $I_{Con-2P-unb}$ requirements and R_{PSE_min} and R_{PSE_max} conformance to Equation 33-14	M	Yes [ ]

Copyright © 2016 IEEE. All rights reserved.
This is an unapproved IEEE Standards draft, subject to change.