Contents

TDL #460 from D2.0. (D2.1 clause 33.3.8.3 page 158 lines 35-41)

Comment #460 from D2.0 text:

"If a PD has a larger C Port or C Port-2P value, then the PD shall limit the input inrush current such that I Inrush_PD max and I Inrush_PD-2P max, as defined in Table 33-28, are met."

Very true, but also redundant to the requirement a few paragraphs above:
"PDs shall draw less than I Inrush_PD and I Inrush_PD-2P from T Inrush-2P min until T delay-2P min."

SuggestedRemedy

Remove the "If a PD has a larger..." sentence.
ACCEPT.
Add to the TDL: Darshan, Make sure removal of shall on page 149, line 30 in D2.0 does not cause issues.

Analysis:

The intent of legacy PDs (Type 1 and Type 2):

For Cport<180uF:

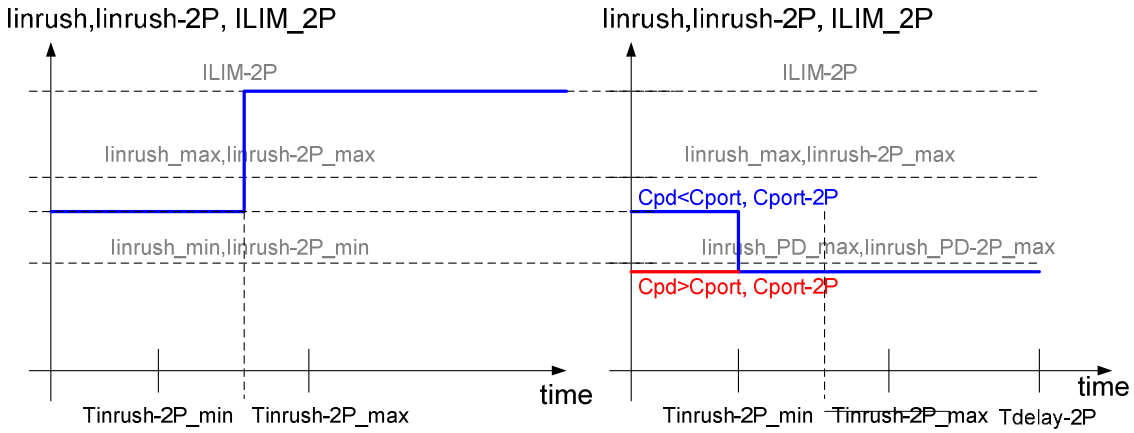
-The PSE is limiting the current to a range between Iinrush_min to Iinrush_max for a time duration of Tinrush=50 to 75msec, both per Table 33-19.

-The PD has to finish POWER_UP within Tinrush_min=50msec. During this time, the PD doesn't need to meet Iinrush_PD limits in Table 33-31 since PSE is limiting the current to higher values than Table 33-31.

-If PD doesn't finish Iinrush within 50msec it can limit Iinrush by itself after 50msec for unspecified time OR it can limit Inrush per Table 33-31 for the whole POWER_UP period including t<Tinrush_min and after Tdelay.

For Cport>180uF:

PD has to limit the Inrush per Table 33-31 or all the POWER_UP duration including t<Tinrush_min and after Tdelay if inrush process was not ended.



PSE behavior for Cpd with any value of Cport, Cport-2P

PD behavior for Cpd with any value of Cport, Cport-2P

33.3.8.3 Input inrush current

The total PD inrush time duration is defined as beginning with the application of input voltage at the PI when VPD crosses the PD power supply turn on voltage, VOn_PD as defined in Table 33–31, and ends after Tdelay-2P.

The inrush current is the initial current drawn by the PD, which is used to charge CPort or CPort-2P. The inrush current is limited by the PSE. A PD may limit the inrush current below IInrush_PD and IInrush_PD-2P to allow for large values of CPort and CPort-2P.

Issue 1: Lines 38-39 just say that PD may limit Iinrush howevr it doesn't specify the conditions as we had prior deleting the text in D2.1. The conditions where when C> CPort and CPort-2P and in this case the A PD shall ~~may~~ limit the inrush current below IInrush_PD and IInrush_PD-2P

PDs shall draw less than IInrush_PD and IInrush_PD-2P from TInrush-2P min until Tdelay-2P min. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to change the available current from the POWER_UP to the POWER_ON limits. A PD can meet this requirement (to draw less than IInrush_PD and IInrush_PD-2P from TInrush-2P min until Tdelay-2P min) by either having CPort or CPort-2P charged within TInrush-2P min, or, by limiting the input inrush current.

Issue 2 line 46-47: It is not clear which requiremet. We need to add text that clarifies that the requirement is "PDs shall draw less than IInrush_PD and IInrush_PD-2P from TInrush-2P min until Tdelay-2P min". See proposed changes.

Single-signature PDs assigned to Class 1, 2, or 3 shall conform to PClass_PD and PPeak_PD within TInrush-2P min as defined Table 33–19. Type 3 and Type 4 dual-signature PDs assigned to Class 1, 2, or 3 shall conform to PClass_PD-2P and PPeak_PD-2P within TInrush-2P min as defined Table 33–19 on that pairset.

Issue 3, lines 53-55:
-What are the requirements for single-signature PDs with class 4-8?
-What are the requirements for dual-signature PDs with class 4-5?
-Why we need the term "assigned class" here? What will happen if we will not have it. The same issue for all Inrush related text.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after Tinrush-2P min. See 33.2.8.5 for details.

The PD shall meet the inrush requirements with the PSE behavior described in 33.2.8.5.

Editor's Note: These paragraphs have changed as a result of MR1277 and further work. Do not change this paragraph without consulting the request of MR1277.

CPort in Table 33–31 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. CPort-2P in Table 33–31 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–35 for a simpli-fied PSE-PD CPort and CPort-2P interpretation model.

Input inrush currents at startup, IInrush_PD and IInrush_PD-2P, as defined in Table 33–19, are limited by the PSE if CPort < 180 µF for single-signature PDs assigned to Class 0 to 6, and if CPort < 360 µF for PDs assigned to Class 7 or 8.
Input inrush current at startup, IInrush PD-2P, is limited by the PSE if CPort-2P < 110 µF for dual-signature PDs assigned to Class 0 to 4 and if CPort-2P < 180 µF for dual-signature assigned to Class 5.

Issue 4, lines 68-72:
-Missing requirements for e.g. when Cport > 180uF etc. The deleted text was addressing this case with shall.
-The deleted text was a modification for exiting legacy text with a "shall". PD shall limit IInrush_PD and IInrush_PD-2P when Cport >180uF etc.
-The deleted text force PD to limit the current when Cport>180uF etc. also for Tinrush-2P<50msec.

[The following text was deleted in D2.1 and is the reason for this work.
If a PD has a larger CPort or CPort-2P value, then the PD shall limit the input inrush current such that IInrush_PD max and IInrush_PD-2P max, as defined in Table 33–28, are met for the whole (*)*PD inrush time duration(*)* .]
(*) new addition that clarifies the point.
[To verify with David Abramson if his logical arguments at September meeting still valid after the above analysis]

Analysis Summary:

1. We touched legacy text. See Annex A.
2. It is not clear from the D2.1 text what are the requirements from Iinrush-PD and Iinrush_PD-2P when Cport>180uF etc. as in D2.0 and in 802.3at.
3. In D2.0 and in 802.3at it is a "shall" requirement that PD shall limit IInrush_PD max and IInrush_PD-2P max if Cport>180uF etc. which applies to the whole inrush duration and not just from Tinrush_2P_min to Tdelay-2P.
4. The other issues in this document will be addressed after getting some feedbacs from the group to verify if they are real issues or I missed something here.

Recommendations:

To restore the D2.1 deleted text:

If a PD has a larger CPort or CPort-2P value, then the PD shall limit the input inrush current such that IInrush_PD max and IInrush_PD-2P max, as defined in Table 33–28, are met for the whole PD inrush time duration .

Annex – A – IEEE802.3at

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99 % of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180$ µF, as specified in Table 33–11.

If $C_{Port} \geq 180$ µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

Legacy text.

This is modification of the legacy text in D2.0 in order to support 802.3bt for e.g. Cport>180uF etc.

If a PD has a larger CPort or CPort-2P value, then the PD shall limit the input inrush current such that IInrush_PD max and IInrush_PD-2P max, as defined in Table 33–28, are met.

We can see that the legacy text or its modification in D2.0 has value in terms of that PD has to limit Iinrush_PD and Iinrush_PD-2P for t<Tinrush-2P_min as well if larger CPort or CPort-2P value are used.
This requirement must be with "shall".