D2.1 COMMENT #55.
TDL #254 from D2.0. (D2.1, Figure 97, Page 97, line 23)

Comment:

The text supports PSE that needs to know the PD class by issuing 3 class events, class reset and then starting 1st class event again. This is required for power management for PSE or PSE host to know PD actual advertised class so when PSE has the power, I can supply it for the PD that is working now in reduced operating mode. The above is regardless if PSE support DLL or not.

Users would like to have their PD getting the full power they need and are OK that for some time the PD will work with reduced power mode but not all the time.

In addition, Users don't like the idea to turn off the port and start the process again just to know the advertised class due to system shutdown time limits so in this way power can be increased up to the advertised class without waiting valuable time.
This behavior is not covered by the PSE single—signature state machine.

Suggested Remedy:

1. Add the missing state machine that follows the following principles:
   a) PSE may issue 3 class events for class code detection when PSE available power is < 5 (i.e. available power is 30W or less which results with < 3 class events).
   b) When PSE issues 3 class events and class reset, the first the first class event doesn't have to be long class event if PSE planes at the end of the process after class reset to issue 1 or 2 class events. This will save classification time.
   c) In addition to (b), no need to implement start tclassacs_timer in the first class event (**CLASS_EV1_LCE state)** prior to class reset.

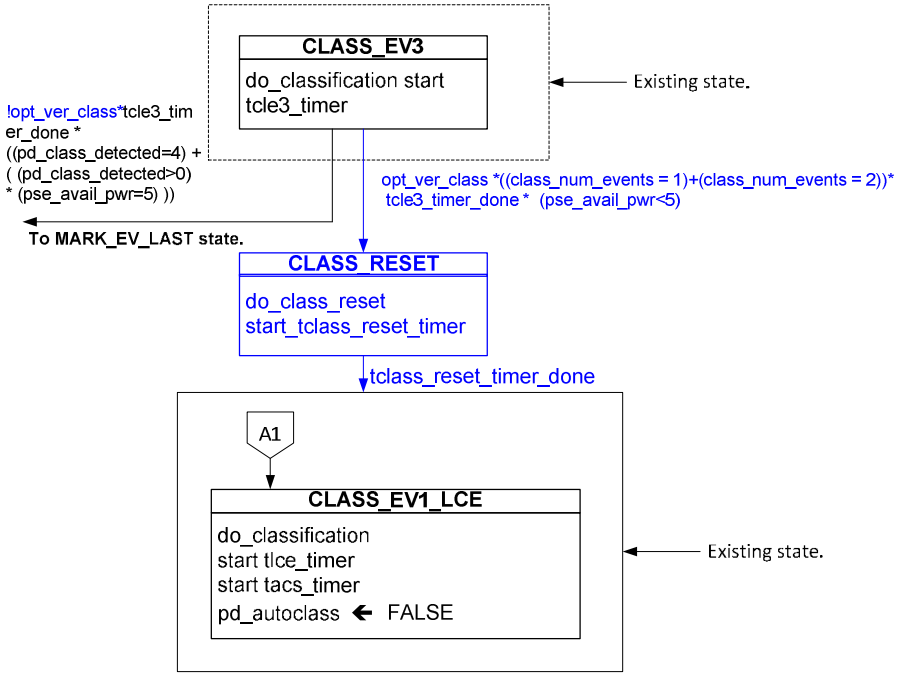
Proposed Baseline

1. **Add the following variable to the variable list of 33.2.5.9.:**

opt_ver_class

Optional variable that controls the use of issuing 3 class events for detecting the single-signature PD physical layer advertised class followed by class reset and then starting again **CLASS_EV1_LCE**.
If PSE has prior knowledge that opt_ver_class is going to be set to TRUE then the PSE may use TCLE1 timing instead of TLCE timing for the first class event that is used prior using class reset.
Values:
FALSE: The PSE is not using a sequence of 3 class events followed by class reset.
TRUE: The PSE is using a sequence of 3 class events followed by class reset.

2. **Add the following SM part to Figure 33-18 (Type 3 and Type 4 PSE single-signature classification state diagram**


CLASS_EV3
do_classification start
tcle3_timer
Existing state.
!opt_ver_class*tcle3_tim
er_done *
((pd_class_detected=4) +
((pd_class_detected>0)
* (pse_avail_pwr=5)))
To MARK_EV_LAST state.
opt_ver_class *((class_num_events = 1)+(class_num_events = 2))*
tcle3_timer_done * (pse_avail_pwr<5)
CLASS_RESET
do_class_reset
start_tclass_reset_timer
tclass_reset_timer_done
A1
CLASS_EV1_LCE
do_classification
start tlce_timer
start tacs_timer
pd_autoclass ← FALSE
Existing state.