## Comment #39 D2.1
## (TDL for comments #214 , #248, #304, #239 and #195 from D2.0)

**From TDL List for comment #214 response and remedy + new issues:**

1. To update DLL SM for single and dual PDs and PSEs with the following objectives:
   -Power Demotion
   -Addressing cases when power is not sufficient for one of the modes or both modes.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, clause 33.5 PD/PSE DLL power state machine (Figures 33-48 and 33-49) and its variable list.
3. To figure out how DLL state machine uses variables from Physical Layer class (this is about the response for commnet #248 from D2.0 regarding the question How DLL will know if PD is single–signature PD or dual-sig PD? (The problem is that the PSE know it from the physical layer. The PD can't know unless the PD is using existing PD variable that tells the PD DLL if it is single or dual signature PD.)
2. Editing constant and variables per Type 1,2 and Type 3 and 4 in separate clauses where applicable.

**Concept (Option 2)**
(Option 1 is shown in separate document)

1. Keep 33.5 for Type 1-4 system.
2. Duplicate 33.5.2, 33.5.3 with similar content with the additional suffix "_(M)" whenever relevant.
3. Duplicate PSE and PD DLL state machine and add the suffix "-mode(M)" to all variables and constants.
4. Duplicate Table 33-41
5. Duplicate all other related DLL and TLV tables.
6. Add additional TLV fields in the TLV structure (page 218) for:
   -PDRequestedPowerValue_ModeA
   -PDRequestedPowerValue_ModeB
   -PSEAllocatedPowerValue_ModeA
   -PSEAllocatedPowerValue_ModeB

## Proposed Remedy:

Adopt darshan_11_1116_option2.pdf if ready for the meeting. If not, keep it in the TDL.

**Proposed Baseline starts here**

Adding missing tables for dual-signature PDs.

### 1. Add the following table after Table 33-15 on clause 33.2.7, page 108 line 35

**Table 33–15a—Relation of assigned Class and DLL for dual-signature PDs**

| PSEAllocatedPowerValue_(M) | Assigned Class |
|---|---|
| 1 – 39 | 1 |
| 40 – 65 | 2 |
| 66 – 130 | 3 |
| 131 – 255 | 4 |
| 256 – 400 | 5 |

### 2. Add the following table after Table 33-25 on clause 33.3.6.1, 150 page 150 line 20

**Table 33–25a—Relation of assigned Class and DLL for dual-signature PDs**

| PDMaxPowerValue_(M) | Assigned Class |
|---|---|
| 1 – 39 | 1 |
| 40 – 65 | 2 |
| 66 – 130 | 3 |
| 131 – 255 | 4 |
| 256 – 400 | 5 |

## 3. Make the following changes to 33.5

## 33.5 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Single-signature PDs advertising a Class 4 signature or higher and Type 3 and Type 4 dual-signature PDs support Data Link Layer classification (see 33.3.6). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

### 33.5.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and may support the Power via MDI Measurements TLV defined in 79.3.8; and shall support the control state diagrams defined in 33.5.3.

### 33.5.2 Data Link Layer classification timing requirements

Type 2, 3, and 4 PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.5.4, 33.5.3.3).

A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.5.3.3).

Type 1 PDs that implement Data Link Layer classification and Type 2, 3, and 4 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.7, 33.5.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PSE allocated power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PD requested power value" field is different from the previously communicated value.

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PD requested power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PSE allocated power value" field is different from the previously communicated value.

### 33.5.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively.

When singl-signature PDs are supported, PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–48. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–49.

When dual-signature PDs are supporte, PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–48a. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–49a. See 33.3.5.3.1.7.

#### 33.5.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 33.2.5.2.

### 33.5.3.1.1 Single-signature system Constants

Variables PD_DLLMAX_VALUE, PD_INITIAL_VALUE, and PSE_INITIAL_VALUE, are quantized to fit the available resolution. Additional information on power levels for Classes 6 and 8 may be found in 33.3.8.2.1.

#### ~~33.5.3.2.1~~ 33.5.3.1.1.1. Type 1 and Type 2 PSE constants

PSE_INITIAL_VALUE
This value is derived as follows from parameter_type and the mr_pd_class_detected (33.2.5.6) variable used in the Type 1 and Type 2 PSE state diagram defined in Figure 33–13:

| parameter_type | PSE_INITIAL_VALUE |
|---|---|
| 1 | 130 |
| 1 | 39 |
| 1 | 65 |
| 1 | 130 |
| 1 | 130 |
| 2 | 255 |

#### ~~33.5.3.2.2~~ 33.5.3.1.1.2 Single-signature system Type 3 and Type 4 PSE constants

PD_DLLMAX_VALUE
This value is derived from pd_max_power variable (33.3.3.7) described as follows:

| pd_max_power | PD_DLLMAX_VALUE |
|---|---|
| 0 | 130 |
| 1 | 39 |
| 2 | 65 |
| 3 | 130 |
| 4 | 255 |
| 5 | 400 |
| 6 | 600 |
| 7 | 620 |
| 8 | 999 |

PD_INITIAL_VALUE
This value is derived as follows from the pd_max_power (33.3.3.7) variable used in the PD state Diagram; defined in Figure 33–31 and Figure 33-32:

| pd_max_power | PD_INITIAL_VALUE |
|---|---|
| 0 | ≤ 130 |
| 1 | ≤ 39 |
| 2 | ≤ 65 |
| 3 | ≤ 130 |
| 4 | ≤ 255 |
| 5 | ≤ 400 |
| 6 | ≤ 600 |
| 7 | ≤ 620 |
| 8 | ≤ 900 |

PSE_INITIAL_VALUE
This value is derived as follows from pd_allocated_power, as defined in 33.2.5.11, which is used in the Type 3 and Type 4 PSE state diagrams in 33.2.5.12:

| pd_allocated_power | PSE_INITIAL_VALUE |
|---|---|
| 1 | 130 |
| 1 | 39 |
| 1 | 65 |
| 1 | 130 |
| 1 | 130 |
| 2 | 255 |
| 3 | 400 |
| 3 | 600 |
| 4 | 620 |
| 4 | 900 |

### ~~33.5.3.3~~ 33.5.3.1.2 Single-signature system Variables

The PSE power control state diagram (Figure 33–49) and PD power control state diagram (Figure 33–50) use the following variables:

MirroredPDRequestedPowerValue
The copy of the PD Requested Power Value field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of MirroredPDRequestedPowerValue.
Values: 1 through 999
When a PD mode is not active, the value shall be set to zero.

MirroredPDRequestedPowerValueEcho
The copy of the PD Requested Power Value filed in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).
Values: 1 through 999
When a PD mode is not active, the value shall be set to zero.

MirroredPSEAllocatedPowerValue
The copy of the PSE Allocated Power Value field in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of MirroredPSEAllocatedPowerValue.
Values: 1 through 999
When a PD mode is not active, the value shall be set to zero.

MirroredPSEAllocatedPowerValueEcho

The copy of the PSE Allocated Power Value field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).

PDRequestedPowerValueEcho

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

PDMaxPowerValue

Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.8.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PDMaxPowerValue.

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

PDRequestedPowerValue

Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.8.2) the PD requests. This power value is encoded according to Equation (79–1), where *X* is the decimal value of PDRequestedPowerValue. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.8.2) the PD ever draws. This power value is encoded according to Equation (79–2), where *X* is the decimal value of PSEAllocatedPowerValue. This variable maps to the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

TempVar

A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1) or Equation (79–2), where *X* is the decimal value of TempVar.

Values: 1 through 999

When a PD mode is not active, the value shall be set to zero.

local_system_change

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.

Values:

FALSE: The local system does not wants to change the power allocation.

TRUE: The local system wants to change the power allocation.

parameter_type

A Type 1 and 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification. Type 3 and 4 PSE state diagrams do not use this variable.

Values:

1: Type 1 PSE parameter values (default).

2: Type 2 PSE parameter values.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–32) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values:

FALSE: PD Data Link Layer classification is not enabled.

TRUE: PD Data Link Layer classification is enabled.

pd_dll_power_type

A Type 1 and Type 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification. Type 3 and Type 4 PSE state diagrams do not use this variable.

Values:

1: PD is a Type 1 PD (default).

2: PD is a Type 2 PD.

pd_dll_ready

An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–13) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values:

FALSE: PSE Data Link Layer classification is not enabled.

TRUE: PSE Data Link Layer classification is enabled.

pse_dll_power_type

A control variable output by the PD power control state diagram, defined in Figure 33–49, that indicates the PSE Type as 1 or 2, see 79.3.2.4.1.

Values:

1: The PSE is a Type 1 PSE, for a Type-1 PSE.

2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSEs

pse_dll_ready

An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

pse_power_type

A control variable that indicates to the PD the type of PSE by which it is being powered.

Values:

1: The PSE is a Type 1 PSE.

2: The PSE is a Type 2, Type 3, or Type 4 PSE.

pd_dll_single_or_dual

A control variable output by PD power control state diagram, defined in Figure 33-49, that indicates if the PD is single-signature PD or dual-signature PD. Type 3 and Type 4 PD state diagrams do not use this variable.

Values:

single: A single-signature PD configuration is connected to the PI.

dual: A dual-signature PD configuration is connected to the PI.

pse_dll_single_or_dual

A control variable output by PSE power control state diagram defined in Figure 33-48 (generated from the do_cxn_check function of the Type 3 and Type 4 PSE state diagram in Figure 33-15) which indicates if the PSE is connected to a single-signature PD or dual-signature PD.

Values:

invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been found. This includes an open circuit condition.

single: A single-signature PD configuration is connected to the PI.

dual: A dual-signature PD configuration is connected to the PI.

### ~~33.5.3.4~~ 33.5.3.1.3 Functions

pse_power_review

This function evaluates the PSE power allocation or **power** budget of the PSE based on local system changes. The function returns the following variables:

PSE_NEW_VALUE:

The new maximum total power value that the PSE expects the PD to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE_NEW_VALUE.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:

PD_NEW_VALUE:

The new maximum power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PD_NEW_VALUE.

## 4. Add pd_dll_single_or_dual and pse_dll_single_or_dual to Table 33-41.

**Table 33–41—Attribute to state diagram variable cross-reference**

| Entity | Attribute | Mapping | State diagram variable |
|---|---|---|---|
| oLldpXdot3LocSystemsGroup Object Class | | | |
| PSE | aLldpXdot3LocPDRequestedPowerValue | ⇐ | PDRequestedPowerValueEcho |
| | aLldpXdot3LocPSEAllocatedPowerValue | ⇐ | PSEAllocatedPowerValue |
| | aLldpXdot3LocReady | ⇐ | pse_dll_ready |
| PD | aLldpXdot3LocPDRequestedPowerValue | ⇐ | PDRequestedPowerValue |
| | aLldpXdot3LocPSEAllocatedPowerValue | ⇐ | PSEAllocatedPowerValueEcho |
| | aLldpXdot3LocReady | ⇐ | pd_dll_ready |
| oLldpXdot3RemSystemsGroup Object Class | | | |
| PSE | aLldpXdot3RemPDRequestedPowerValue | ⇒ | MirroredPDRequestedPowerValue |
| | aLldpXdot3RemPSEAllocatedPowerValue | ⇒ | MirroredPSEAllocatedPowerValueEcho |
| | aLldpXdot3RemPowerType Value[1]<br>11<br>01 | <br>⇒<br>⇒ | pd_dll_power_type Value[1]<br>01<br>10 |
| PD | aLldpXdot3RemPSEAllocatedPowerValue | ⇒ | MirroredPSEAllocatedPowerValue |
| | aLldpXdot3RemPDRequestedPowerValue | ⇒ | MirroredPDRequestedPowerValueEcho |
| | aLldpXdot3RemPowerType Value[1]<br>10<br>00 | <br>⇒<br>⇒ | pse_dll_power_type Value[1]<br>01<br>10 |

[1]Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

## 5. Update the following PSE state diagram Figure 33-48

### 33.5.3.1.4 ~~33.5.3.5~~ State diagrams

The general state change procedure for PSEs is shown in Figure 33–48.

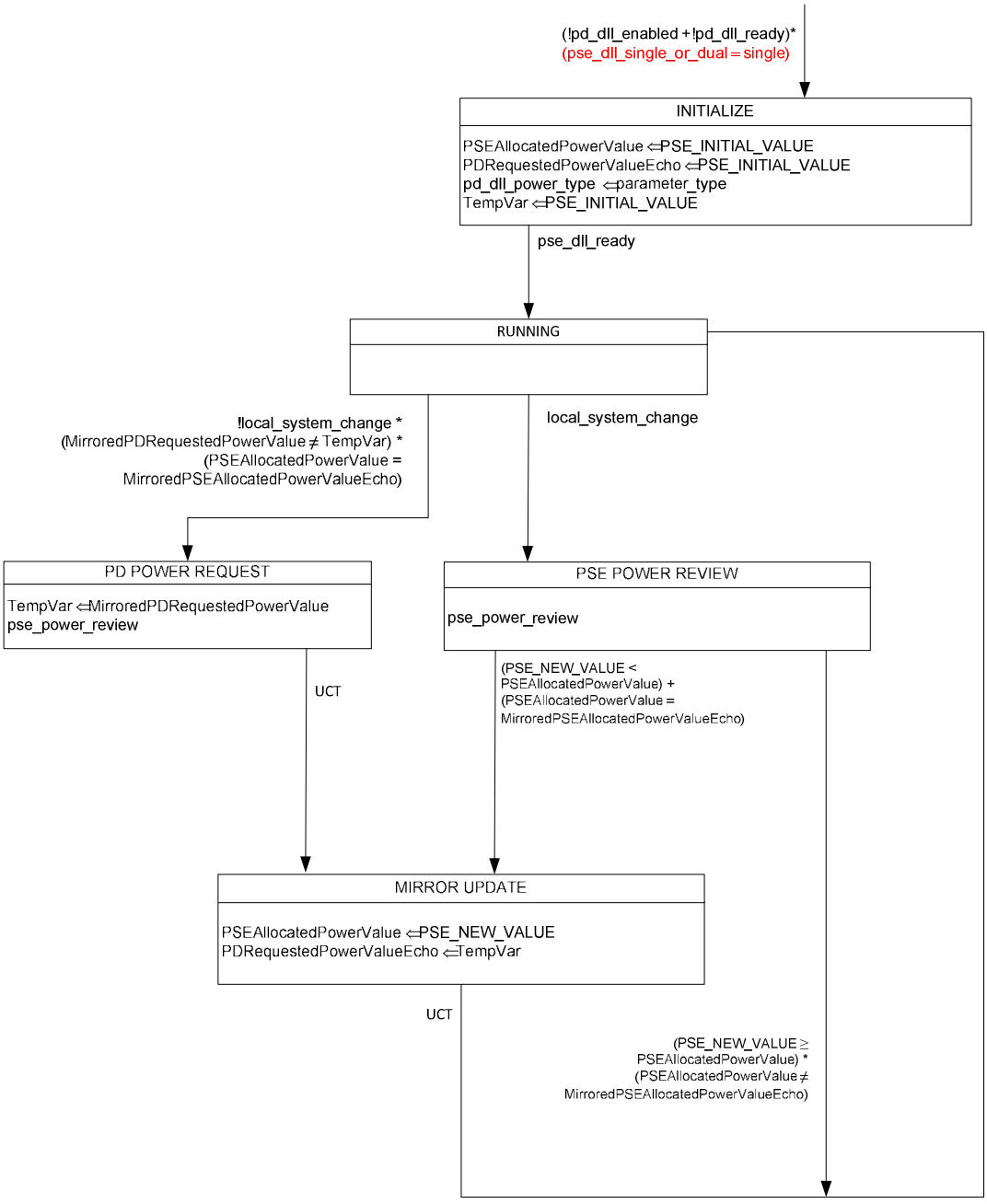


**Figure 33–48—PSE power control state diagram**

## 6. Update the following PSE state diagram Figure 33-49

The general state change procedure for PDs is shown in Figure 33–49.

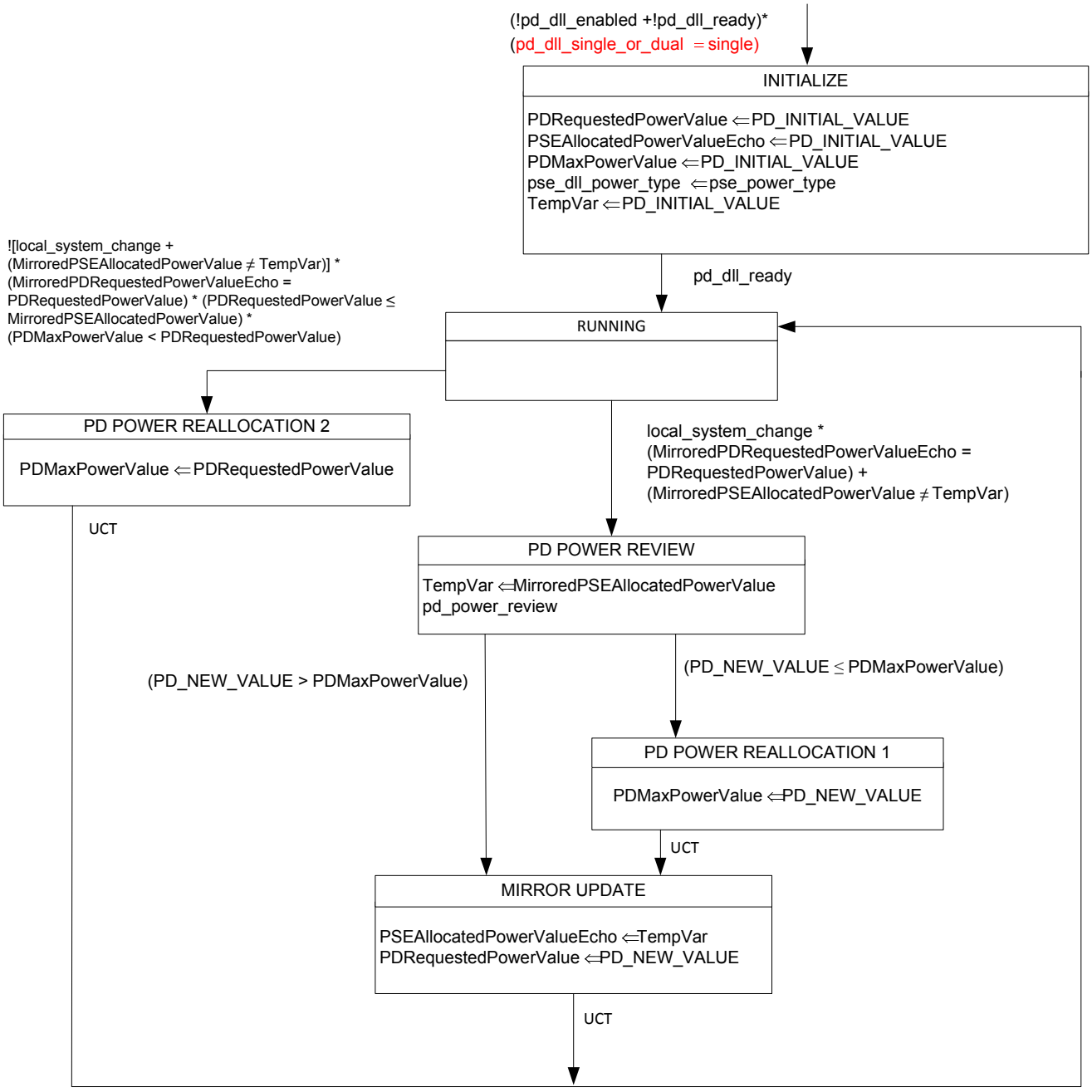


**Figure 33–49—PD power control state diagram**

## 7. Update the following text

### 33.5.3.1.5 ~~33.5.4~~ State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams describe the behavior above.

#### 33.5.3.1.5.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is allowed to change its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, PSE_NEW_VALUE, is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE is smaller than PSEAllocatedPowerValue, it enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

If the PSE's previously stored MirroredPDRequestedPowerValue changes, a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

#### ~~33.5.4.2~~ 33.5.3.1.5.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD's previously stored MirroredPSEAllocatedPowerValue is changed or local_system_change is asserted by the PD so as to change its power allocation, the PD enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE. If PD_NEW_VALUE is less than PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD POWERREALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to the RUNNING state.

## ~~33.5.5~~ 33.5.3.1.6 Autoclass

| This is not part of the baseline |
| --- |
| This sub clause was not addressed in this document. |

### 33.5.3.1.7 Dual-signature system constants

Variables PD_DLLMAX_VALUE_(M), PD_INITIAL_VALUE_(M), and PSE_INITIAL_VALUE_(M), are quantized to fit the available resolution. Additional information on power levels for Classes 6 and 8 may be found in 33.3.8.2.1.

PD_DLLMAX_VALUE_(M)
This value is derived from pd_max_power_(M) variable (33.3.3.12) described as follows:

| pd_max_power_(M) | PD_DLLMAX_VALUE |
| --- | --- |
| 1 | 39 |
| 2 | 65 |
| 3 | 130 |
| 4 | 255 |
| 5 | 355 |

PD_INITIAL_VALUE_(M)
This value is derived as follows from the pd_max_power_(M) variable (33.3.3.12) used in the PD state diagram (Figure 33–33):

| pd_max_power_(M) | PD_INITIAL_VALUE |
| --- | --- |
| 1 | ≤39 |
| 2 | ≤ 65 |
| 3 | ≤ 130 |
| 4 | ≤255 |
| 5 | ≤355 |

PSE_INITIAL_VALUE_(M)
This value is derived as follows from pd_allocated_power_pri or pd_allocated_power_sec, as defined in 33.2.5.11, which is used in the Type 3 and Type 4 PSE state diagrams in 33.2.5.12:

| parameter_type | PSE_INITIAL_VALUE_(M) |
| --- | --- |
| 3 | 39 |
| 3 | 65 |
| 3 | 130 |
| 3 | 255 |
| 4 | 355 |

single_or_dual
This value is generate by a Type 3 PD that indicates if the PD is single-signature PD or dual-signature-PD.
Values:
single: A single-signature PD configuration is connected to the PI.
dual: A dual-signature PD configuration is connected to the PI.

### 33.5.3.1.8 Dual-signature system Variables

Figure 33-49a uses PD load information in Table 79-5b **bit #1**, to ensure execution of PSE new power allocation correctly per pairset. This variable is not used in single-signature PD.
When the PD power demand on Mode A and Mode B are not electrically isolated. New assigned power value for Mode A and mode B is identical.

When the PD power demand on Mode A and Mode B are electrically isolated. New assigned power for Mode A and mode B is assigned independently with optional different values from each other.

The PD or PSE control state diagrams (Figure 33-48a and Figure 33-49b) use the PD mode selection bit 0 in Table 79-5b to manage the requested PD power over mode(M) and the allocated power over Alternative(M).
This bit is used only when dual-signature PD is connected to the PSE.

The PSE power control state diagram (Figure 33–48a) and PD power control state diagram (Figure 33–49a) use the following variables:

MirroredPDRequestedPowerValue_(M)
The copy of the PD Requested Power Value field for mode(M) in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute_(M) (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of MirroredPDRequestedPowerValue.
Values: 0 through 499.
When a PD mode is not active, the value is set to zero.

MirroredPDRequestedPowerValueEcho_(M)
The copy of the PD Requested Power Value filed for mode(M) in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue_(M) attribute (30.12.3.1.17).
Values: 0 through 499.
When a PD mode is not active, the value is set to zero.

MirroredPSEAllocatedPowerValue_(M)
The copy of the PSE Allocated Power Value field for mode(M)in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute_(M) (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of MirroredPSEAllocatedPowerValue_(M).
Values: 0 through 499.
When a PD mode is not active, the value is set to zero.

MirroredPSEAllocatedPowerValueEcho_(M)
The copy of the PSE Allocated Power Value for mode(M) field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue_(M) attribute (30.12.3.1.18).

PDRequestedPowerValueEcho_(M)
This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue_(M) attribute (30.12.2.1.17).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.

PDMaxPowerValue_(M)
Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.8.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PDMaxPowerValue_(M).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.
PDRequestedPowerValue_(M)

Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.8.2) the PD requests. This power value is encoded according to Equation (79–1), where *X* is the decimal value of PDRequestedPowerValue_(M). This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue_(M) attribute (30.12.2.1.17).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValue_(M)

Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.8.2) the PD ever draws. This power value is encoded according to Equation (79–2), where *X* is the decimal value of PSEAllocatedPowerValue_(M). This variable maps to the aLldpXdot3LocPSEAllocatedPowerValue_(M) attribute (30.12.2.1.18).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValueEcho_(M)

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue_(M) attribute (30.12.2.1.18).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.

TempVar_(M)

A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1) or Equation (79–2), where *X* is the decimal value of TempVar_(M).
Values: 0 through 499.
When a PD mode is not active, the value shall be set to zero.

local_system_change_(M)

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.
Values:
FALSE: The local system does not wants to change the power allocation.
TRUE: The local system wants to change the power allocation.

parameter_type

A Type 1 and 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification. Type 3 and 4 PSE state diagrams do not use this variable.
Values:
1: Type 1 PSE parameter values (default).
2: Type 2 PSE parameter values.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–32) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values:

FALSE: PD Data Link Layer classification is not enabled.

TRUE: PD Data Link Layer classification is enabled.

pd_dll_power_type

A Type 1 and Type 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification. Type 3 and Type 4 PSE state diagrams do not use this variable.

Values:

1: PD is a Type 1 PD (default).

2: PD is a Type 2 PD.

pd_dll_ready

An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–13) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values:

FALSE: PSE Data Link Layer classification is not enabled.

TRUE: PSE Data Link Layer classification is enabled.

pse_dll_power_type

A control variable output by the PD power control state diagram, defined in Figure 33–49, that indicates the PSE Type as 1 or 2, see 79.3.2.4.1.

Values:

1: The PSE is a Type 1 PSE, for a Type-1 PSE.

2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSEs

pse_dll_ready

An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values:

FALSE: Data Link Layer classification has not completed initialization.

TRUE: Data Link Layer classification has completed initialization.

pse_power_type

A control variable that indicates to the PD the type of PSE by which it is being powered.

Values:

1: The PSE is a Type 1 PSE.

2: The PSE is a Type 2, Type 3, or Type 4 PSE.

pd_dll_single_or_dual

A control variable output by PD power control state diagram, defined in Figure 33-49, that indicates if the PD is single-signature PD or dual-signature PD. Type 3 and Type 4 PD state diagrams do not use this variable.

Values:

single: A single-signature PD configuration is connected to the PI.

dual: A dual-signature PD configuration is connected to the PI.

pse_dll_single_or_dual

A control variable output by PSE power control state diagram defined in Figure 33-48 (generated from the do_cxn_check function of the Type 3 and Type 4 PSE state diagram in Figure 33-15) which indicates if the PSE is connected to a single-signature PD or dual-signature PD.

Values:

invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been found. This includes an open circuit condition.

single: A single-signature PD configuration is connected to the PI.

dual: A dual-signature PD configuration is connected to the PI.

#### 33.5.3.1.9 Functions

pse_power_review_(M)

This function evaluates the PSE power allocation or **power** budget of the PSE over Alternative(M) based on local system changes. See PD Load bit in 79.3.2.6b.3. The function returns the following variables:

PSE_NEW_VALUE:

The new maximum power value that the PSE expects the PD to draw over Alternative(M). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE_NEW_VALUE_(M).

pd_power_review_(M)

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. See PD Load bit in 79.3.2.6b.3. The function returns the following variables:

PD_NEW_VALUE_ mode(M):

The new maximum power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PD_NEW_VALUE_(M).

## 8. Copy Table 33-41 from the single-signature section and make the following changes:

1. Change the Table number from 33-41 to 33-41a. The text of the title remains the same.
2. Add suffix _(M) to all variables.
3. Add the new added variables to the table.

## 9. Update the following PSE state diagram Figure 33-48a

### 9.1 *Editor to replace all terms with the suffix "_mode(M)" with the suffix "_(M)" in Figure 33-48a and Figure 33-49a.*

***(The reason is that some of the variables belong to PSE state machine and some to the PD state machine and the term "mode" is reserved for the PD.)***

#### 33.5.3.1.10 State diagrams

The general state change procedure for PSEs is shown in Figure 33–48a.

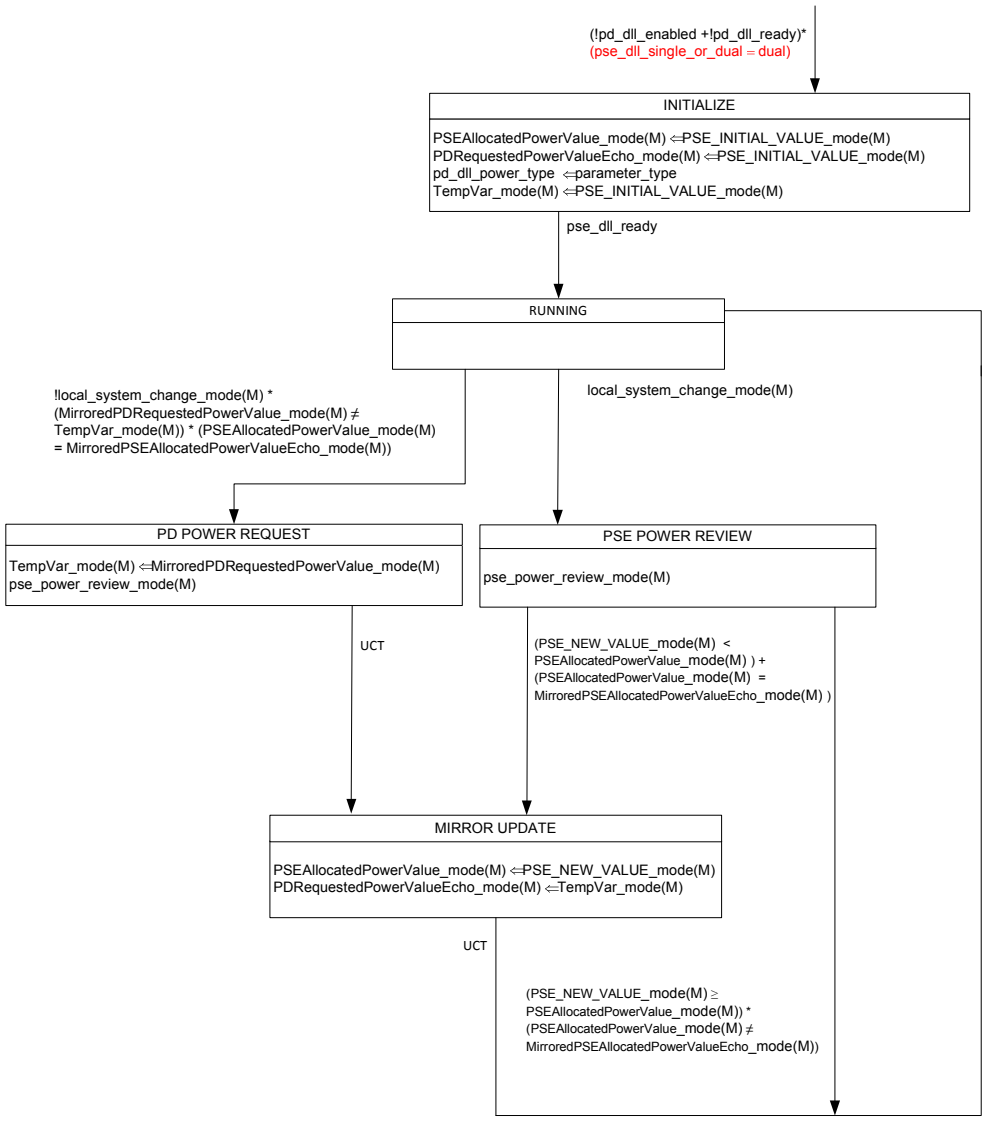


**Figure 33–48A—PSE power control state diagram when connected to dual-signature PD**

## 10. Update the following PSE state diagram Figure 33-49a

## 10.1 *Editor to replace all terms with the suffix "_mode(M)" with the suffix "_(M)" in Figure 33-48a and Figure 33-49a. (The reason is that some of the variables belong to PSE state machine and some to the PD state machine and the term "mode" is reserved for the PD.)*

The general state change procedure for PDs is shown in Figure 33–49A.

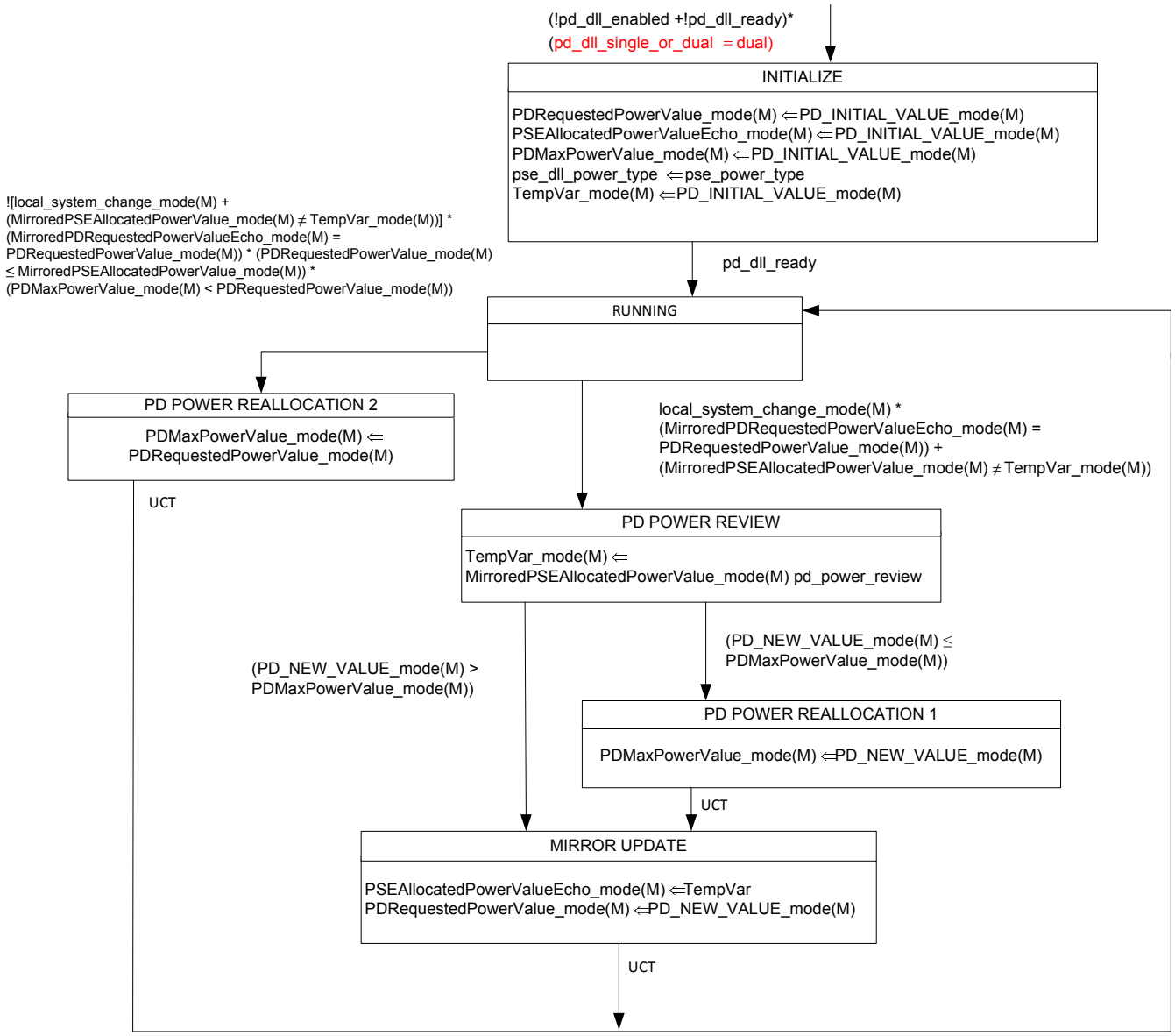


**Figure 33–49A—Dual-signature PD power control state diagram**

# 11. Add the following text:

### 33.5.3.2 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue_(M) (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup_(M) object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue_(M) (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup_(M) object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue_(M) (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup_(M) object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue _(M) (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup_(M) object class to the aLldpXdot3LocPDRequestedPowerValue_(M) (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class_(M). This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue_(M) (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup_(M) object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue_(M) (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup_(M) object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue_(M) (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup_(M) object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue_(M) (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup_(M) object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue_(M) (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup_(M) object class to the aLldpXdot3LocPSEAllocatedPowerValue_(M) (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup_(M) object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue_(M) (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup_(M) object class.

The state diagrams describe the behavior above.

#### 33.5.3.2.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue_(M) matches the value of MirroredPSEAllocatedPowerValueEcho_(M). When the PSE is not in sync with the PD, the PSE is allowed to change its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change_(M) is asserted and the PSE enters the PSE POWER REVIEW_(M) state, where a new power allocation value, PSE_NEW_VALUE_(M), is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE_(M) is smaller than PSEAllocatedPowerValue_(M), it enters the MIRROR UPDATE_(M) state where PSE_NEW_VALUE_(M) is assigned to PSEAllocatedPowerValue_(M). It also updates PDRequestedPowerValueEcho_(M) and returns to the RUNNING state.

If the PSE's previously stored MirroredPDRequestedPowerValue changes_(M), a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE_(M), is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE_(M) is assigned to PSEAllocatedPowerValue_(M). It also updates PDRequestedPowerValueEcho_(M) and returns to the RUNNING state.

#### 33.5.3.2.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue_(M) matches the value of MirroredPDRequestedPowerValueEcho_(M). The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD's previously stored MirroredPSEAllocatedPowerValue_(M) is changed or local_system_change_(M) is asserted by the PD so as to change its power allocation, the PD enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE_(M). If PD_NEW_VALUE_(M) is less than PDMaxPowerValue_(M), it updates PDMaxPowerValue_(M) in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE_(M) is assigned to PDRequestedPowerValue_(M). It also updates PSEAllocatedPowerValueEcho_(M) and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE_(M) is greater than PDMaxPowerValue_(M), the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD POWERREALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue_(M) to PDRequestedPowerValue_(M) and returns to the RUNNING state.

## 12. Make the following changes to clause 79:

### 79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

**This is not part of the baseline**

-The power typex bits were updated to differentiate between single and dual signature PD.
-PD mode selection was updated to allow using the same bit for both PSE and PD depending who is the source of the LLDPPDU.

**Table 79–5b—System setup value field**

| Bit | Function | Value/meaning |
|---|---|---|
| 7:4 | Power typex | 7 6 5 4<br>1 1 1 1= Type 4 dual-signature PD ~~Reserved/Ignore~~<br>1 1 1 0= Reserved/Ignore<br>1 1 0 1= Type 3 dual-signature ~~Reserved/Ignore~~<br>1 1 0 0= Reserved/Ignore<br>1 0 1 1= Reserved/Ignore<br>1 0 1 0= Reserved/Ignore<br>1 0 0 1= Type 4 single-signature PD<br>1 0 0 0= Type 4 PSE<br>0 1 1 1= Type 3 single-signature PD<br>0 1 1 0= Type 3 PSE<br>0 1 0 1= Type 2 PD<br>0 1 0 0= Type 2 PSE<br>0 0 1 1= Type 1 PD<br>0 0 1 0= Type 1 PSE<br>0 0 0 1= Reserved/Ignore<br>0 0 0 0= Reserved/Ignore |
| 3 | PD 4PID | 1= PD supports powering of both modes<br>0= PD does not support powering of both modes |
| 2 | Reserved | Transmit as zero. Ignore on receive. |
| 1 | PD Load | 1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated.<br>0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated. |
| 0 | PD Mode selection | 1 = PD requested power applies to Mode A pairset<br>0 = PD requested power applies to Mode B pairset |

#### 79.3.2.6b.5 PD Mode selection

This field shall be set according to Table 79–5b to select the Mode for which the PD is requesting power when the **power typex** (bits 7:4) is PD and a dual-signature PD (see 1.4.186a and 33.3.2) is the source of the LLDPPDU.

## 13. Make the following changes to clause 79, page 218 line 39:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PD requested power value | PSE allocated power value | PD requested power value mode A | PD requested power value mode B | PSE allocated power value ALT A | PSE allocated power value ALT B | PSE power status | System setup | PSE maximum available power | Autoclass | Power down |

**End Of Proposed Baseline**

# Annex A: To be considered by the group:

The current TLV format in D2.1 is:

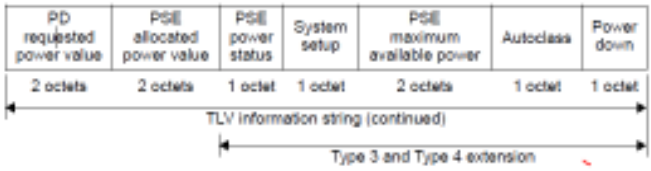


**Figure 79–3—Power Via MDI TLV format**

In this concept (Option 2) the TLV structure need to be:

Advantages: In a single transaction we know if we want to work on ModeA or ModeB even if there is no local_system_change request. If we depend only on pd_mode_selection bits then even if we don't have local_system_change request, we will need to transmit all the information again any time pd_mode_selection bits flips between "0" and "1".

| PD requested power value | PSE allocated power value | PD requested power value mode A | PD requested power value mode B | PSE allocated power value ALT A | PSE allocated power value ALT B | PSE power status | System setup | PSE maximum available power | Autoclass | Power down |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |

Or It can be:

| PD requested power value **or** PD requested power value mode A | PSE allocated power value **or** PSE allocated power value ALT A | PD requested power value mode B | PSE allocated power value ALT B | PSE power status | System setup | PSE maximum available power | Autoclass | Power down |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |

To discuss which is preferred.