

1 **Comment #39 D2.1**

2 **(TDL for comments #214 , #248, #304, #239 and #195 from D2.0)**

3  
4 **From TDL List for comment #214 response and remedy + new issues:**

- 5 1. To update DLL SM for single and dual PDs and PSEs with the following objectives:
- 6 -Power Demotion
- 7 -Addressing cases when power is not sufficient for one of the modes or both modes.
- 8 2. To fix some error regarding the sync between variable names in PD state machine and its variable list, clause
- 9 33.5 PD/PSE DLL power state machine (Figures 33-48 and 33-49) and its variable list.
- 10 3. To figure out how DLL state machine uses variables from Physical Layer class (this is about the response for
- 11 commnet #248 from D2.0 regarding the question How DLL will know if PD is single–signature PD or dual-sig PD?
- 12 (The problem is that the PSE know it from the physical layer. The PD can’t know unless the PD is using existing PD variable
- 13 that tells the PD DLL if it is single or dual signature PD.)
- 14 2. Editing constant and variables per Type 1,2 and Type 3 and 4 in separate clauses where applicable.

15  
16 **Concept (Option 2)**

17 (Option 1 is shown in separate document)

- 18
- 19 1. Keep 33.5 for Type 1-4 system.
- 20 2. Duplicate 33.5.2, 33.5.3 with similar content with the additional suffix “\_(M)” whenever relevant.
- 21 3. Duplicate PSE and PD DLL state machine and add the suffix “-mode(M)” to all variables and constants.
- 22 4. Duplicate Table 33-41
- 23 5. Duplicate all other related DLL and TLV tables.
- 24 6. Add additional TLV fields in the TLV structure (page 218) for:
- 25 -PDRrequestedPowerValue\_ModeA
- 26 -PDRrequestedPowerValue\_ModeB
- 27 -PSEAllocatedPowerValue\_ModeA
- 28 -PSEAllocatedPowerValue\_ModeB
- 29

30 **Proposed Remedy:**

31 Adopt darshan\_11\_1116\_option2.pdf if ready for the meeting. If not, keep it in the TDL.

32  
33 **Proposed Baseline starts here**

34  
35 Adding missing tables for dual-signature PDs.

36  
37 **1. Add the following table after Table 33-15 on clause 33.2.7, page 108 line 35**

38 **Table 33–15a—Relation of assigned Class and DLL for dual-signature PDs**

PSEAllocatedPowerValue_(M)	Assigned Class
1 – 39	1
40 – 65	2
66 – 130	3
131 – 255	4
256 – 400	5

39  
40 **2. Add the following table after Table 33-25 on clause 33.3.6.1, 150 page 150 line 20**

41 **Table 33–25a—Relation of assigned Class and DLL for dual-signature PDs**

PDMaxPowerValue_(M)	Assigned Class
1 – 39	1
40 – 65	2
66 – 130	3
131 – 255	4
256 – 400	5

43 **3. Make the following changes to 33.5**

44 **33.5 Data Link Layer classification**

45 Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE  
46 802.3 Organizationally Specific TLVs defined in Clause 79. Single-signature PDs advertising a Class 4 signature or higher and  
47 Type 3 and Type 4 dual-signature PDs support Data Link Layer classification (see 33.3.6). Data Link Layer classification is  
48 optional for all other devices.

49 All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI  
50 TLVs shall be ignored.

51 **33.5.1 TLV frame definition**

52 Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009;  
53 shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and may support the Power via MDI  
54 Measurements TLV defined in 79.3.8; and shall support the control state diagrams defined in 33.5.3.

55  
56 **33.5.2 Data Link Layer classification timing requirements**

57  
58 Type 2, 3, and 4 PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data  
59 Link Layer classification being enabled in the PSE as indicated by the variable pse\_dll\_enabled (33.2.5.4,  
60 33.5.3.3).

61  
62 A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power  
63 via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable  
64 pse\_dll\_ready (33.5.3.3).

65  
66 Type 1 PDs that implement Data Link Layer classification and Type 2, 3, and 4 PDs shall set the state  
67 variable pd\_dll\_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated  
68 by the variable pd\_dll\_enabled (33.3.3.7, 33.5.3.3).

69  
70 Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PSE  
71 allocated power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power  
72 via MDI TLV where the “PD requested power value” field is different from the previously communicated  
73 value.

74  
75 Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PD  
76 requested power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power  
77 via MDI TLV where the “PSE allocated power value” field is different from the previously communicated  
78 value.

79  
80 **33.5.3 Power control state diagrams**

81 The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and  
82 PD Data Link Layer classification respectively.

83 When single-signature PDs are supported, PSE Data Link Layer classification shall provide the  
84 behavior of the state diagram as shown in Figure 33–48. PD Data Link Layer classification shall provide the  
85 behavior of the state diagram as shown in Figure 33–49.

86  
87 When dual-signature PDs are supported, PSE Data Link Layer classification shall provide the  
88 behavior of the state diagram as shown in Figure 33–48a. PD Data Link Layer classification shall provide the  
89 behavior of the state diagram as shown in Figure 33–49a. See 33.3.5.3.1.7.

90  
91 **33.5.3.1 Conventions**

92 The body of this subclause is comprised of state diagrams, including the associated definitions of variables,  
93 constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the  
94 state diagram prevails.

95  
96 The notation used in the state diagrams follows the conventions of state diagrams as described in 33.2.5.2.  
97

98 **33.5.3.1.1 Single-signature system Constants**

99

100 Variables PD\_DLLMAX\_VALUE, PD\_INITIAL\_VALUE, and PSE\_INITIAL\_VALUE, are quantized to fit the available resolution.  
101 Additional information on power levels for Classes 6 and 8 may be found in 33.3.8.2.1.

102

103 ~~33.5.3.2.1~~ **33.5.3.1.1.1. Type 1 and Type 2 PSE constants**

104

105 PSE\_INITIAL\_VALUE

106 This value is derived as follows from parameter\_type and the mr\_pd\_class\_detected (33.2.5.6) variable used in the Type 1 and  
107 Type 2 PSE state diagram defined in Figure 33–13:

parameter_type	PSE_INITIAL_VALUE
1	130
1	39
1	65
1	130
1	130
2	255

115

116 ~~33.5.3.2.2~~ **33.5.3.1.1.2 Single-signature system Type 3 and Type 4 PSE constants**

117

118 PD\_DLLMAX\_VALUE

119 This value is derived from pd\_max\_power variable (33.3.3.7) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255
5	400
6	600
7	620
8	999

130

131

132 PD\_INITIAL\_VALUE  
133 This value is derived as follows from the pd\_max\_power (33.3.3.7) variable used in the PD state  
134 Diagram; defined in Figure 33–31 and Figure 33-32:

pd_max_power	PD_INITIAL_VALUE
0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255
5	≤ 400
6	≤ 600
7	≤ 620
8	≤ 900

144  
145  
146  
147 PSE\_INITIAL\_VALUE  
148 This value is derived as follows from pd\_allocated\_power, as defined in 33.2.5.11, which is used in the Type 3 and Type 4 PSE  
149 state diagrams in 33.2.5.12:

pd_allocated_power	PSE_INITIAL_VALUE
1	130
1	39
1	65
1	130
1	130
2	255
3	400
3	600
4	620
4	900

### 163 ~~33.5.3.3~~ [33.5.3.1.2 Single-signature system](#) Variables

164  
165 The PSE power control state diagram (Figure 33–49) and PD power control state diagram (Figure 33–50) use the following  
166 variables:

167  
168 MirroredPDRequestedPowerValue  
169 The copy of the PD Requested Power Value field in the Power Via MDI TLV that the PSE receives from the remote system. This  
170 variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are  
171 represented using an integer value that is encoded according to Equation (79–1), where  $X$  is the decimal value of  
172 MirroredPDRequestedPowerValue.

173 Values: 1 through 999  
174 When a PD mode is not active, the value shall be set to zero.

175  
176 MirroredPDRequestedPowerValueEcho  
177 The copy of the PD Requested Power Value field in the Power Via MDI TLV that the PD receives from the remote system. This  
178 variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).

179 Values: 1 through 999  
180 When a PD mode is not active, the value shall be set to zero.

181  
182 MirroredPSEAllocatedPowerValue  
183 The copy of the PSE Allocated Power Value field in the Power Via MDI TLV that the PD receives from the remote system. This  
184 variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are  
185 represented using an integer value that is encoded according to Equation (79–2), where  $X$  is the decimal value of  
186 MirroredPSEAllocatedPowerValue.

187 Values: 1 through 999  
188 When a PD mode is not active, the value shall be set to zero.

189

190 MirroredPSEAllocatedPowerValueEcho  
191       The copy of the PSE Allocated Power Value field in the Power Via MDI TLV that the PSE receives from the remote  
192       system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).  
193

194 PDRequestedPowerValueEcho  
195       This variable is updated by the PSE state diagram. This variable maps into the  
196       aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).  
197       Values: 1 through 999  
198       When a PD mode is not active, the value shall be set to zero.  
199

200 PDMaxPowerValue  
201       Integer that indicates the actual PD power value of the local system. The actual PD power value for  
202       a PD is the maximum input average power (see 33.3.8.2) the PD ever draws under the current  
203       power allocation. Actual power numbers are represented using an integer value that is encoded  
204       according to Equation (79–1), where  $X$  is the decimal value of PDMaxPowerValue.  
205       Values: 1 through 999  
206       When a PD mode is not active, the value shall be set to zero.  
207

208 PDRequestedPowerValue  
209       Integer that indicates the PD requested power value in the PD. The value is the maximum input  
210       average power (see 33.3.8.2) the PD requests. This power value is encoded according to Equation  
211       (79–1), where  $X$  is the decimal value of PDRequestedPowerValue. This variable is mapped from  
212       the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).  
213       Values: 1 through 999  
214       When a PD mode is not active, the value shall be set to zero.  
215

216 PSEAllocatedPowerValue  
217       Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see  
218       33.3.8.2) the PD ever draws. This power value is encoded according to Equation (79–2), where  $X$  is the decimal value  
219       of PSEAllocatedPowerValue. This variable maps to the aLldpXdot3LocPSEAllocatedPowerValue attribute  
220       (30.12.2.1.18).  
221       Values: 1 through 999  
222       When a PD mode is not active, the value shall be set to zero.  
223

224 PSEAllocatedPowerValueEcho  
225       This variable is updated by the PD state diagram. This variable maps into the  
226       aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).  
227       Values: 1 through 999  
228       When a PD mode is not active, the value shall be set to zero.  
229

230 TempVar  
231       A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded  
232       according to Equation (79–1) or Equation (79–2), where  $X$  is the decimal value of TempVar.  
233       Values: 1 through 999  
234       When a PD mode is not active, the value shall be set to zero.  
235

236 local\_system\_change  
237       An implementation-specific control variable that indicates that the local system wants to change  
238       the allocated power value. In a PSE, this indicates it is going to change the power allocated to the  
239       PD. In a PD, this indicates it is going to request a new power allocation from the PSE.  
240       Values:  
241       FALSE: The local system does not wants to change the power allocation.  
242       TRUE: The local system wants to change the power allocation.  
243  
244  
245  
246  
247

248 parameter\_type  
249 A Type 1 and 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised  
250 through Data Link Layer classification. Type 3 and 4 PSE state diagrams do not use this variable.  
251 Values:  
252 1: Type 1 PSE parameter values (default).  
253 2: Type 2 PSE parameter values.  
254

255 pd\_dll\_enabled  
256 A variable output by the PD state diagram (Figure 33–32) to indicate if the PD Data Link Layer  
257 classification mechanism is enabled.  
258 Values:  
259 FALSE: PD Data Link Layer classification is not enabled.  
260 TRUE: PD Data Link Layer classification is enabled.  
261

262 pd\_dll\_power\_type  
263 A Type 1 and Type 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as  
264 advertised through Data Link Layer classification. Type 3 and Type 4 PSE state diagrams do not use this variable.  
265 Values:  
266 1: PD is a Type 1 PD (default).  
267 2: PD is a Type 2 PD.  
268

269 pd\_dll\_ready  
270 An implementation-specific control variable that indicates that the PD has initialized Data Link  
271 Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).  
272 Values:  
273 FALSE: Data Link Layer classification has not completed initialization.  
274 TRUE: Data Link Layer classification has completed initialization.  
275

276 pse\_dll\_enabled  
277 A variable output by the PSE state diagram (Figure 33–13) to indicate if the PSE Data Link Layer  
278 classification mechanism is enabled.  
279 Values:  
280 FALSE: PSE Data Link Layer classification is not enabled.  
281 TRUE: PSE Data Link Layer classification is enabled.  
282

283 pse\_dll\_power\_type  
284 A control variable output by the PD power control state diagram, defined in Figure 33–49, that indicates the PSE Type as  
285 1 or 2, see 79.3.2.4.1.  
286 Values:  
287 1: The PSE is a Type 1 PSE, for a Type-1 PSE.  
288 2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSEs.  
289

290 pse\_dll\_ready  
291 An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification.  
292 This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).  
293 Values:  
294 FALSE: Data Link Layer classification has not completed initialization.  
295 TRUE: Data Link Layer classification has completed initialization.  
296

297 pse\_power\_type  
298 A control variable that indicates to the PD the type of PSE by which it is being powered.  
299 Values:  
300 1: The PSE is a Type 1 PSE.  
301 2: The PSE is a Type 2, Type 3, or Type 4 PSE.  
302  
303

304 pd\_dll\_single\_or\_dual  
 305 A control variable output by PD power control state diagram, defined in Figure 33-49, that indicates if the PD is single-signature PD or dual-  
 306 signature PD. Type 3 and Type 4 PD state diagrams do not use this variable.

307 Values:  
 308 single: A single-signature PD configuration is connected to the PI.  
 309 dual: A dual-signature PD configuration is connected to the PI.

311  
 312 pse\_dll\_single\_or\_dual  
 313 A control variable output by PSE power control state diagram defined in Figure 33-48 (generated from the do\_cxn\_check function of the Type  
 314 3 and Type 4 PSE state diagram in Figure 33-15) which indicates if the PSE is connected to a single-signature PD or dual-signature PD.

315 Values:  
 316 invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been  
 317 found. This includes an open circuit condition.  
 318 single: A single-signature PD configuration is connected to the PI.  
 319 dual: A dual-signature PD configuration is connected to the PI.

### 33.5.3.4 ~~33.5.3.4~~ 33.5.3.1.3 Functions

322 pse\_power\_review  
 323 This function evaluates the PSE power allocation or **power** budget of the PSE based on local system changes. The function  
 324 returns the following variables:

325 PSE\_NEW\_VALUE:  
 326 The new maximum **total** power value that the PSE expects the PD to draw. Actual power numbers are represented  
 327 using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE\_NEW\_VALUE.

328 pd\_power\_review  
 329 This function evaluates the power requirements of the PD based on local system changes and/or  
 330 changes in the PSE allocated power value. The function returns the following variables:

331 PD\_NEW\_VALUE:  
 332 The new maximum power value that the PD wants to draw. Actual power numbers are  
 333 represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of  
 334 PD\_NEW\_VALUE.

#### 336 4. Add pd\_dll\_single\_or\_dual and pse\_dll\_single\_or\_dual to Table 33-41.

Table 33–41—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRRequestedPowerValue	=	PDRRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	=	PSEAllocatedPowerValue
	aLldpXdot3LocReady	=	pse_dll_ready
PD	aLldpXdot3LocPDRRequestedPowerValue	=	PDRRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	=	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	=	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRRequestedPowerValue	=	MirroredPDRRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	=	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerTypeValue <sup>1</sup>	=	pd_dll_power_type Value <sup>1</sup>
PD	11	=	01
	01	=	10
	aLldpXdot3RemPowerTypeValue <sup>1</sup>	=	pse_dll_power_type Value <sup>1</sup>
PD	10	=	01
	00	=	10
		=	

<sup>1</sup> Other value combinations mapping from aLldpXdot3RemPowerType to pd\_dll\_power\_type or pse\_dll\_power\_type are not possible.

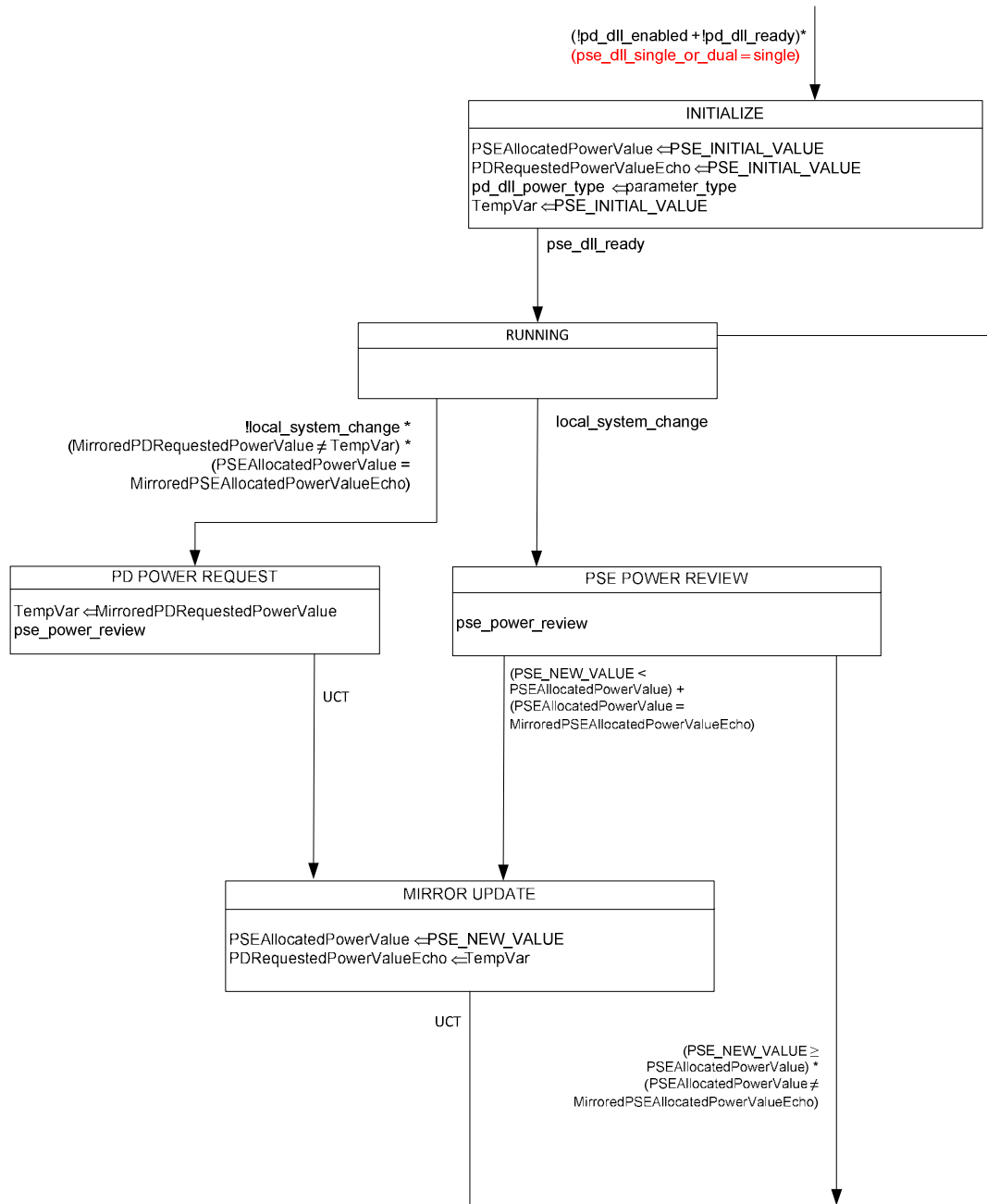
338

339  
 340  
 341  
 342  
 343

**5. Update the following PSE state diagram Figure 33-48**

**33.5.3.1.4 ~~33.5.3.5~~ State diagrams**

The general state change procedure for PSEs is shown in Figure 33-48.



**Figure 33-48—PSE power control state diagram**

344



345 **6. Update the following PSE state diagram Figure 33-49**

346 The general state change procedure for PDs is shown in Figure 33-49.

347

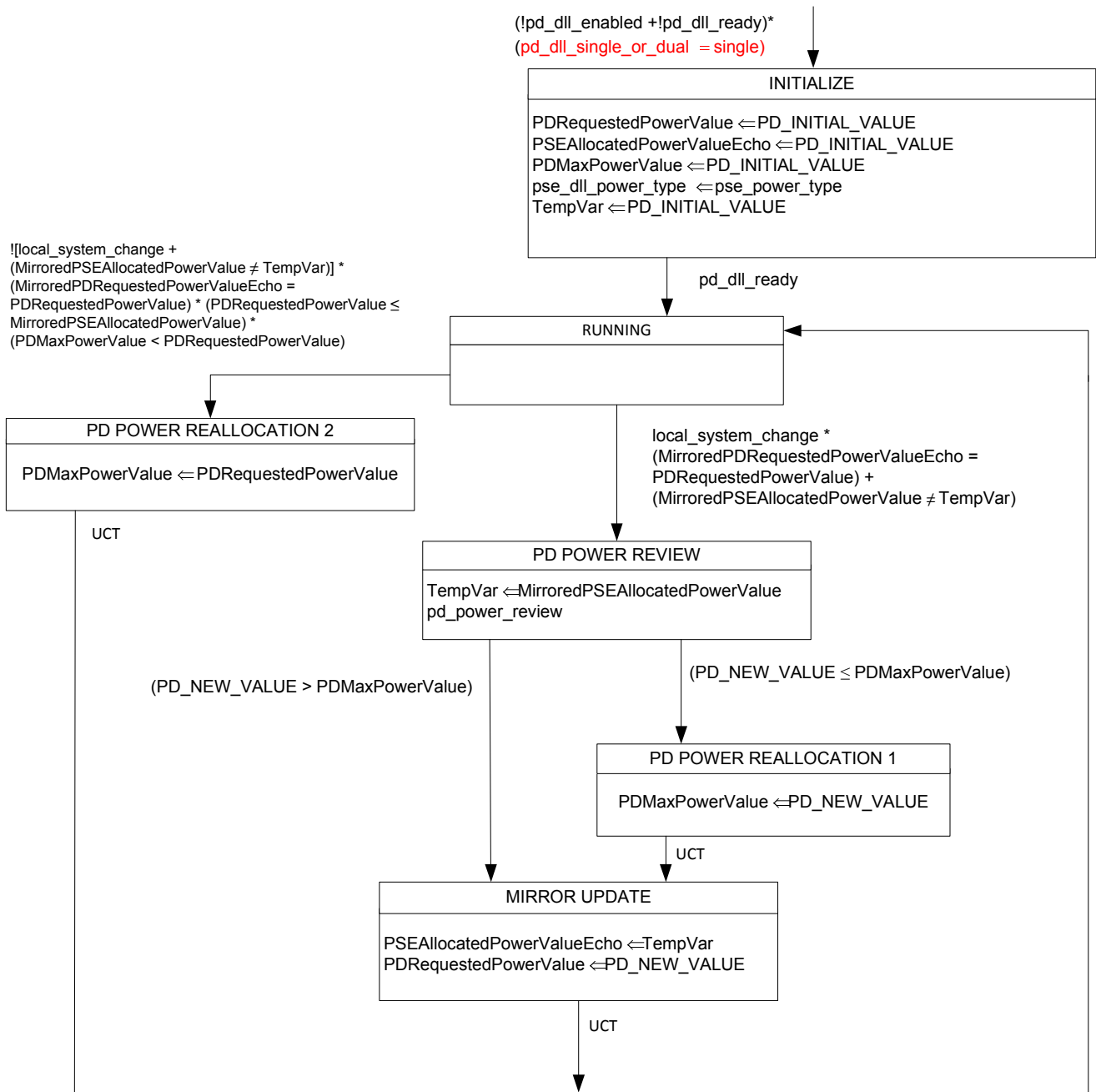


Figure 33-49—PD power control state diagram

348

349

350

## 351 **7. Update the following text**

### 352 **33.5.3.1.5 ~~33.5.4~~ State change procedure across a link**

353 The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

354

355 The PD may request a new power value through the aLldpXdot3LocPDRRequestedPowerValue  
356 (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as  
357 a change to the aLldpXdot3RemPDRRequestedPowerValue (30.12.3.1.17) attribute in the  
358 oLldpXdot3RemSystemsGroup object class.

359

360 The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the  
361 oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRRequestedPowerValue (30.12.3.1.17) in the  
362 oLldpXdot3RemSystemsGroup object class  
363 to the aLldpXdot3LocPDRRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a  
364 change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class.

365

366 The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue  
367 (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a  
368 change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the  
369 oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the  
370 aLldpXdot3LocPDRRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup  
371 object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18)  
372 attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue  
373 (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a  
374 change to the aLldpXdot3RemPDRRequestedPowerValue (30.12.3.1.17) attribute in the  
375 oLldpXdot3RemSystemsGroup object class.

376

377 The state diagrams describe the behavior above.

378

### 379 **33.5.3.1.5.1 PSE state change procedure across a link**

380 A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of  
381 MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is allowed to change its power allocation.

382

383 During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the  
384 local\_system\_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value,  
385 PSE\_NEW\_VALUE, is computed. If the PSE is in sync with the PD or if PSE\_NEW\_VALUE is smaller than PSEAllocatedPowerValue, it  
386 enters the MIRROR UPDATE state where PSE\_NEW\_VALUE is assigned to PSEAllocatedPowerValue. It also updates  
387 PDRRequestedPowerValueEcho and returns to the RUNNING state.

388

389 If the PSE's previously stored MirroredPDRRequestedPowerValue changes, a request by the PD to change its power allocation is recognized. It  
390 entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new  
391 power allocation value, PSE\_NEW\_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE\_NEW\_VALUE is assigned  
392 to PSEAllocatedPowerValue. It also updates PDRRequestedPowerValueEcho and returns to the RUNNING state.

393

### 394 **~~33.5.4.2~~ 33.5.3.1.5.2 PD state change procedure across a link**

395

396 A PD is considered to be in sync with the PSE when the value of PDRRequestedPowerValue matches the  
397 value of MirroredPDRRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw  
398 or the requested power value when it is not in sync with the PSE.

399

400 During normal operation, the PD is in the RUNNING state. If the PD's previously stored  
401 MirroredPSEAllocatedPowerValue is changed or local\_system\_change is asserted by the PD so as to change  
402 its power allocation, the PD enters the PD POWER REVIEW state. In this state, the PD evaluates the change  
403 and generates an updated power value called PD\_NEW\_VALUE. If PD\_NEW\_VALUE is less than  
404 PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD  
405 finally enters the MIRROR UPDATE state where PD\_NEW\_VALUE is assigned to  
406 PDRRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING  
407 state.

408

409 In the above flow, if PD\_NEW\_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync

410 with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD POWERREALLOCATION 2  
411 state. In this state, the PD assigns PDMaxPowerValue to

412 PDRRequestedPowerValue and returns to the RUNNING state.

413  
414  
415

**33.5.5-33.5.3.1.6 Autoclass**

This is not part of the baseline
This sub clause was not addressed in this document.

416  
417  
418  
419

**33.5.3.1.7 Dual-signature system constants**

420 Variables PD\_DLLMAX\_VALUE\_(M), PD\_INITIAL\_VALUE\_(M), and PSE\_INITIAL\_VALUE\_(M), are quantized to fit the available  
421 resolution. Additional information on power levels for Classes 6 and 8 may be found in 33.3.8.2.1.  
422

423 PD\_DLLMAX\_VALUE\_(M)  
424 This value is derived from pd\_max\_power\_(M) variable (33.3.3.12) described as follows:

pd_max_power_(M)	PD_DLLMAX_VALUE
425 1	39
426 2	65
427 3	130
428 4	255
429 5	355

431 PD\_INITIAL\_VALUE\_(M)  
432 This value is derived as follows from the pd\_max\_power\_(M) variable (33.3.3.12) used in the PD state diagram  
433 (Figure 33–33):  
434

pd_max_power_(M)	PD_INITIAL_VALUE
435 1	≤39
436 2	≤ 65
437 3	≤ 130
438 4	≤255
439 5	≤355

441 PSE\_INITIAL\_VALUE\_(M)  
442 This value is derived as follows from pd\_allocated\_power\_pri or pd\_allocated\_power\_sec, as defined in 33.2.5.11, which is used  
443 in the Type 3 and Type 4 PSE state diagrams in 33.2.5.12:  
444

parameter_type	PSE_INITIAL_VALUE_(M)
445 3	39
446 3	65
447 3	130
448 3	255
449 4	355

450 single\_or\_dual  
451 This value is generate by a Type 3 PD that indicates if the PD is single-signature PD or dual-signature-PD.  
452 Values:

- 453 single: A single-signature PD configuration is connected to the PI.
- 454 dual: A dual-signature PD configuration is connected to the PI.

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### 33.5.3.1.8 Dual-signature system Variables

Figure 33-49a uses PD load information in Table 79-5b **bit #1**, to ensure execution of PSE new power allocation correctly per pairset. This variable is not used in single-signature PD.

When the PD power demand on Mode A and Mode B are not electrically isolated. New assigned power value for Mode A and mode B is identical.

When the PD power demand on Mode A and Mode B are electrically isolated. New assigned power for Mode A and mode B is assigned independently with optional different values from each other.

The PD or PSE control state diagrams (Figure 33-48a and Figure 33-49b) use the PD mode selection bit 0 in Table 79-5b to manage the requested PD power over mode(M) and the allocated power over Alternative(M).

This bit is used only when dual-signature PD is connected to the PSE.

The PSE power control state diagram (Figure 33-48a) and PD power control state diagram (Figure 33-49a) use the following variables:

#### MirroredPDRequestedPowerValue\_(M)

The copy of the PD Requested Power Value field for mode(M) in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute\_(M) (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79-1), where  $X$  is the decimal value of MirroredPDRequestedPowerValue.

Values: 0 through 499.

When a PD mode is not active, the value is set to zero.

#### MirroredPDRequestedPowerValueEcho\_(M)

The copy of the PD Requested Power Value field for mode(M) in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue\_(M) attribute (30.12.3.1.17).

Values: 0 through 499.

When a PD mode is not active, the value is set to zero.

#### MirroredPSEAllocatedPowerValue\_(M)

The copy of the PSE Allocated Power Value field for mode(M) in the Power Via MDI TLV that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute\_(M) (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79-2), where  $X$  is the decimal value of MirroredPSEAllocatedPowerValue\_(M).

Values: 0 through 499.

When a PD mode is not active, the value is set to zero.

#### MirroredPSEAllocatedPowerValueEcho\_(M)

The copy of the PSE Allocated Power Value for mode(M) field in the Power Via MDI TLV that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue\_(M) attribute (30.12.3.1.18).

#### PDRequestedPowerValueEcho\_(M)

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue\_(M) attribute (30.12.2.1.17).

Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

#### PDMaxPowerValue\_(M)

Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.8.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79-1), where  $X$  is the decimal value of PDMaxPowerValue\_(M).

Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

#### PDRequestedPowerValue\_(M)

519 Integer that indicates the PD requested power value in the PD. The value is the maximum input  
520 average power (see 33.3.8.2) the PD requests. This power value is encoded according to Equation  
521 (79–1), where  $X$  is the decimal value of PDRequestedPowerValue\_(M). This variable is mapped from  
522 the aLldpXdot3LocPDRequestedPowerValue\_(M) attribute (30.12.2.1.17).  
523 Values: 0 through 499.  
524 When a PD mode is not active, the value shall be set to zero.  
525

526 PSEAllocatedPowerValue\_(M)  
527 Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see  
528 33.3.8.2) the PD ever draws. This power value is encoded according to Equation (79–2), where  $X$  is the decimal value  
529 of PSEAllocatedPowerValue\_(M). This variable maps to the aLldpXdot3LocPSEAllocatedPowerValue\_(M) attribute  
530 (30.12.2.1.18).  
531 Values: 0 through 499.  
532 When a PD mode is not active, the value shall be set to zero.  
533

534 PSEAllocatedPowerValueEcho\_(M)  
535 This variable is updated by the PD state diagram. This variable maps into the  
536 aLldpXdot3LocPSEAllocatedPowerValue\_(M) attribute (30.12.2.1.18).  
537 Values: 0 through 499.  
538 When a PD mode is not active, the value shall be set to zero.  
539

540 TempVar\_(M)  
541 A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded  
542 according to Equation (79–1) or Equation (79–2), where  $X$  is the decimal value of TempVar\_(M).  
543 Values: 0 through 499.  
544 When a PD mode is not active, the value shall be set to zero.  
545

546 local\_system\_change\_(M)  
547 An implementation-specific control variable that indicates that the local system wants to change  
548 the allocated power value. In a PSE, this indicates it is going to change the power allocated to the  
549 PD. In a PD, this indicates it is going to request a new power allocation from the PSE.  
550 Values:  
551 FALSE: The local system does not wants to change the power allocation.  
552 TRUE: The local system wants to change the power allocation.  
553

554 parameter\_type  
555 A Type 1 and 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised  
556 through Data Link Layer classification. Type 3 and 4 PSE state diagrams do not use this variable.  
557 Values:  
558 1: Type 1 PSE parameter values (default).  
559 2: Type 2 PSE parameter values.  
560  
561

562 **pd\_dll\_enabled**  
563 A variable output by the PD state diagram (Figure 33–32) to indicate if the PD Data Link Layer  
564 classification mechanism is enabled.  
565 Values:  
566 FALSE: PD Data Link Layer classification is not enabled.  
567 TRUE: PD Data Link Layer classification is enabled.  
568  
569 **pd\_dll\_power\_type**  
570 A Type 1 and Type 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as  
571 advertised through Data Link Layer classification. Type 3 and Type 4 PSE state diagrams do not use this variable.  
572 Values:  
573 1: PD is a Type 1 PD (default).  
574 2: PD is a Type 2 PD.  
575  
576 **pd\_dll\_ready**  
577 An implementation-specific control variable that indicates that the PD has initialized Data Link  
578 Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).  
579 Values:  
580 FALSE: Data Link Layer classification has not completed initialization.  
581 TRUE: Data Link Layer classification has completed initialization.  
582  
583 **pse\_dll\_enabled**  
584 A variable output by the PSE state diagram (Figure 33–13) to indicate if the PSE Data Link Layer  
585 classification mechanism is enabled.  
586 Values:  
587 FALSE: PSE Data Link Layer classification is not enabled.  
588 TRUE: PSE Data Link Layer classification is enabled.  
589  
590 **pse\_dll\_power\_type**  
591 A control variable output by the PD power control state diagram, defined in Figure 33–49, that indicates the PSE Type as  
592 1 or 2, see 79.3.2.4.1.  
593 Values:  
594 1: The PSE is a Type 1 PSE, for a Type-1 PSE.  
595 2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSEs  
596  
597 **pse\_dll\_ready**  
598 An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification.  
599 This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).  
600 Values:  
601 FALSE: Data Link Layer classification has not completed initialization.  
602 TRUE: Data Link Layer classification has completed initialization.  
603  
604 **pse\_power\_type**  
605 A control variable that indicates to the PD the type of PSE by which it is being powered.  
606 Values:  
607 1: The PSE is a Type 1 PSE.  
608 2: The PSE is a Type 2, Type 3, or Type 4 PSE.  
609  
610 **pd\_dll\_single\_or\_dual**  
611 A control variable output by PD power control state diagram, defined in Figure 33-49, that indicates if the PD is single-signature PD or dual-  
612 signature PD. Type 3 and Type 4 PD state diagrams do not use this variable.  
613 Values:  
614 single: A single-signature PD configuration is connected to the PI.  
615 dual: A dual-signature PD configuration is connected to the PI.  
616  
617 **pse\_dll\_single\_or\_dual**  
618 A control variable output by PSE power control state diagram defined in Figure 33-48 (generated from the do\_cxn\_check function of the Type  
619 3 and Type 4 PSE state diagram in Figure 33-15) which indicates if the PSE is connected to a single-signature PD or dual-signature PD.  
620 Values:  
621 invalid: Neither a single-signature PD nor a dual-signature PD connection check signature has been  
found. This includes an open circuit condition.  
single: A single-signature PD configuration is connected to the PI.  
dual: A dual-signature PD configuration is connected to the PI.

622 **33.5.3.1.9 Functions**

623 `pse_power_review_(M)`

624 This function evaluates the PSE power allocation or **power** budget of the PSE over Alternative(M) based on local system  
625 changes. See PD Load bit in 79.3.2.6b.3. The function returns the following variables:

626 `PSE_NEW_VALUE`:

627 The new maximum power value that the PSE expects the PD to draw over Alternative(M). Actual power numbers are  
628 represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of  
629 `PSE_NEW_VALUE_(M)`.

630

631 `pd_power_review_(M)`

632 This function evaluates the power requirements of the PD based on local system changes and/or  
633 changes in the PSE allocated power value. See PD Load bit in 79.3.2.6b.3. The function returns the following variables:

634 `PD_NEW_VALUE_mode(M)`:

635 The new maximum power value that the PD wants to draw. Actual power numbers are represented using an integer  
636 value that is encoded according to Equation (79–1), where *X* is the decimal value of `PD_NEW_VALUE_(M)`.

637

638

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640 **8. Copy Table 33-41 from the single-signature section and make the following**  
641 **changes:**

- 642 1. Change the Table number from 33-41 to 33-41a. The text of the title remains the same.  
643 2. Add suffix `_(M)` to all variables.  
644 3. Add the new added variables to the table.

645

646

647 **9. Update the following PSE state diagram Figure 33-48a**  
 648 **9.1 Editor to replace all terms with the suffix “\_mode(M)” with the suffix “\_(M)” in Figure 33-48a and**  
 649 **Figure 33-49a.**

650 *(The reason is that some of the variables belong to PSE state machine and some to the PD state machine and the term*  
 651 *“mode” is reserved for the PD.)*

652  
 653 **33.5.3.1.10 State diagrams**

654  
 655 The general state change procedure for PSEs is shown in Figure 33-48a.  
 656  
 657

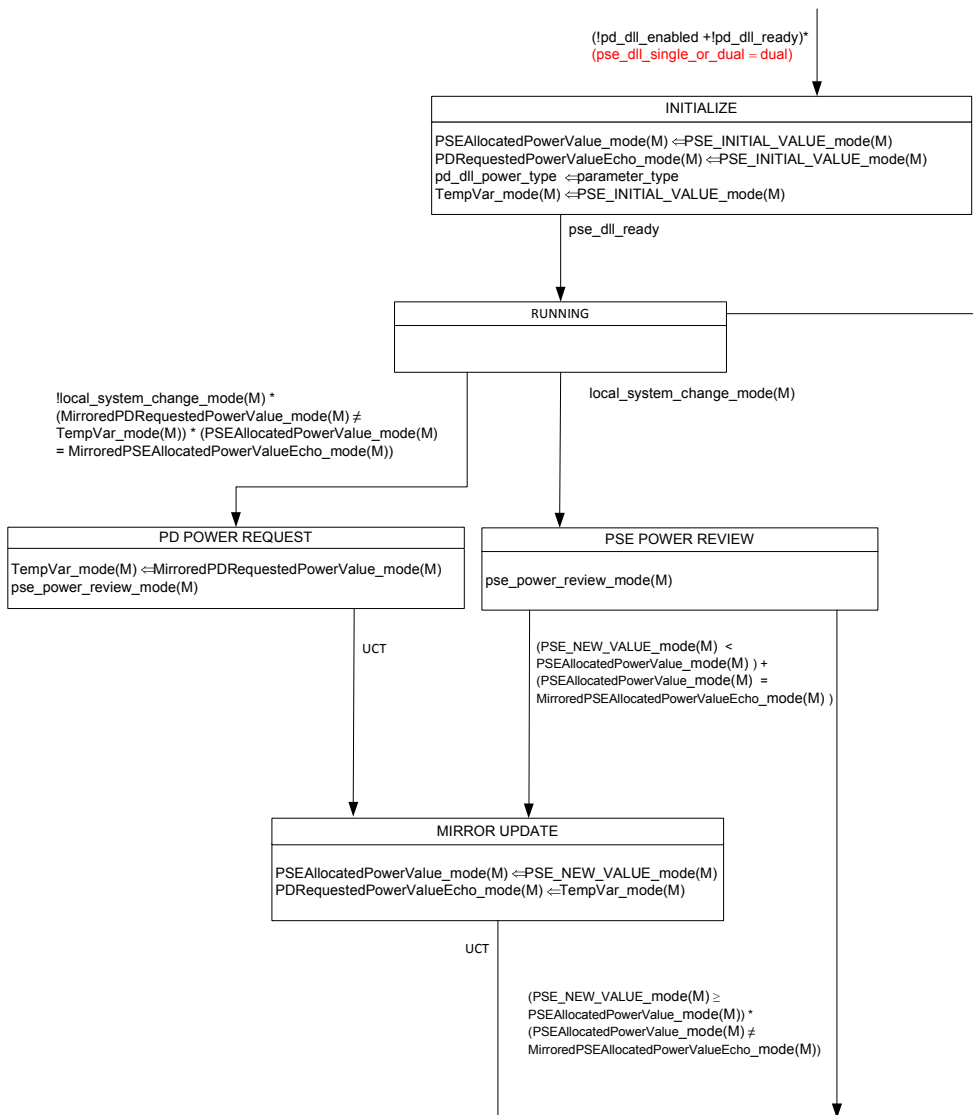


Figure 33-48A—PSE power control state diagram when connected to dual-signature PD

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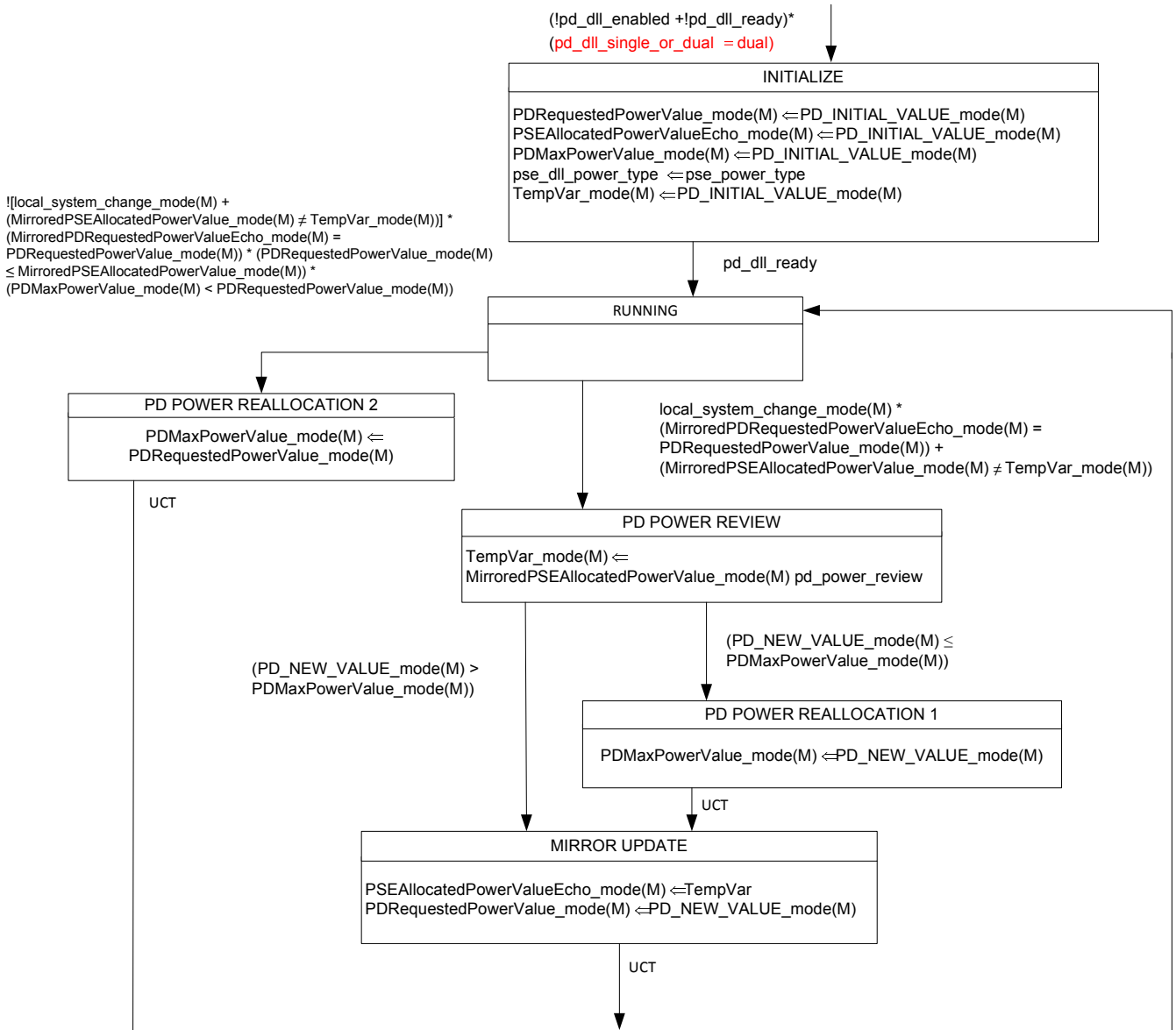


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**10. Update the following PSE state diagram Figure 33-49a**

**10.1 Editor to replace all terms with the suffix “\_mode(M)” with the suffix “\_(M)” in Figure 33-48a and Figure 33-49a. (The reason is that some of the variables belong to PSE state machine and some to the PD state machine and the term “mode” is reserved for the PD.)**

The general state change procedure for PDs is shown in Figure 33–49A.



**Figure 33–49A—Dual-signature PD power control state diagram**

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## 11. Add the following text:

### 33.5.3.2 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the `aLldpXdot3LocPDRRequestedPowerValue_(M)` (30.12.2.1.17) attribute in the `oLldpXdot3LocSystemsGroup_(M)` object class. The request appears to the PSE as a change to the `aLldpXdot3RemPDRRequestedPowerValue_(M)` (30.12.3.1.17) attribute in the `oLldpXdot3RemSystemsGroup_(M)` object class.

The PSE responds to the PD's request through the `aLldpXdot3LocPSEAllocatedPowerValue_(M)` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup_(M)` object class. The PSE also copies the value of the `aLldpXdot3RemPDRRequestedPowerValue_(M)` (30.12.3.1.17) in the `oLldpXdot3RemSystemsGroup_(M)` object class to the `aLldpXdot3LocPDRRequestedPowerValue_(M)` (30.12.2.1.17) in the `oLldpXdot3LocSystemsGroup_(M)` object class.

The PSE may allocate a new power value through the `aLldpXdot3LocPSEAllocatedPowerValue_(M)` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup_(M)` object class. The request appears to the PD as a change to the `aLldpXdot3RemPSEAllocatedPowerValue_(M)` (30.12.3.1.18) attribute in the `oLldpXdot3RemSystemsGroup_(M)` object class. The PD responds to a PSE's request through the `aLldpXdot3LocPDRRequestedPowerValue_(M)` (30.12.2.1.17) attribute in the `oLldpXdot3LocSystemsGroup_(M)` object class. The PD also copies the value of the `aLldpXdot3RemPSEAllocatedPowerValue_(M)` (30.12.3.1.18) attribute in the `oLldpXdot3RemSystemsGroup_(M)` object class to the `aLldpXdot3LocPSEAllocatedPowerValue_(M)` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup_(M)` object class. This appears to the PSE as a change to the `aLldpXdot3RemPDRRequestedPowerValue_(M)` (30.12.3.1.17) attribute in the `oLldpXdot3RemSystemsGroup_(M)` object class.

The state diagrams describe the behavior above.

#### 33.5.3.2.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of `PSEAllocatedPowerValue_(M)` matches the value of `MirroredPSEAllocatedPowerValueEcho_(M)`. When the PSE is not in sync with the PD, the PSE is allowed to change its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the `local_system_change_(M)` is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, `PSE_NEW_VALUE_(M)`, is computed. If the PSE is in sync with the PD or if `PSE_NEW_VALUE_(M)` is smaller than `PSEAllocatedPowerValue_(M)`, it enters the MIRROR UPDATE state where `PSE_NEW_VALUE_(M)` is assigned to `PSEAllocatedPowerValue_(M)`. It also updates `PDRRequestedPowerValueEcho_(M)` and returns to the RUNNING state.

If the PSE's previously stored `MirroredPDRRequestedPowerValue changes_(M)`, a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, `PSE_NEW_VALUE_(M)`, is computed. It then enters the MIRROR UPDATE state where `PSE_NEW_VALUE_(M)` is assigned to `PSEAllocatedPowerValue_(M)`. It also updates `PDRRequestedPowerValueEcho_(M)` and returns to the RUNNING state.

#### 33.5.3.2.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of `PDRRequestedPowerValue_(M)` matches the value of `MirroredPDRRequestedPowerValueEcho_(M)`. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD's previously stored `MirroredPSEAllocatedPowerValue_(M)` is changed or `local_system_change_(M)` is asserted by the PD so as to change its power allocation, the PD enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called `PD_NEW_VALUE_(M)`. If `PD_NEW_VALUE_(M)` is less than `PDMaxPowerValue_(M)`, it updates `PDMaxPowerValue_(M)` in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where `PD_NEW_VALUE_(M)` is assigned to `PDRRequestedPowerValue_(M)`. It also updates `PSEAllocatedPowerValueEcho_(M)` and returns to the RUNNING state.

In the above flow, if `PD_NEW_VALUE_(M)` is greater than `PDMaxPowerValue_(M)`, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD POWERREALLOCATION 2 state. In this state, the PD assigns `PDMaxPowerValue_(M)` to `PDRRequestedPowerValue_(M)` and returns to the RUNNING state.

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**12. Make the following changes to clause 79:**

**79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements**

**This is not part of the baseline**  
 -The power typex bits were updated to differentiate between single and dual signature PD.  
 -PD mode selection was updated to allow using the same bit for both PSE and PD depending who is the source of the LLDP PDU.

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**Table 79–5b—System setup value field**

Bit	Function	Value/meaning																																																																																					
7:4	Power typex	<table border="0"> <tr> <td><u>7</u></td> <td><u>6</u></td> <td><u>5</u></td> <td><u>4</u></td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1= Type 4 dual-signature PD <del>Reserved/Ignore</del></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>0= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1= Type 3 dual-signature <del>Reserved/Ignore</del></td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1= Type 4 <a href="#">single-signature</a> PD</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0= Type 4 PSE</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1= Type 3 <a href="#">single-signature</a> PD</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0= Type 3 PSE</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1= Type 2 PD</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0= Type 2 PSE</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1= Type 1 PD</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0= Type 1 PSE</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1= Reserved/Ignore</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0= Reserved/Ignore</td> </tr> </table>	<u>7</u>	<u>6</u>	<u>5</u>	<u>4</u>		1	1	1	1	1= Type 4 dual-signature PD <del>Reserved/Ignore</del>	1	1	1	0	0= Reserved/Ignore	1	1	0	1	1= Type 3 dual-signature <del>Reserved/Ignore</del>	1	1	0	0	0= Reserved/Ignore	1	0	1	1	1= Reserved/Ignore	1	0	1	0	0= Reserved/Ignore	1	0	0	1	1= Type 4 <a href="#">single-signature</a> PD	1	0	0	0	0= Type 4 PSE	0	1	1	1	1= Type 3 <a href="#">single-signature</a> PD	0	1	1	0	0= Type 3 PSE	0	1	0	1	1= Type 2 PD	0	1	0	0	0= Type 2 PSE	0	0	1	1	1= Type 1 PD	0	0	1	0	0= Type 1 PSE	0	0	0	1	1= Reserved/Ignore	0	0	0	0	0= Reserved/Ignore
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0	0	1	0	0= Type 1 PSE																																																																																			
0	0	0	1	1= Reserved/Ignore																																																																																			
0	0	0	0	0= Reserved/Ignore																																																																																			
3	PD 4PID	1= PD supports powering of both modes 0= PD does not support powering of both modes																																																																																					
2	Reserved	Transmit as zero. Ignore on receive.																																																																																					
1	PD Load	1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated. 0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated.																																																																																					
0	PD Mode selection	1 = PD requested power applies to Mode A pairset 0 = PD requested power applies to Mode B pairset																																																																																					

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**79.3.2.6b.5 PD Mode selection**

This field shall be set according to Table 79–5b to select the Mode for which the PD is requesting power when the **power typex (bits 7:4)** is PD and a dual-signature PD (see 1.4.186a and 33.3.2) is the source of the LLDP PDU.

**13. Make the following changes to clause 79, page 218 line 39:**

PD requested power value	PSE allocated power value	PD requested power value mode A	PD requested power value mode B	PSE allocated power value ALT A	PSE allocated power value ALT B	PSE power status	System setup	PSE maximum available power	Autoclass	Power down
--------------------------	---------------------------	---------------------------------	---------------------------------	---------------------------------	---------------------------------	------------------	--------------	-----------------------------	-----------	------------

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**End Of Proposed Baseline**

756 Annex A: To be considered by the group:

757

758 The current TLV format in D2.1 is:

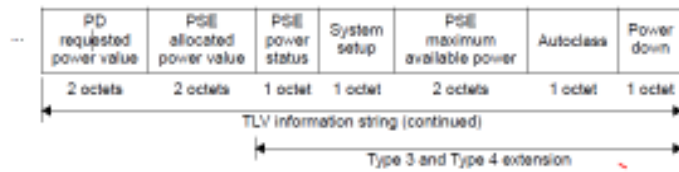


Figure 79-3—Power Via MDI TLV format

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760

761 In this concept (Option 2) the TLV structure need to be:

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Advantages: In a single transaction we know if we want to work on ModeA or ModeB even if there is no local\_system\_change request. If we depend only on pd\_mode\_selection bits then even if we don't have local\_system\_change request, we will need to transmit all the information again any time pd\_mode\_selection bits flips between "0" and "1".

PD requested power value	PSE allocated power value	PD requested power value mode A	PD requested power value mode B	PSE allocated power value ALT A	PSE allocated power value ALT B	PSE power status	System setup	PSE maximum available power	Autoclass	Power down
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Or It can be:

PD requested power value <b>or</b> PD requested power value mode A	PSE allocated power value <b>or</b> PSE allocated power value ALT A	PD requested power value mode B	PSE allocated power value ALT B	PSE power status	System setup	PSE maximum available power	Autoclass	Power down
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To discuss which is preferred.