Comment (Comments: #74, #37, #108, #83)

(1) The following Dual-signature PD state diagram baseline was approved in September 2016 however parts of it were not implemented. See http://www.ieee802.org/3/bt/public/sep16/darshan_09_0915Rev005.pdf option 2.

(2) Pse_dll_power_level_mode(M) is not used in the dual-signature state machine and should be deleted.

(3) PSE dll_power_type should be the same for Mode A and Mode B.

Suggested Remedy:

1. Update according to the following proposed baseline.

33.3.3 PD state diagram

Add the following text:

Lines 17-20 was in the approved baseline from September 2016 and was not implemented. See ref 1 in the comment above. David Abramson improved version of it from comment #37 is show below.

The PD state diagram specifies the externally observable behavior of a PD. Type 1 and Type 2 PDs shall provide the behavior of the state diagram shown in Figure 33–31. Single-signature Type 3 and Type 4 PDs shall provide the behavior of the state diagram show in Figure 33–32. Dual-signature Type 3 and Type 4 PDs shall provide the behavior of the state diagram shown in Figure 33–33.

Dual-signature Type 3 and Type 4 PDs shall provide the behavior of the state diagram shown in Figure 33–33 over each pairset independently unless otherwise specified. All the parameters that apply to mode A and mode B are denoted with the suffix "_mode(M)" where "M" can be "A" or "B". A parameter that ends with the suffix "_mode(M)" may have different values for mode A and mode B."

33.3.3.15 was moved to this location to be defined before it is used.

~~33.3.3.15~~ 33.3.3.x.x Mode designation

PD Modes are referred to by the letter 'A' or 'B' for Mode A and Mode B respectively. Mode information is obtained by replacing the M in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

M

Generic Mode designator. When M is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.

33.3.3.11 Type 3 and Type 4 dual-signature constants

The PD state diagram uses the following constants:

V_{Reset}

Reset voltage per pairset (see Table 33–29)

V_{Reset_th}

Reset voltage threshold per pairset (see Table 33–29)

V_{Mark_th}

Mark event voltage threshold per pairset (see Table 33–29)

pd_req_class_mode(M)

A constant indicating the requested Class of the PD over mode M.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

33.3.3.12 Type 3 and Type 4 dual-signature variables

The PD state diagram uses the following variables:

mdi_power_required_ mode(M)
: A control variable indicating that over mode M, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.
Values:
FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

pd_dll_enabled
A variable indicating whether the Data Link Layer classification mechanism is enabled.
Values:
FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pd_max_power_ mode(M)
: A control variable indicating the max power that the PD may draw from the PSE over mode M. See power classifications in Table 33–31.
Values:
1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power
5: PD may draw Class 5 power

pd_reset_ mode(M)
: An implementation-specific control variable that unconditionally resets the PD state diagram over mode M to the OFFLINE_ mode(M) state.
Values:
FALSE:The device has not been reset (default).
TRUE:The device has been reset.

pd_undefined_ mode(M)
: A control variable that indicates that the PD is in an undefined condition over mode M. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeA variable.
Values:
FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

power_received_ mode(M)
: An indication from the circuitry that power is present on the PD's PI over mode M.
Values:
FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–31.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

present_class_sig_A_ mode(M)
: Controls presenting the classification signature that is used during first two class events (see 33.3.6) by the PD over mode M.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B_ mode(M)
: Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode M (see 33.3.6) by the PD.

Values:

FALSE:The PD classification signature is not to be applied to the link.

TRUE:The PD classification signature is to be applied to the link.

present_det_sig_ mode(M)

Controls presenting the detection signature (see 33.3.4) by the PD over mode M.

Values:

invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.

valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.

either: Either a valid or non-valid PD detection signature may be applied to the link.

present_mark_sig_mode(M)

Controls presenting the mark event current and impedance (see 33.3.6.2.1) by the PD over mode M.

Values:

FALSE:The PD does not present mark event behavior.

TRUE:The PD does present mark event behavior.

present_mps_mode(M)

Controls applying MPS over mode M (see 33.3.8.10) to the PD's PI.

Values:

FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.

TRUE:The MPS is to be applied to the PD's PI.

Pse_dll_power_level_mode(M) is not used in the PD dual-signature state machine.

~~pse_dll_power_level_mode(M)~~

~~A control variable output by the PD power control state diagram (Figure 33-49) that indicates the power level of the PSE by which the PD is being powered over mode M.~~

~~Values:~~

~~1: The PSE has allocated Class 3 power or less (default).~~

~~2: The PSE has allocated Class 4 power.~~

~~3: The PSE has allocated Class 5~~

PSE dll_power_type is the same for Mode A and Mode B.

pse_dll_power_type

A control variable output by the PD power control state diagram (Figure 33-49) that indicates the PSE type connected to the PD ~~to mode M~~ as 1 or 2, see 79.3.2.4.1.

Values:

1: The PSE is a Type 1 PSE, for a Type-1 PSE.

2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE.

pse_power_level_mode(M)

A control variable that indicates to the PD over mode M the level of power the PSE is supplying.

Values:

3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.

4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.

5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

VPD_mode(M)

Voltage at the PD PI as defined in 1.4.425 over mode M.

33.3.3.13 Type 3 and Type 4 dual-signature timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer_mode(M)
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode M and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode M during the PSE's inrush period; see $T_{delay-2P}$ in Table 33–31.

33.3.3.14 Type 3 and Type 4 dual-signature functions

do_class_timing_mode(M)
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over Mode M. The class event timing requirements are defined in Table 33–29. This function returns the following variable:

long_class_event_mode(M): A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.9) the PD should use. Values:
TRUE: The PSE is identified as a Type 3 or Type 4 PSE.
FALSE: The PSE is identified as a Type 1 or Type 2 PSE.

2. Make the following changes to the state diagram:

Page 145 Figure 33-33: Replace '"Vpd(M)" with "Vpd_mode(M)"

Page 146 Figure 33-33: Update the stste machine as follows:

(*) Same improvement was used in single-signature state diagram and may be implemented here as well.
(**) It is pse_power_level and not pse_power_type as in the approved baseline from September 2016 and was not implemented. See ref 1.

Make the following changes in Figure 33-33 on page 136 (marked in Blue):

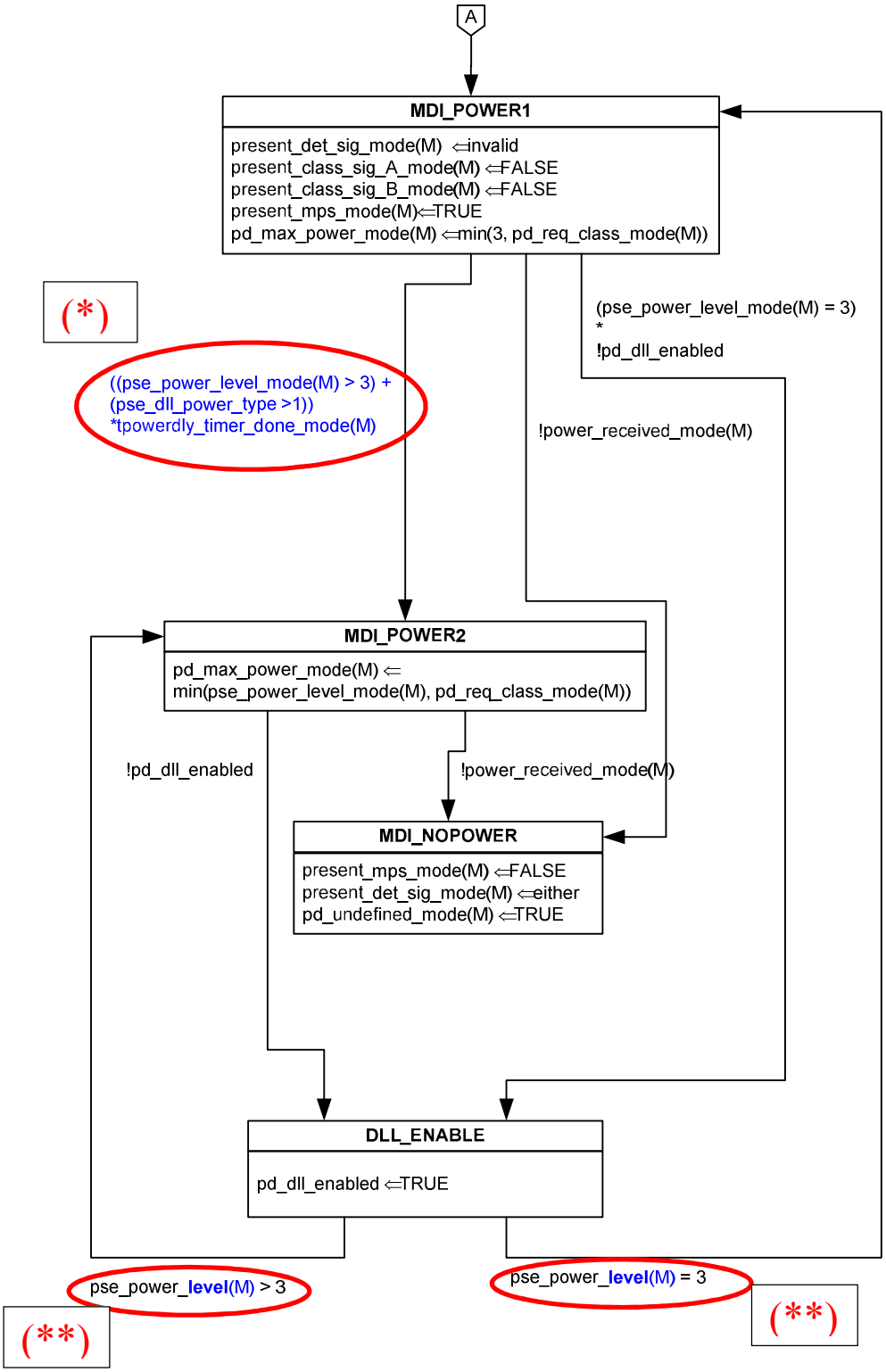

Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram *(continued)*

Base Line ends here

Revision History

#	Revision	Draft	Changes made
1	002	1.8	----------
2	003	2.0	1. Deleting unused variables. 2. Deleting suffix “modeA’ from pd_dll_enabled and delete pd_dll_enabled_modeB 3. pse_dll_power_type was added. 4. Figures 33-33 and 33-34 where updated accordingly.
3	004		Optional solution to further simplifying dual-signature state machine was added (Option B). Suffix “X” was changed to “Y” since “X” is used in other places.
4	006		Updates for D2.1 after adopting option B.