pse_dll_power_type

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pse_power_type Phrasing Indicative of Overwhelmed Variable

pse_dll_power_type

A control variable output by the PD power control state diagram, defined in Figure 33–49, that indicates the PSE Type as 1 or 2, see 79.3.2.4.1.

Values:

1: The PSE is a Type 1 PSE~~, for a Type 1 PSE~~

2: The PSE is a ~~Type 2~~ not a Type 1 PSE~~, for Type 2, Type 3, or Type 4 PSEs~~

Step One

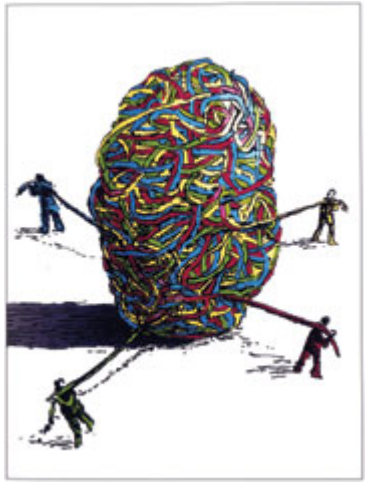
Improve pse_dll_power_type description

pse_power_type Usage and Validation

- Type 1 and 2 PSE SM
  - parameter_type
- Type 3 and 4 PSE SM
  - <none>

- Type 1 and 2 PD SM
  - pse_dll_power_type
  - pse_power_type
- Type 3 and 4 SS PD SM
  - pse_dll_power_type
  - pse_power_level
- Type 3 and 4 DS PD SM
  - pse_dll_power_type
  - pse_power_level_mode(M)

- PD Power Control SM
  - aLldpXdot3RemPowerType
  - pd_dll_power_type
  - parameter_type
- PSE Power Control SM
  - aLldpXdot3RemPowerType
  - pse_power_type
  - pse_dll_power_type



Step Two

Validate step one change by following pse_dll_power_type

Context – Type 1 / Type 2 PD SM

- pse_power_type is used to inform the DLL via the Power Control SM of the attached PSE's Type (1 or 2)

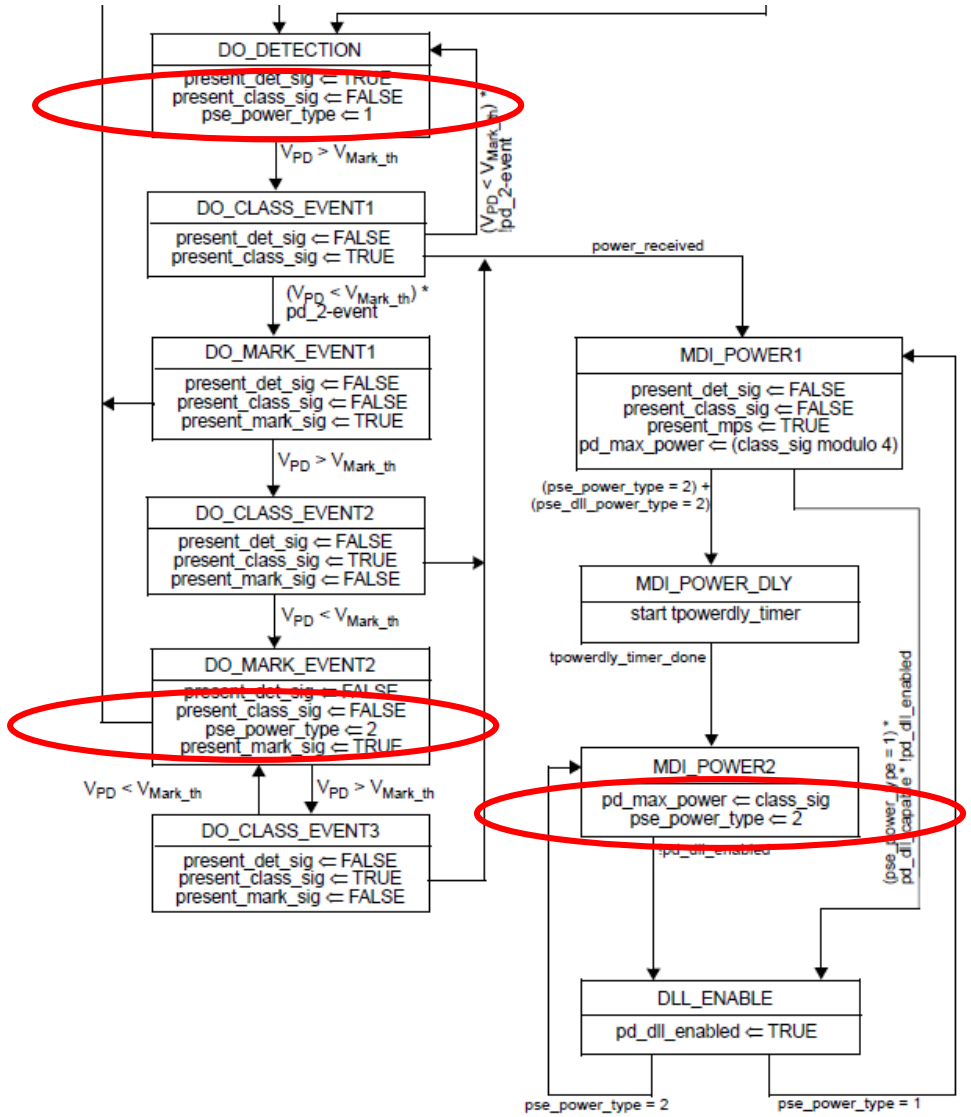


Figure 33–31—Type 1 and Type 2 PD state diagram

Additional Issue – Type 3 / Type 4 SS PD SM

- tpowerdly_timer should block DLL_ENABLE (thus MDI_POWER2)
- pse_power_level is the analogue of the Type 1/Type 2 PSE pse_power_type
  - pse_dll_power_type of D2.0 is incorrect

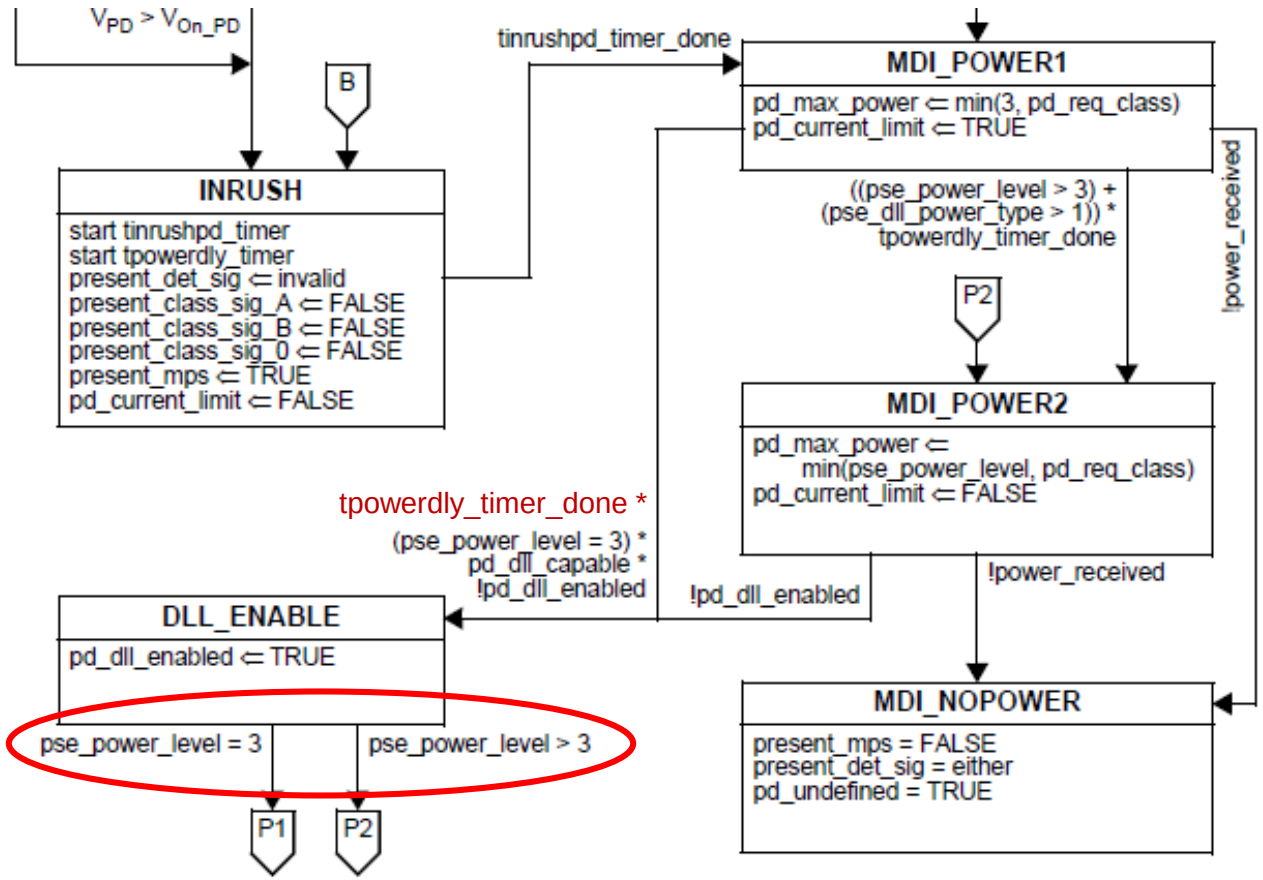
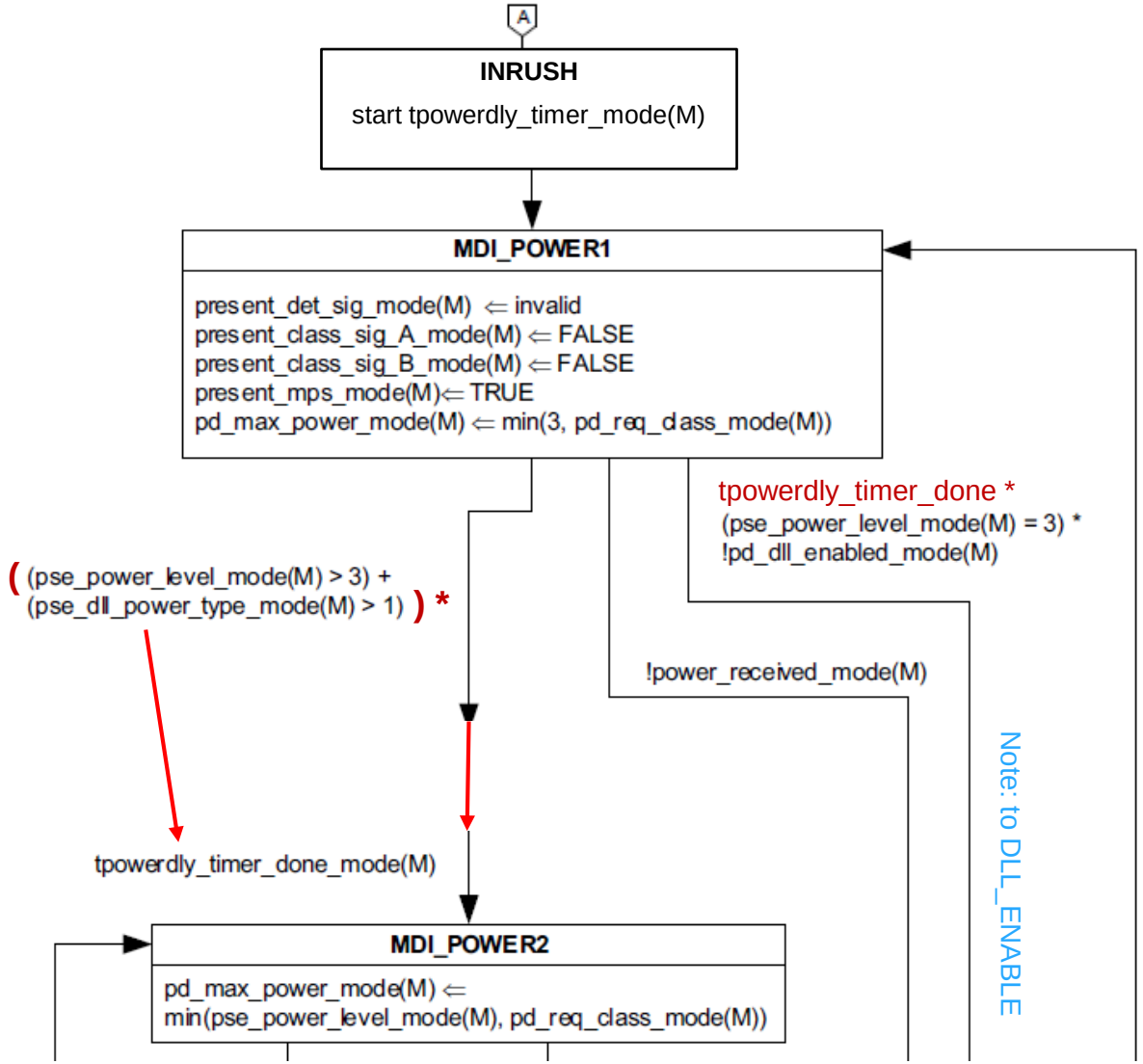


Figure 33–32—Type 3 and Type 4 single-signature PD state diagram *(continued)*

Additional Issue – Type 3 / Type 4 DS PD SM

- MDI_POWER_DELAY can collapse out (per YD #83)
  - Needed for rest of solution thus repeated here
- tpowerdly_timer should block DLL_ENABLE (thus MDI_POWER2)



Additional Issue – Type 3 / Type 4 DS PD SM

- Per YD #69
  - pse_power_type should be pse_power_level_mode(M)
  - pse_power_level_mode(M) is the analogue of the Type 1/Type 2 PSE pse_power_type

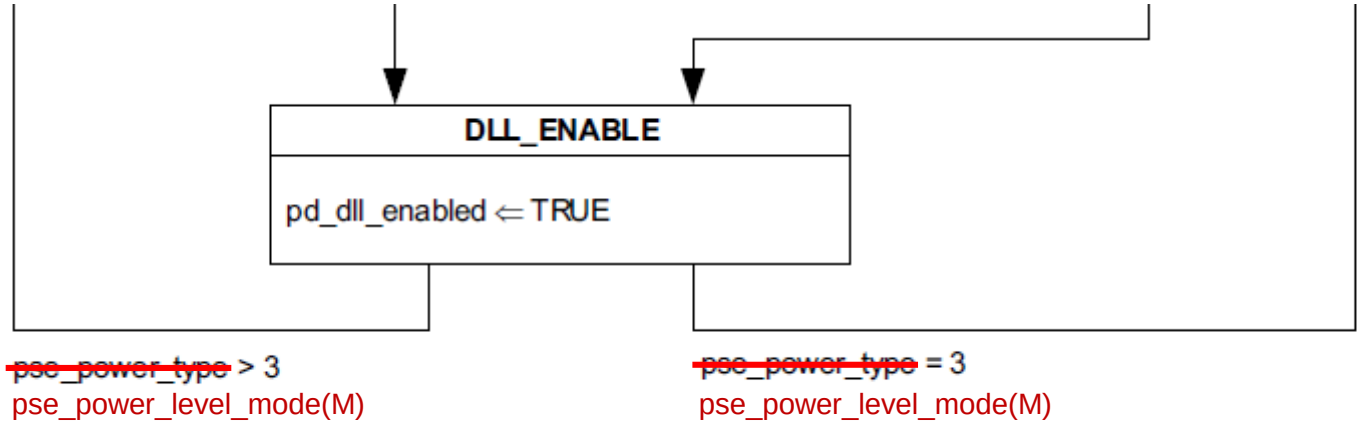


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram *(continued)*

Additional Issue – PSE Type Identification

33.3.7 PSE Type identification

A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 as shown in Figure 33–31. The default value of pse_power_type is 1. After a successful Multiple-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_type is set to 2. The Type 2 PD resets the pse_power_type to ‘1’ when the PD enters the DO_DETECTION state.

Type 3 and Type 4 PDs may determine the Type of the PSE they are connected to by measuring the length of the first class event. The default value for long_class_event is FALSE, which indicates the PSE is a Type 1 or Type 2 PSE. The PD may set long_class_event to TRUE if the first class event is longer than TLCE_PD min and shall set long_class_event to TRUE if the first class event is longer than TLCE_PD max. This indicates the PSE is Type 3 or Type 4 PSE. This determination allows the PD to make use of short MPS to reduce standby power

This text may need to be touched based on closure with PSE/PD Power Control SMs (next two slides)

Additional Issue – PD Power Control SM pse_power_type

- pse_power_type is undefined for Type 3/Type 4 PDs
- Instead pse_power_level and pse_power_level_mode(M) exist

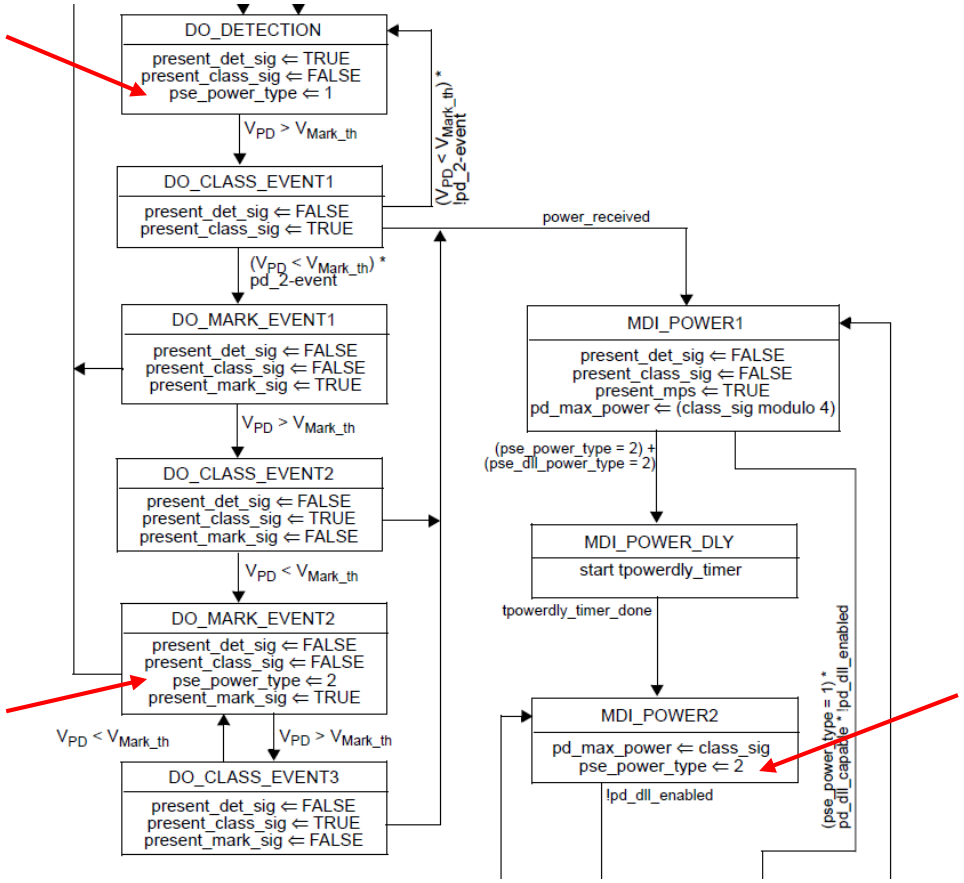


Figure 33–31—Type 1 and Type 2 PD state diagram

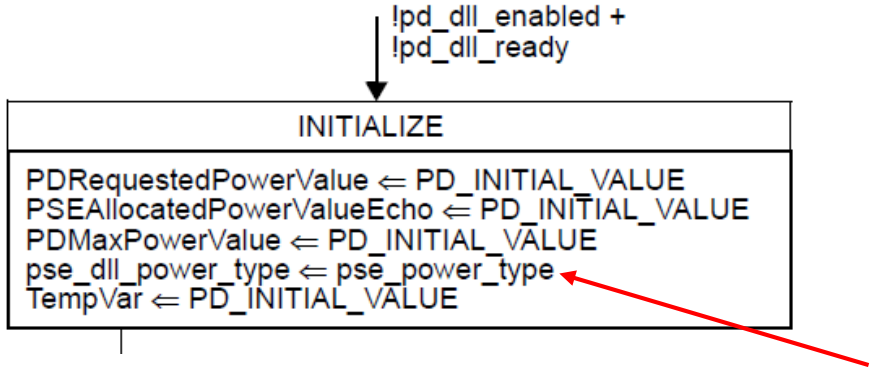


Figure 33–49—PD power control state diagram

Unsure of best solution…

Additional Issue – PSE Power Control SM parameter_type

- parameter_type is undefined for Type 3/Type 4 PSEs
- Unsure of best solution…

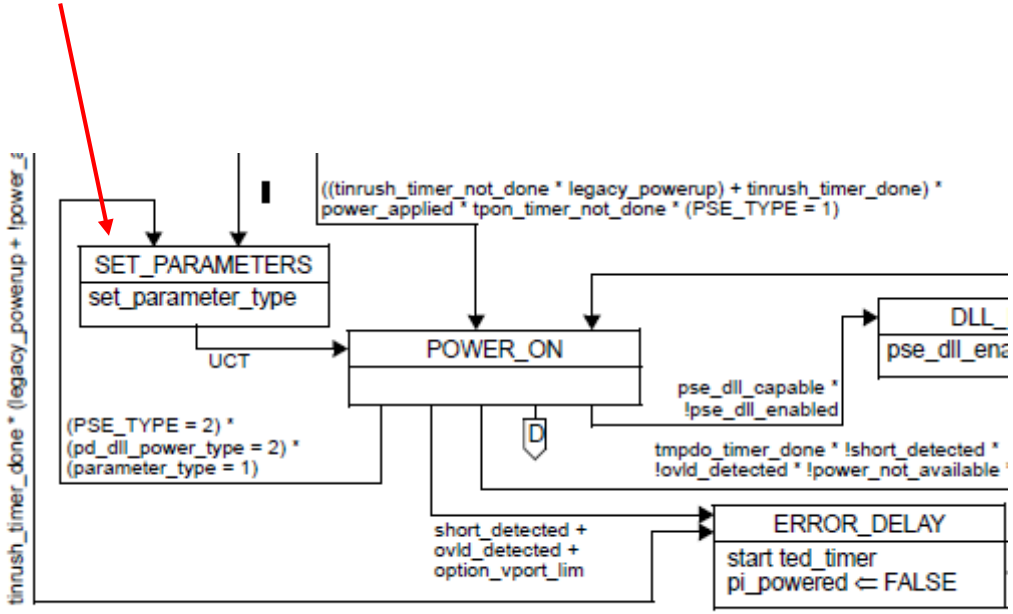


Figure 33–13—Type 1 and Type 2 PSE state diagram

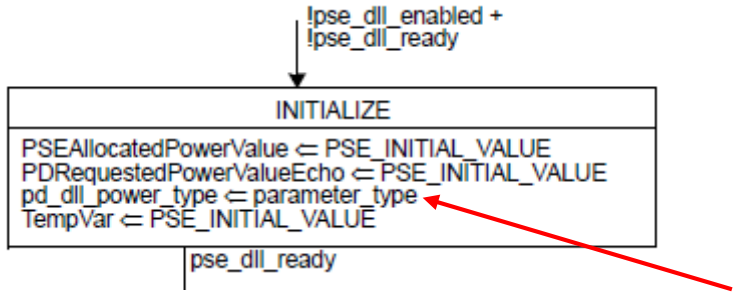


Figure 33–48—PSE power control state diagram