1. Comment r01-462 - Updating Figure 145-22 page 168 line 35, Figure 145-31 page 207 line 22 to sync with proposed text in comments r01-286, r01-287.
2. Addressing comment r01-378 regarding the need to split Rsource_min/max to Rsource1_min, Rsource2_min and Rsource1_max, Rsource2_max for setting the correct PSE voltage at the PSE PI to allow adjusting Vsource to get VPort_PSE-2P at the PSI PI. This comment is addressed in a simpler way.

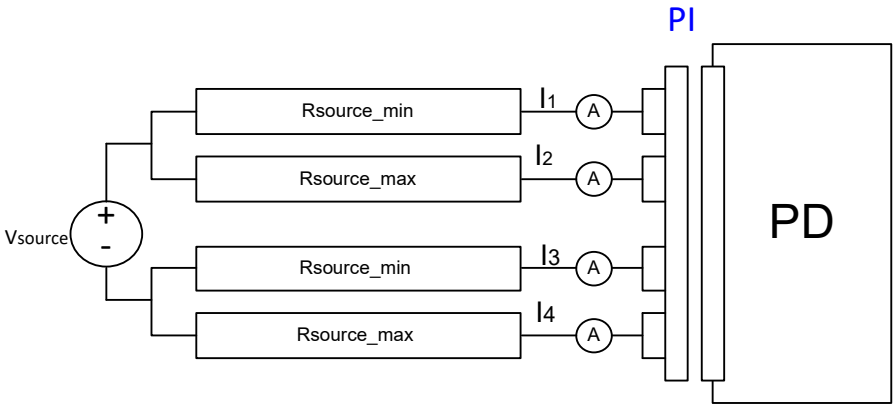
Per the latest changes we did to include equipment connector in the PSE PI and in the PD PI for unbalance tests the following changes should be made:

a) Figure 145-22, the borders of the test verification model need to be clearly shown.
b) Figure 145-31 and NOTE 1 in line 33 need similar adjustments.

Proposed remedy:

1. ***Change the title of Figure 145-22 from:***
   "Figure 145–22—PSE PI unbalance specification and system resistance unbalance"
   To:
   "Figure 145–22—PSE current unbalance verification circuit"

2. ***Change figure 145-31 as follows:***



3. ***Change the title of Figure 145-31 from:***
   "Figure 145–31—Icon-2P_unb and Iunbalance evaluation model"
   To:
   "Figure 145–31—PD current unbalance verification circuit"
5. ***Delete Note 1 (***"OTE 1—Rsource includes the connector resistance at the PD PI, for which the maximum recommended value is 20 mΩ per contact.)
6. ***Make the following changes to NOTE 2:***

   NOTE 2—The pairset current limit~~s~~ requirement also holds ~~should also be met~~ when Rsource_max and Rsource_min are ~~swapped~~ exchanged~~between pairs of the same polarity~~.

7. Change the following text in page 206 line 24 as follows:

Single-signature PDs shall not exceed IUnbalance-2P for longer than TCUT min and 5 % duty cycle, and shall not exceed IPeak-2P-unb, as defined in Equation (145–12) on any pair when PD PI pairs of the same polarity are connected to any voltage in the range of VPort_PSE-2P min+0.31V to VPort_PSE-2P max through two common mode resistances, Rsource_min and Rsource_max, as defined in Equation (145–27) and shown in Figure 145–31.

Dual-signature PDs shall not exceed ICon_PD-2P, as defined in Equation (145–28), for longer than TCUT-2P min and 5 % duty cycle, as defined in Table 145–16, and shall not exceed IPeak_PD-2P, as defined in Equation (145–29), on any pair when PD PI pairs of the same polarity are connected to any voltage in the range of VPort_PSE-2P min+0.31V to VPort_PSE-2P max through two common mode resistances, Rsource_min and Rsource_max, as defined in Equation (145–27) and shown in Figure 145–31.