Concurrency issues in the PSE state diagram (D3.1) v102

Info (not part of baseline)

There is an issue in the PSE state diagram where when sism=FALSE, both the toplevel state diagram and the Primary/Secondary state diagrams write in variables pd_4pair_cand, sig_pri, and sig_sec. This happens because of the assignment statements in the IDLE_PRI and IDLE_SEC states. In this baseline these are disabled by introducing a new holding state for the Primary and Secondary SISM state diagrams.

145.2.5.7 State diagrams

Change Figures in 145.2.5.7 as follows:

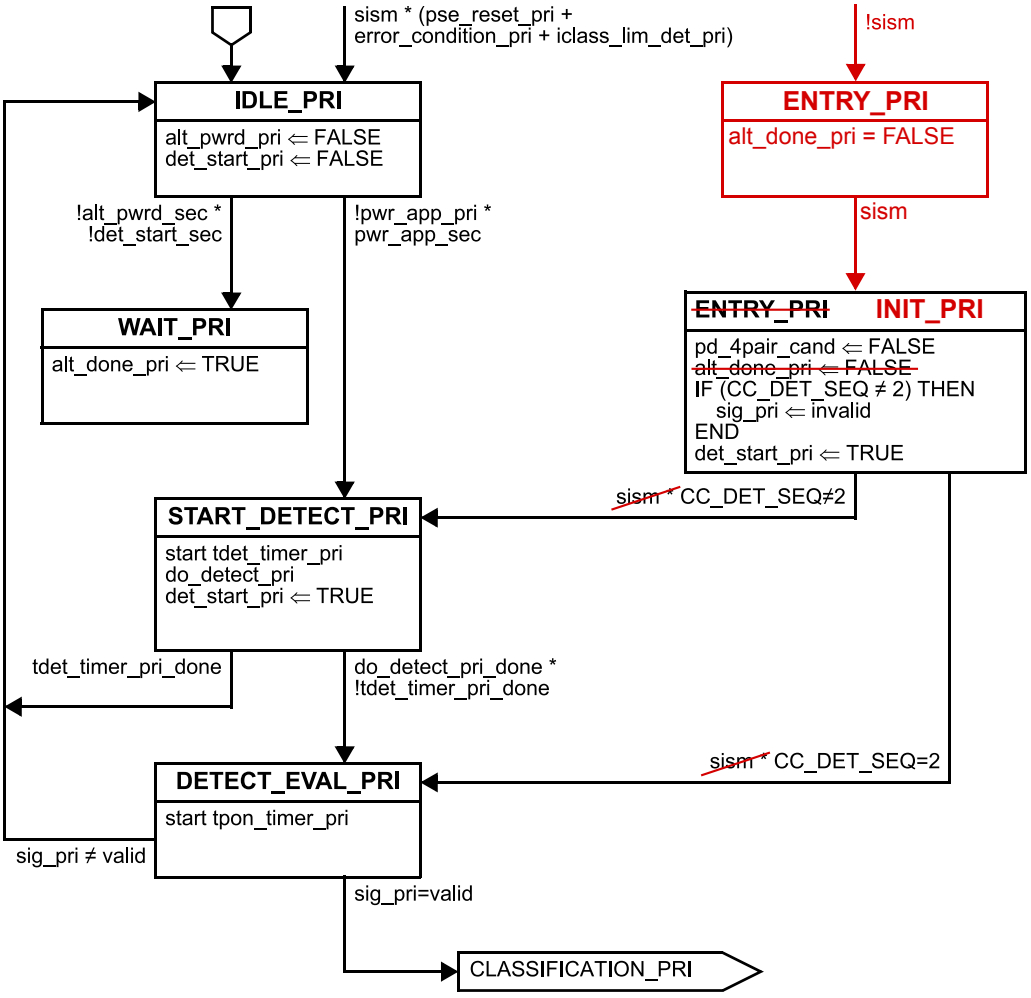

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram

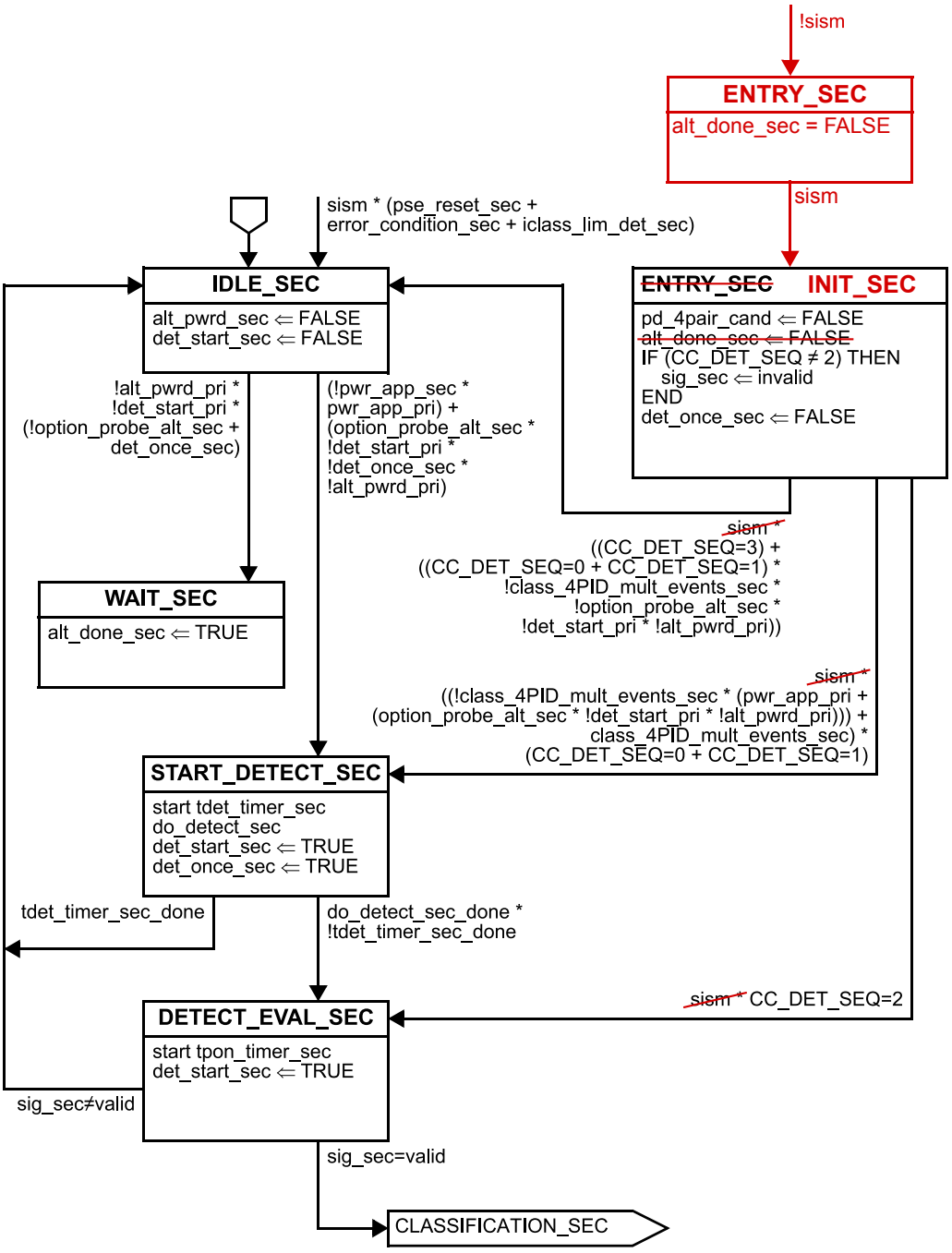

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram