Remedy for Comment #238

Original 33.2.7.5 text (with strikeouts removed):

33.2.7.5 Output current in POWER_UP mode

POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of $T_{Inrush-2P}$ or, for Type 1 and Type 2 PSEs that make use of legacy powerup, the conclusion of PD inrush currents on that pairset (see 33.3.7.3). Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a single-signature PD shall reach POWER_ON on both pairsets within $T_{Inrush-2P}$ max, starting with the first pairset transitioning into the POWER_UP state.

See legacy_powerup variable in section 33.2.4.4 for more information on the POWER_UP to POWER_ON transition.

The PSE shall limit the maximum current sourced per pairset during POWER_UP. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset inrush template in Figure 33–13 and Equation (33–5).

a) During POWER_UP, for pairset voltages between 0 V and 10 V, the minimum $I_{Inrush-2P}$ requirement is 5 mA.
b) During POWER_UP, for pairset voltages between 10 V and 30 V, the minimum $I_{Inrush-2P}$ requirement is 60 mA.
c) During POWER_UP, for pairset voltages above 30 V, the minimum $I_{Inrush-2P}$ requirement is as specified in Table 33–11.
d) For Type 1 PSE, measurement of minimum $I_{Inrush-2P}$ requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses Single-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a Class 4 PD as if it used Multiple-Event Physical Layer classification.

<figure 33-13>

The PSE inrush template, $I_{PSEIT-2P}$, is defined by the following segments:

<equation 33-5>

where *t* is the time in seconds

<end>

For reference, here are the Iinrush specs from Table 33-11:

5	Output current in POWER_UP state	I_{Inrush}	A	0.400	See info	~~1, 2,~~ All	For Type 1 and Type 2 PDs. See 33.2.7.5. Max value defined by Figure 33–13.

5a	Output current per pairset in POWER_UP state	$I_{Inrush-2P}$	A	0.400	See info	3, 4	For Type 3 and Type 4 PDs. See 33.2.7.5. Max value defined by Figure 33–13.
6	Inrush time per pairset	$T_{Inrush-2P}$	s	0.050	0.075	~~1, 2~~ All	See 33.2.7.5

The problem:

With 4-pair power and a single-load PD, balance during inrush is not accounted for in section 33.2.7.5. If one pair meets Iinrush-2p, the second pair may violate the minimum spec due to E2EUNB. Proposed solution:

1) Spec total current for SS PDs as Iinrush (= Iinrush-2p * 2). This would also apply to DS matched class PDs.
2) Additionally, spec the larger pair current to meet Iinrush-2p specs as written, and the smaller pair current with a relaxed Iinrush-2p minimum (by 19%? …should be the same as Class 4 unbalance)

Proposed new text:

Replace bullet c with:

c) During POWER_UP, for Type 1 and 2 PSEs with pairset voltages above 30 V, the minimum I_{Inrush} requirement is as specified in Table 33–11.

   For Type 3 and 4 PSEs with pairset voltages above 30 V, when connected to an SS PD or a DS PD with matching classification signatures, the minimum I_{Inrush} (total on both pairsets) and Iinrush-2p-unb (per pairset) requirements are as specified in Table 33–11.

   For pairset voltages above 30 V, when connected to a DS PD with unmatched classification signatures, the minimum $I_{Inrush-2P}$ requirement (per pairset) is as specified in Table 33–11.

And…

Add new Iinrush-2p-unb line to Table 33-11, specifying minimum current ~19% below the existing Iinrush-2p specs. Actual values TBD (for Iinrush, Iinrush-2p, and Iinrush-2p-unb) based on final consensus on inrush current values.

Note that this new bullet c text (inherited from af/at) does not include shalls. To include them, replace “requirement is” with “shall be” in three places.