Current Limits

IEEE802.3bt – September 2014 Interim

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Motivation

- Monitoring per two-pair is needed to avoid having to over-design components
- To explore possible current limits for the new IEEE802.3bt operating conditions
- This includes
  - Inrush Current limiting (Iinrush)
  - Overload Current limiting (Icut)
  - Short Circuit current limiting (Ilim)
- Type 3 and Type 4 terminologies used in this presentation follow http://www.ieee802.org/3/bt/public/may14/abramson_01a_0514.pdf

Inrush History

- Inrush was derived in IEEE 802.3 Std 2012 by considering a balance between

  1) Energy dissipation on the PSE chip packages during startup, where heavy voltage drop occurs on PSE until PD charges up

  2) To have decent enough PD power up time, EMI performance and system stability (which defines the PD cap and minimum PD operating voltage)

PD Capacitance

- IEEE 802.3 Std 2012 limits PD capacitance

  Cport < 180uf → PSE must do inrush limiting

  Cport > 180uf → PD must do inrush limiting

- **PD Capacitance for Type 3 and Type 4 PDs??**
  - In order to maintain backward compatibility
    - Type 3 and Type 4 PDs, at the minimum will need to do inrush control for caps > 180uf total on each pair-set. (Type 1/2 PSEs are two-pair systems)
    - Otherwise these PDs will not work with Type 1 and Type 2 PSEs
  - Same inrush control can be applied when Type 3 and 4 PDs are attached to Type 3 and 4 PSEs → simple solution and fits the need

PD Capacitance And Backward Compatibility

- To maintain Backward Compatibility with IEEE 802.3 Std 2012
  - **Cport per pair-set** for Type 3 and Type 4 PD should meet the following conditions

    Cport per pair-set < 180uf → PSE must do inrush limiting

    Cport per pair-set > 180uf → PD must do inrush limiting
- The above takes care of backward compatibility without limiting 4-pair PD implementations
  - As long as **Cport per pair-set** is same as IEEE 802.3 Std 2012 no backward compatibility issues will arise

NOTE: Cport per pair-set is the Cport seen by an attached PSE on two twisted pairs

Proposal for PD Capacitance

Section 33.3.7.3

Input inrush current at startup is limited by the PSE if Cport per pair-set < 180 µF, as specified in Table 33–11.

If Cport per pair-set ≥ 180 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} per pair-set max is satisfied.

NOTE:

1. Cport per pair-set is the Cport seen by an attached PSE on two twisted pairs

Proposal for Inrush Current

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
5	Output Current per pair-set in POWER_UP STATE	$I_{inrush-2p}$	A	0.400	See Info	1, 2	See 33.2.7.5. Max value defined by Figure 33–13.
				0.400		3,4	

- This wont create any backward compatibility problems
  - Type 1 and Type 2 PDs will power on fine with Type 3 and Type 4 PSEs.

- No energy implication or violation on PSE side
  - External FET solutions – No problem on FET SOA
    - FET SOA would anyway meet high power load conditions for Type 3/4.
  - Internal FET solutions
    - IEEE802.3af Inrush work already considers multi port internal FET chips and hence simultaneous multi port turn on – refer to slide 19 in backup
  - Inrush definition in IEEE offers fold-back as well

- Allows backward compatibility, interoperability without limiting PD implementations
  - Type 3/4 PDs can have just one cap shared across both pair-sets(OR)
  - Type 3/4 PDs can have separate cap on each pair-set, as long as Cport per pair-set is as per specifications

- Minimum requirement that meets rules and does not affect anything

Simplified Proposal

- Modify Item 5 of Table 33-11 in IEEE 802.3 Std 2012 as follows
  - Changes are shown in blue

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
5	Output Current per pair-set in POWER_UP State	$I_{inrush\text{-}2p}$	A	0.400	See info	1, 2, 3, 4	See 33.2.7.5. Max value defined by Figure 33–13.

- Modify Item 5 of Table 33-18 in IEEE 802.3 Std 2012 as follows
  - Changes are shown in blue

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional Information
5	Input Inrush Current per pair-set	$I_{inrush\_PD\text{-}2P}$	A		0.400	1,2,3,4	Peak Value-see 33.3.7.3

Inrush Figure proposal

- Modify Figure 33-13 in IEEE 802.3 Std 2012 to

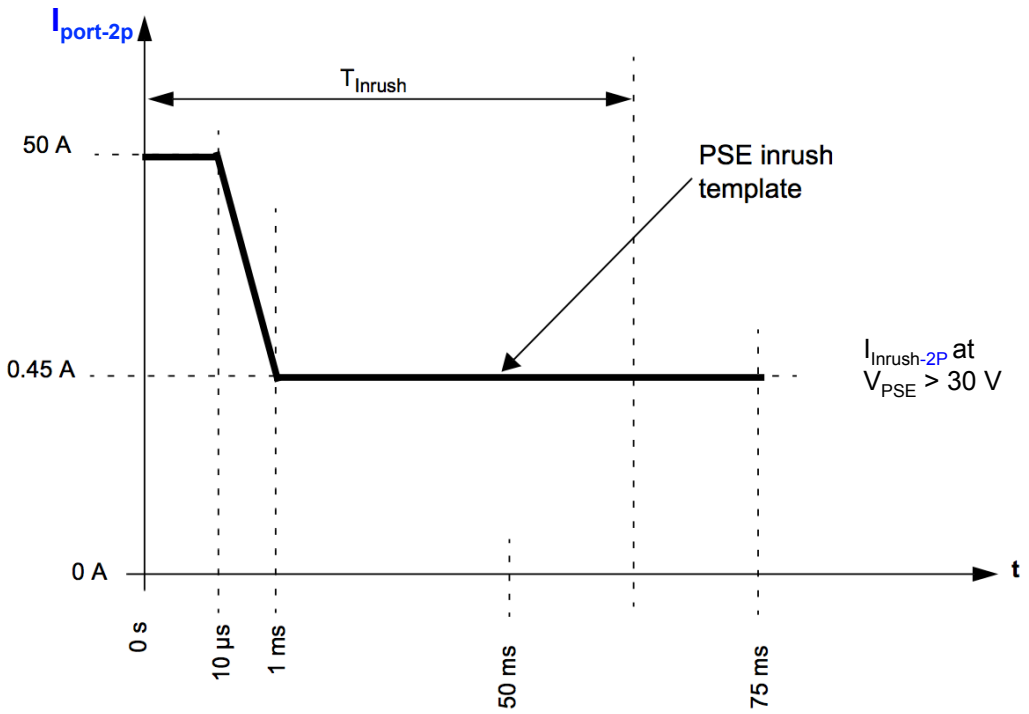


Figure 33-13 Inrush current and timing limits, per pair-set in POWER_UP state

Overload current Limit - Icut

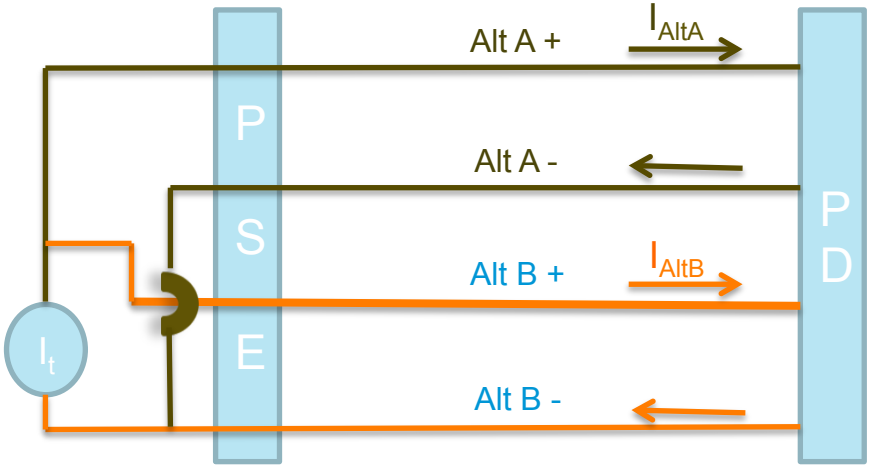
- Overload current limit per pair-set can be set based on the understanding that in a 4-pair system[1]

$$I_{two-pair} = \frac{I_t}{2} + \frac{I_t * E2E\_P2PRUNB}{2} = \frac{I_t * (1 + E2E\_P2PRUNB)}{2}$$

$$I_t = \frac{P_{class}}{V_{port\_PSE}} = I_{AltA} + I_{AltB}$$

$$I_{two-pair} = \frac{1}{2} * \frac{P_{class}}{V_{port\_PSE}} * (1 + E2E\_P2PRUNB)$$

where E2E_P2PRUNB is TBD



[1] - http://www.ieee802.org/3/bt/public/jul14/darshan_02_0714.pdf

Overload Current Limit - Proposal

- Modify Item 7 of Table 33-11 in IEEE 802.3 Std 2012 as follows
  - Changes shown in blue

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
7	Overload current per pair-set, detection range	$I_{CUT\text{-}2P}$	A	P_{class}/V_{Port_PSE} TBD	ILIM	1,2 **3,4**	Optional limit; see 33.2.7.6, Table 33–7.

  - P_{class} for Type 3 and Type 4 need to be added to Table 33-7

Short Circuit Current Limit

- Short Circuit current limit in IEEE802.3 Std 2012 is set based on cable current carrying capability

  -Short Circuit current limit for IEEE802.3bt can be set based on I_{cable} and using the same principles of overload current limit

- The lower limit is easy to define based on the above

Current Limit graph

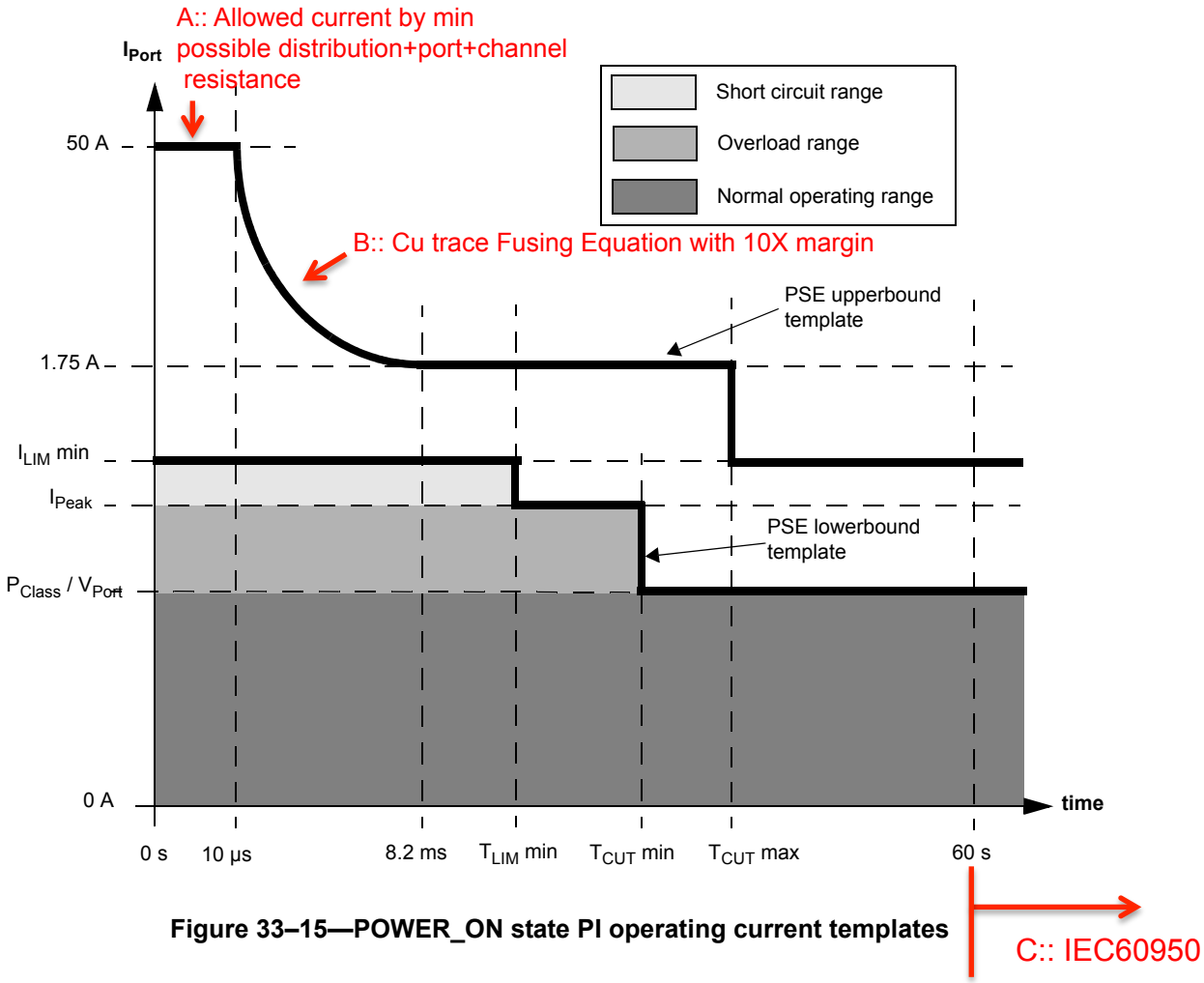


Figure 33–15—POWER_ON state PI operating current templates

Upper limit from IEEE802.3 Std 2012

Analyzing Existing Upper limit of IEEE 802.3 Std 2012:

Portion A: The static 50A is only for short period. Assumes current limited by distribution, channel, port resistance only.

- Derived using extremely low

$$R_{distribution}+R_{port}+R_{channel\ resistance} = 0.14Ohms^{(1)}$$

Portion B: Curve derived from Copper fusing equation

- Refer to Backup slide 22 for details
- Has at least inbuilt 10x margin
- Patch panel PCB X-section area used to arrive at this

Portion C:

- Needs to meet Safety limit IEC60950.
- Is at I_{lim} min << 1.75A (IEC60950 limit = 100VA/57V)

(1) - http://www.ieee802.org/3/at/public/2007/07/schindler_1_0719.pdf

Defining Upper Limit for Type 3

- The same IEEE 802.3 Std 2012 upper template can be adopted per pair-set for 4-pair Type 3 systems
  - This does not cause any additional stress based on understanding from slide 14
    - Portion A:
      - For very short period, doesn't affect anything in the system.
    - Portion B:
      - Patch panel X-section area considered during IEEE802.3at is per pair-set again, so the Cu fusing results per pair-set can stay the same as that of IEEE 802.3 Std 2012
    - Portion C:
      - For Type 3, Total I_{lim} min will still be less than 1.75A (IEC60950 limit)

Ilim Proposal for Type 3

- Modify item 9 of table 33-11 in IEEE 802.3 Std 2012 to say

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
9	Output current per pair-set – at short circuit condition	$I_{LIM\text{-}2P}$	A	0.400	See info	1	See 33.2.7.7. Max value defined by Figure 33–14.
				$1.14 \times I_{Cable}$		2,**3**	
				TBD	TBD	**4**	

Ilim Proposal for Type 3 - Contd

- Modify Figure 33-14 in IEEE 802.3 Std 2012 to

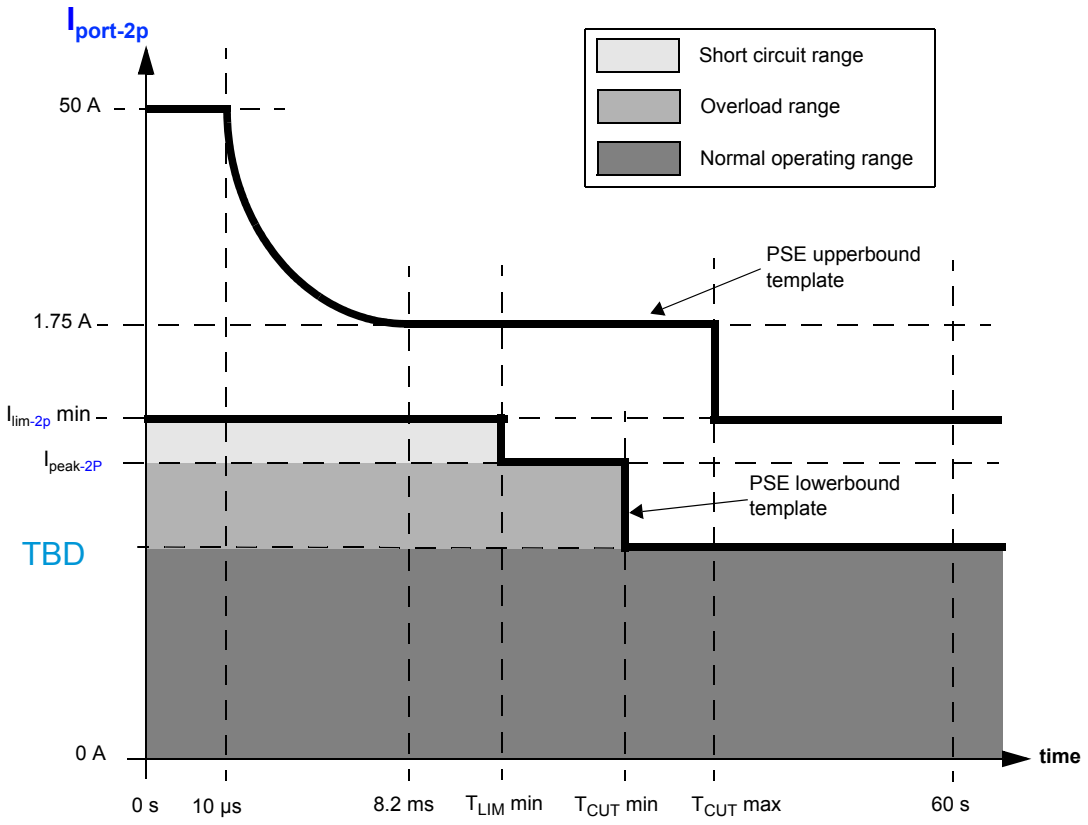


Figure 33-14-POWER_ON state, per pair-set operating current templates

Thank You

Backup

Inrush History

- http://www.ieee802.org/3/af/public/documents/Startup_mode_param_derivation.pdf

- Pavg = Irms * Vrms
- Irms = Ipeak/√2
- Vrms = Vpeak/√2
- Pavg = 0.5*Ipeak*Vpeak*Tinrush*N/Tperiod (assumes N port are turned on simultaneously)
- Energy = Tperiod * Pavg = 0.5*Ipeak*Vpeak*Tinrush*N
- The above energy dissipation should be limited by multiple different package choices → in turn defines inrush parameters
- IEEE802.3af work already considers,
  - Multi port turn on and multi-port chips with internal FETs
  - Due to the fact that in multi-port chip the Mosfets will be located around the package near the I/O pins, we can assume that the energy limit per port will be the same as the single port chip. Hence we can turn on simultaneously multi ports through startup mode.

Ilim upper template history

- http://www.ieee802.org/3/at/public/2007/07/schindler_1_0719.pdf
  - Fusing current defined by Onderdonk's equation
    - I = 0.188 * A/√t → the upper template linear part derived from this with at least 10X margin.
    - Patch panel PCB cross section was used -> 2 oz thick, 5mil wide