Making 1-Channel PSEs Work

Dave Dwelley

Linear Technology

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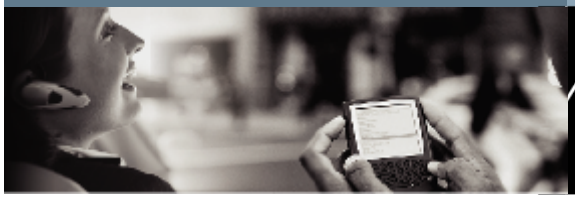
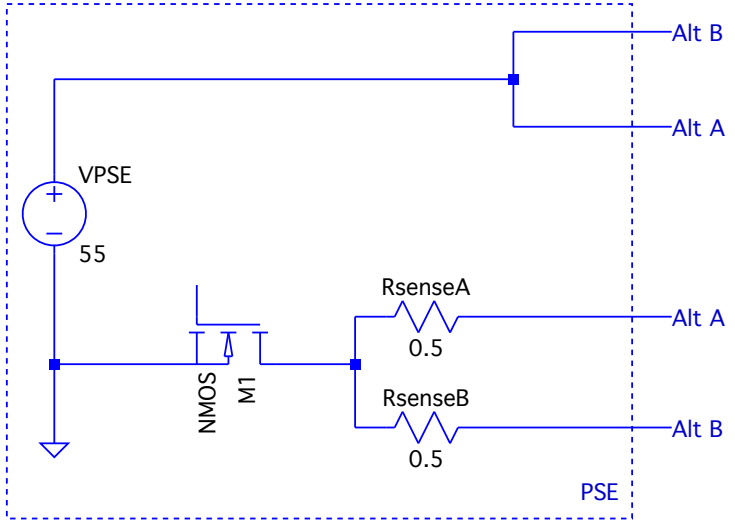


1-Channel PSEs Can't Do Two Things

- Cannot power only 2 pairs
  - But can measure each pair set independently
- Cannot run detection on only 2 pairs (sequential detection) or when any pair set is powered
  - But can measure current balance during parallel detection
  - Can also pollute one side during parallel detection to determine if there is one or two signature paths

Dual Sense Resistors

- Dual sense resistors allow detection, Icut/Ilim, and MPS sensing at each pair
  - Will protect either pair set in case of over-current
  - Will disconnect when one side of a powered Y-cable is opened after detection
  - Allows the detection circuitry to distinguish floating Y-cable signatures
- Any fault present: all 4 pairs off



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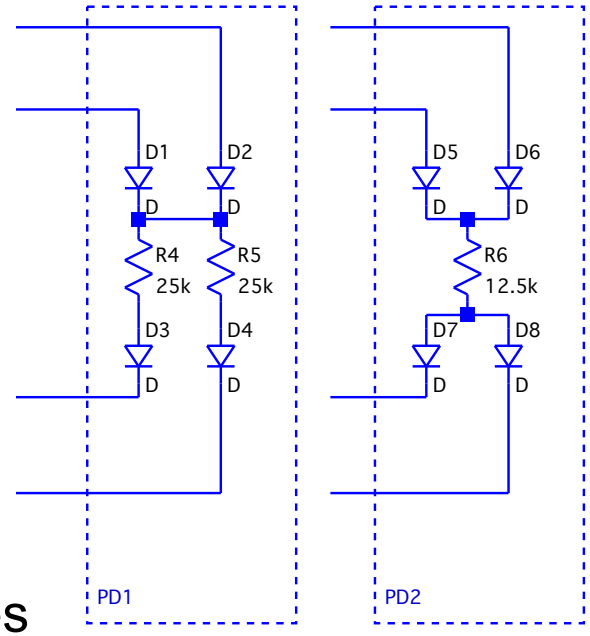
Powering Four Pairs

- All compliant PDs will tolerate 4-pair power
  - 33.3.1: “The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.”
  - This spec is flawed and should be corrected but the intent is clear
- Most Type 1/2 PDs will make use of 4-pair power
  - All AF/AT PDs using the “standard” diode-bridge single front end
  - Nearly all dual front-end PDs
  - In general, the PD controls its own power draw – voltage at additional PI pins will rarely cause unusual behavior
- Mandatory safeguards in the PSE will generally turn off the rare PD that fails to meet the above
  - Ilim/Icut on each pair set will catch Type 1/2 PDs >25.5W
  - MPS sensing on each pair set will remove power if one pair set fails to maintain MPS

Single vs. Dual Signature

- 1-ch PSE cannot detect one pair set at a time
  - Both pairs connected together at each end
  - Dual 25k signatures appear as 12.5k
- If the parallel signature is 12.5k, the PSE can pollute one side and try again
  - Switches shunt R across one pair set (Annex 2)
  - Dual-sig PD: other pair current doesn't change
  - Single-sig PD: other pair current increases
- Now the PSE knows enough to provide or deny power



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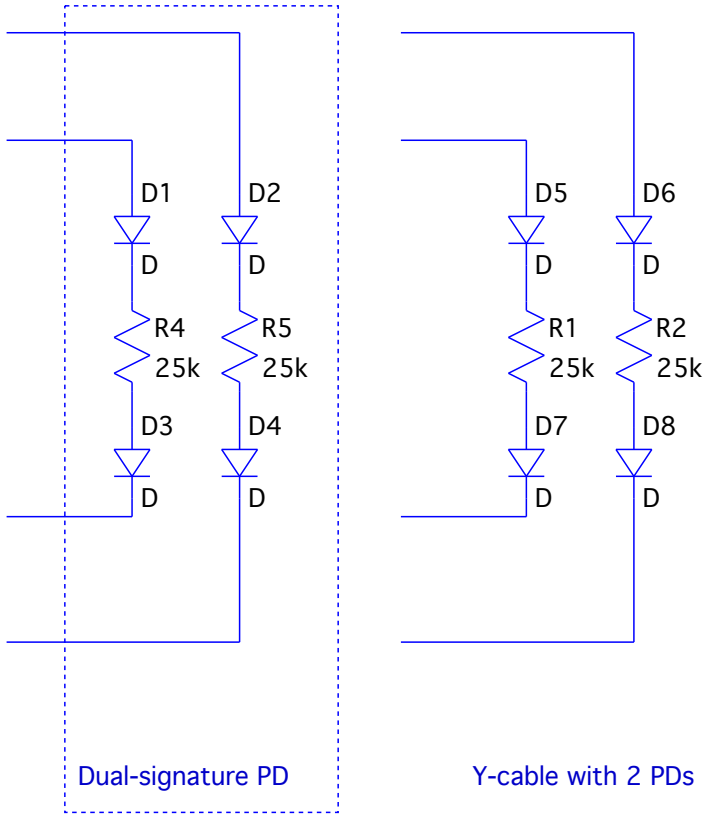
Y-Cable or Dual-Signature PD?

- Y-cable with 2 PDs attached appears the same as a dual-sig PD before power is applied
  - Signature disable loop functions only above Vport_min - cannot be checked without turning on one pair
- 4-pair power is OK for Type 1/2 PDs (per adhoc)
  - PSE behavior is the same for either case: all pairs on after detection, power off if Icut or MPS not met
- Bottom line: PSE doesn't need to know which case is connected during detect



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What's Left?

- X-cables
  - Detection/Classification algorithm will sense floating pairs at PSE PI and deny power
  - Neither X- nor Y-cables are standard link segment configurations – "deny power" is an appropriate response
- Y-cable to 2 PSEs with 50k "must reject" impedances
  - This is a rare and non-functional wiring fault
  - Most PSEs will fail a modern 4-point detection test
  - Nearly all PSEs tolerate 57V without problems
  - This case can be ignored, or screened with "pollution" test after 25k parallel detection result

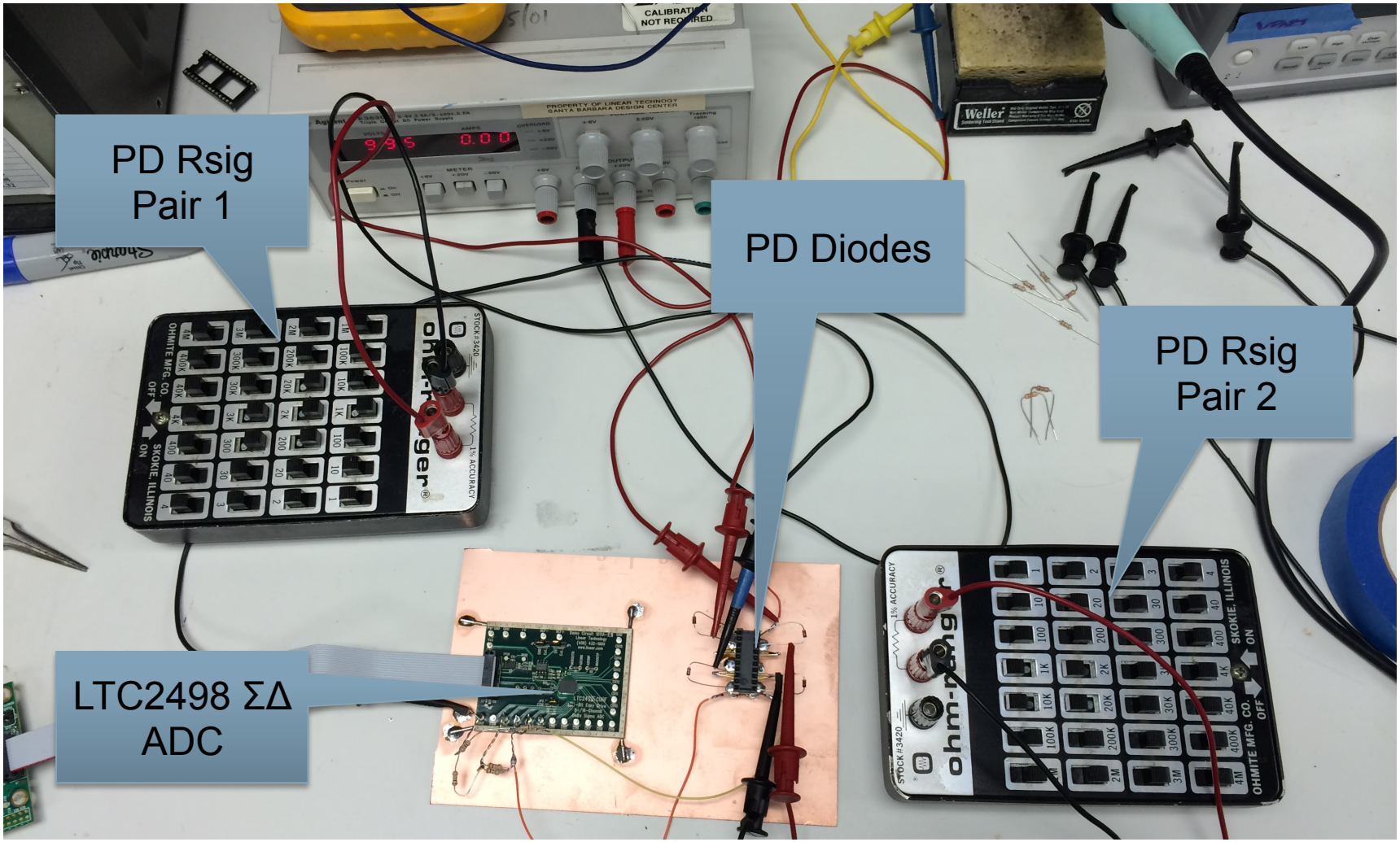
Skeleton Baseline Text

- The PSE shall detect a PD with a valid signature (per Table 33-5) at either or both pair sets, and shall reject an invalid signature (per Table 33-6) at either pair set.
- The PSE shall meet Ilim/Icut/MPS (per Table 33-11) for each pair set that provides power.
- A Type 3+ PSE shall be allowed to provide power over all 4 pairs to any compliant PD

Annex 1: Small Signals

- Detect currents are below 500uA for a valid 25k signature
- This current across a typical sense resistor creates a very small voltage (typically ~100µV)
- How do we do anything useful with such a tiny voltage?
- Can an integrating ADC measure a signal that small?

Test Setup



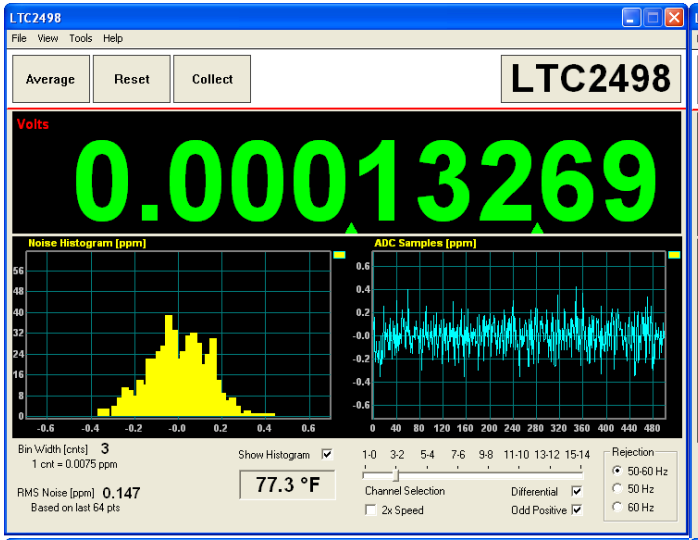
Results

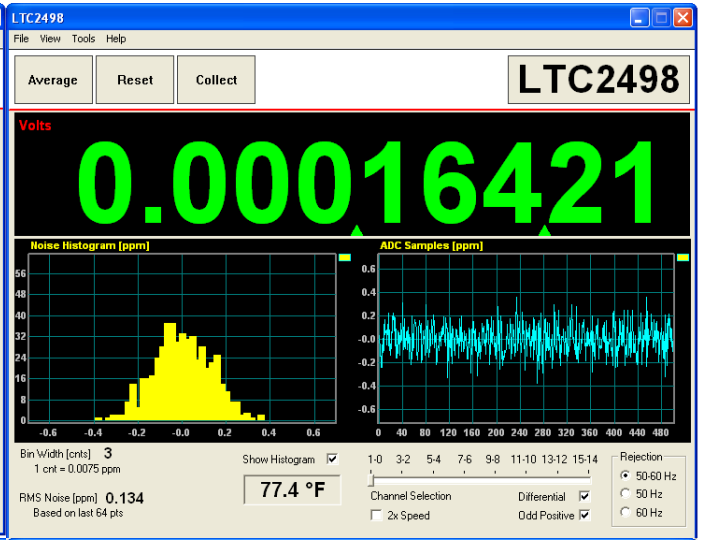
- Test voltage is 10V
- Source impedance (Rsense) is 0.5Ω
- ADC noise is ~3μV p-p in 150ms window
- ADC easily resolves must-accept and must-reject signature resistances:

		test voltage			theory	actual
		after diodes	test current	sense r	voltage across r	measured v
rsig nom	25000	8.6	344.0E-6	0.5	172.0E-6	
		8.6		0.5		
rsig min	23700	8.6	362.9E-6	0.5	181.4E-6	
rsig max	26300	8.6	327.0E-6	0.5	163.5E-6	
must accept min	19000	8.6	452.6E-6	0.5	226.3E-6	228.0E-6
must accept max	26500	8.6	324.5E-6	0.5	162.3E-6	164.0E-6
		8.6		0.5		
must reject min	15000	8.6	573.3E-6	0.5	286.7E-6	287.0E-6
must reject max	33000	8.6	260.6E-6	0.5	130.3E-6	132.0E-6

ADC Output

Must Reject (max)

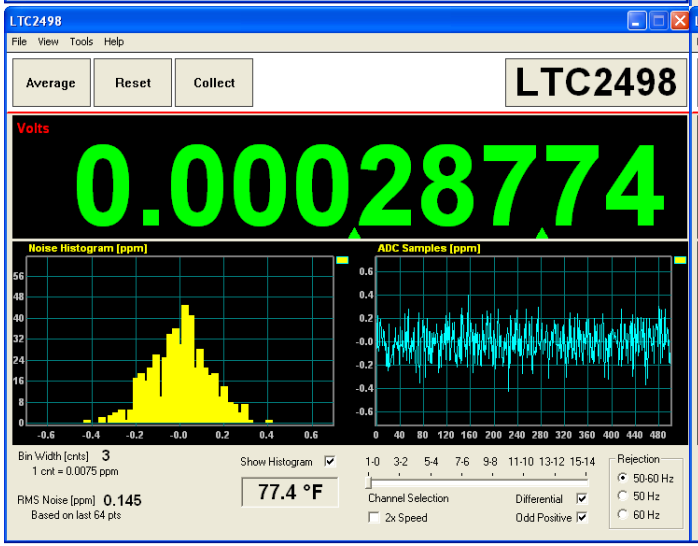


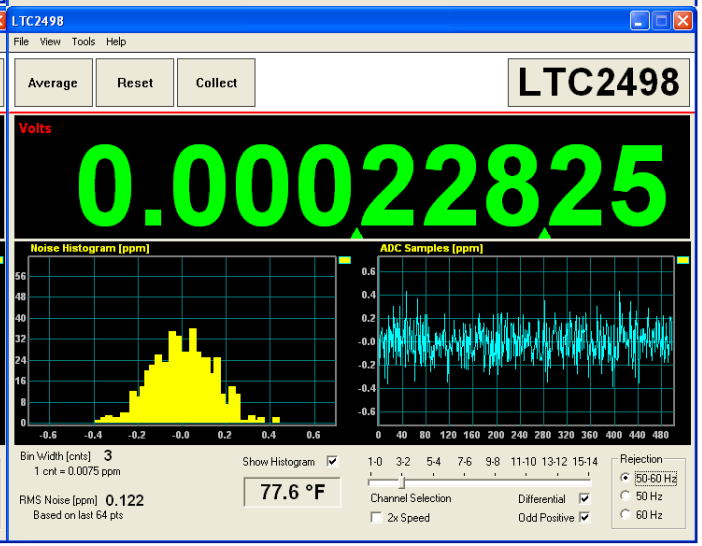


Must Accept (max)

1ppm = 5µV

Must Reject (min)





Must Accept (min)

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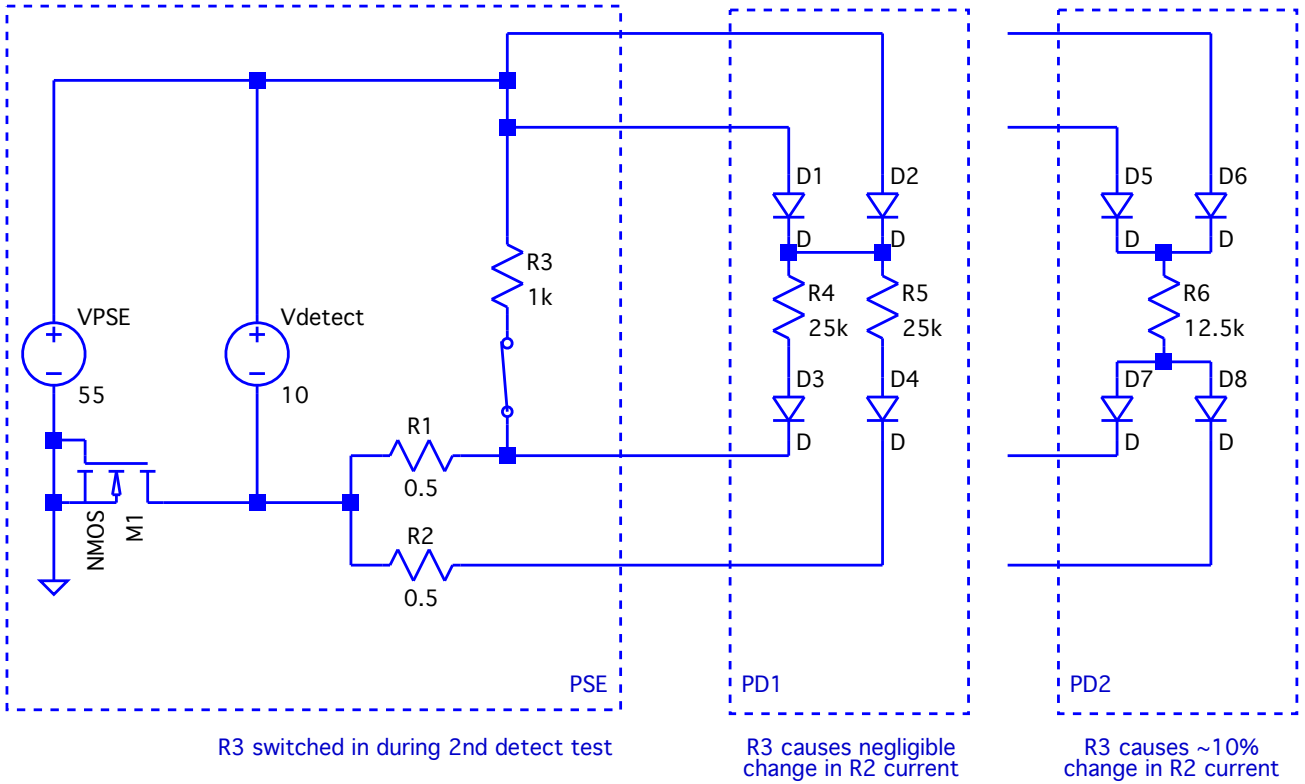
Annex 2: Signature Pollution Test



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Annex 3: P2P Unbalance Concerns

- In general, resistive P2P unbalance does not affect detection
  - Rsig >> Rlinkseg
- Voltage unbalance will affect 1ch PSE detection
  - Minor PD voltage imbalance due to diodes is tolerable since detect currents are small
  - Other sources of PD voltage imbalance will cause problems if present
  - PD signature voltage imbalance must be specified
  - PSE voltage imbalance must also be spec'd but 1ch PSEs should have intrinsically good voltage balance