Power Matters

Only PD affects PD POWERUP Tinrush max.

(Not the PSE Tinrush Timer..)

IEEE802.3bt

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Objectives

- PD spec: IEEE802.3bt D1.2, Clause 33.3.7.3 page 271 lines 39-43
  - To restore the PD Iinrush end time reference point from IEEE 802.3-2012 to IEEE802.3bt with the necessary changes made for 802.3bt.
  - This is what PD vendor needs for PD design to meet Iinrush timing
    - PD Iinrush end time reference point in D1.2 is different than IEEE 802.3-2012 and physically is incorrect although the time duration is correct.

- Separate discussion: To consider:
  - Satisfying with the existing text that already address the concerns OR
  - adding necessary text to address concerns raised during 802.3bt discussions that led to the changes in D1.2

Background - 1

- The following is a description of PD Inrush process in IEEE802.3-2012 Standard

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period **beginning with the application of input voltage at the PI** compliant with VPort_PD requirements as defined in Table 33–18, **and ending when CPort is charged to 99 % of its final value**. **This period should be less than TInrush min per Table 33–11.**

A concern was raised during the 802.3bt work that PD designers turn ON the load during the startup period and cause PD to fail startup.

- An attempt to resolve the concern was made in 802.3bt D1.2 and earlier drafts:

33.3.7.3 Input inrush current

Inrush current per pair set is drawn **beginning with the application of input voltage** at the pair set compliant with Vport_PD-2P requirements as defined in Table 33–18, and ending before TInrush-2P min per Table 33–11.

The objective of this presentation is to show that:

a) The concern was not resolved by the changes made to D1.2.

b) The concerns are already resolved by existing text already in the standard.

c) Incorrect description was used in the new text (marked in red) to define ending of the Inrush process although the requirement to end the process within 50msec is correct.

Background - 2

- The text that is already in the standard and resolve the the concern in **33.3.7.3.**

Type 2, Type 3 and Type 4 PDs with pse_power_leveltype state variable set to 2, 3 and 4 respectively prior to power-on shall behave like a Type 1 PD for at least Tdelay-2P min. Tdelay-2P for each pair set starts when VPD-2P crosses the PD power supply turn on voltage, VOn. This delay is required so that the Type 2, Type3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pair set from IInrush-2P to ILIM-2P.

The above is also covered by the PD state Machine. See Annex D for details.

The problems with the existing text in 802.3bt D1.2

- **33.3.7.3 Input inrush current**

Inrush current per pairset is drawn beginning with the application of input voltage at the pairset compliant with Vport_PD-2P requirements as defined in Table 33–18,

The Inrush process starting point is correct.

and ending before TInrush-2P min per Table 33–11.

X

The ending point is incorrect:
The ending point should depends on PD physics (getting to steady state by charging to 99% of Cport) and not on PSE Iinrush timer!
We do need to specify Tinrush_min as maximum time duration for Inrush process in separate row and not as the process end point!

This part should describe a process: the Inrush start and end time

After TInrush-2P min, the PD shall meet PClass_PD as specified in Table 33–18.

This part guarantees that PD meets Pclass only after Tinrush_min.

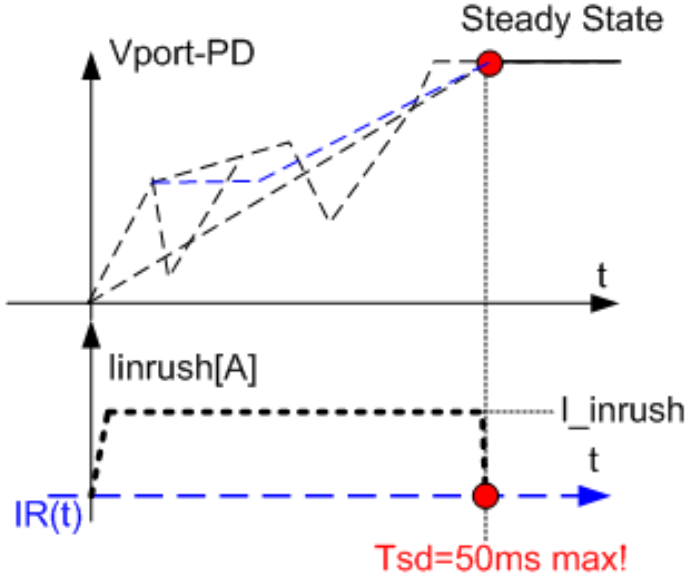
This part guarantees that PD will consume power for >Type 2 after Tdelay.

Type 2, Type 3 and Type 4 PDs with pse_power_level type state variable set to 2, 3 and 4 respectively prior to power-on shall behave like a Type 1 PD for at least Tdelay-2P min. Tdelay-2P for each pairset starts when VPD-2P crosses the PD power supply turn on voltage, VOn_PD. This delay is required so that the Type 2, Type3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from IInrush-2P to ILIM-2P.

This part already address the concerns.

Summary

- The part that is missing in D1.2 is:
  - The definition of the process starting and ending point **per the PD and only the PD physics which implies what to do.**
  - This is what PD vendor needs for PD design to meet Iinrush timing
  - It was clearly defined by IEEE802.3-2012 version
- The process has to end within 50msec



The proposed Remedy

- **33.3.7.3 Input inrush current**

Inrush current per pairset is drawn beginning with the application of input voltage at the pairset compliant with Vport_PD-2P requirements as defined in Table 33–18,

The Inrush process starting point is correct.

and ending when CPort has reached a steady state and is charged to 99 % of its final value.

This period should be ended before TInrush-2P min per Table 33–11.

Now the process is defined and PD Vendor knows that he needs to get to steady state=99% of Vpd with in 50msec!

This part should describe a process: the Inrush start and end time

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This part already address the concerns.

Proposed Remedy

- **Suggested Remedy (changes are in RED)**

Inrush current per pairset is drawn beginning with the application of input voltage at the pairset compliant with Vport_PD-2P requirements as defined in Table 33–18, and ending when CPort has reached a steady state and is charged to 99 % of its final value.

This period should be ended before TInrush-2P min per Table 33–11.

To consider to add the following note that do address any concerns and supply guide lines.

Note: For successful startup, a PSE supplying Iinrush-2P minimum value and a PD not drawing more than Type 1 maximum DC current results in stable voltage ramping across the PD input capacitor which is important for successful POWER UP. In addition, Cport value and PD load current may be time dependent. As a result PD implementers need to ensure that for any combinations of Cport and Type 1 maximum DC current during POWERUP, the PD inrush period is not exceed 50msec and higher PD load power should be used only after Tdelay.

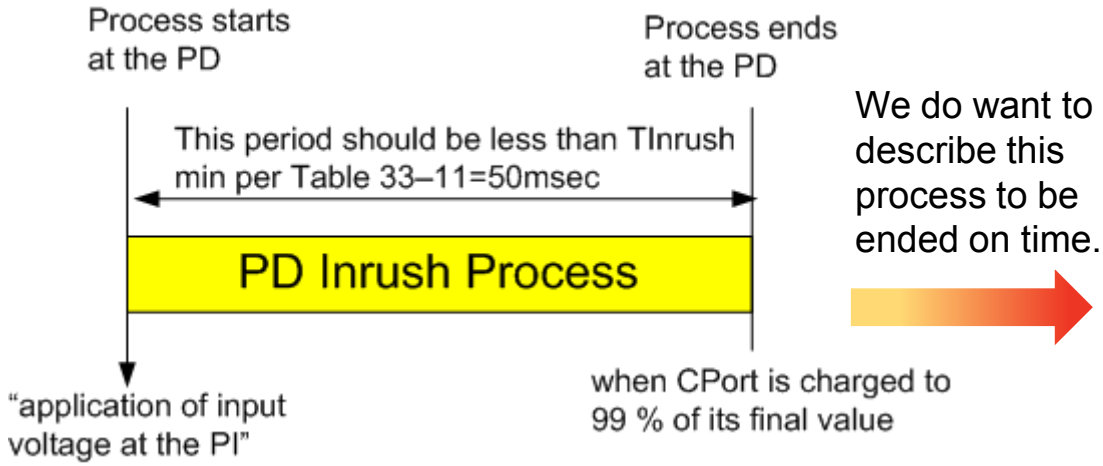
Thank You

Backup slides

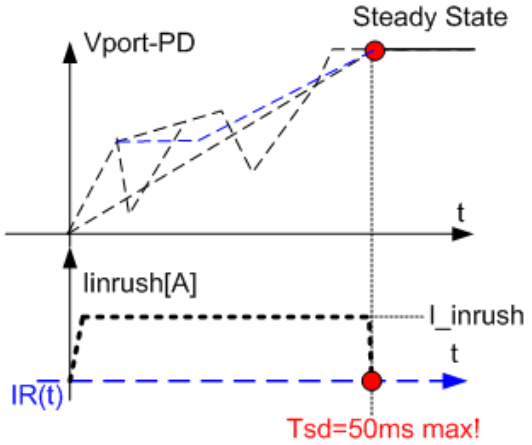
Background - IEEE 802.3-2012, 33.3.7.3

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with VPort_PD requirements as defined in Table 33–18, and ending when CPort is charged to 99 % of its final value. This period should be less than TInrush min per Table 33–11.



We do want to describe this process to be ended on time.



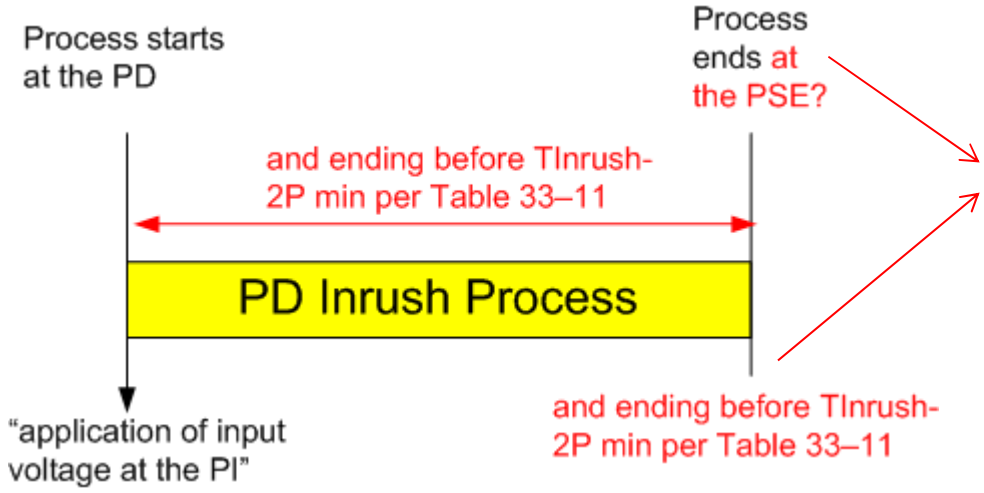
- The original description of the PD Iinrus process is physically correct. Clear starting and ending points.
  - 99% of final value is acceptable definition of STEADY STATE.
    - Other definition is e.g. across Cport, dv/dt ➔ ε=0.01 OR
    - Current through Cport di/dt ➔ ε=0.01 etc.
- It limits the process time duration to 50msec max. Time duration is not depends on PSE Tinrush Timer!
- Type 2 PD IS NOT ALLOWED to turn ON the load during POWERUP time. It has to waits 80msec. (See Table 33-18 Tdelay requirement and PD state machine in Annex D)

Background - IEEE 802.3bt D1.1

We change the old text in 802.3 due to a concern that some PDs turn on the load during POWER UP and fails to startup.

33.3.7.3 Input inrush current

Inrush current per pair set is drawn beginning with the application of input voltage at the pair set compliant with Vport_PD-2P requirements as defined in Table 33–18, and ending before TInrush-2P min per Table 33–11.



NO!
It ends at the PD and by the PD regardless of what happen in the PSE.
PSE has only to guarantee Iinrush_min for 50msec min.
See previous slide.

- The new text doesn't prevent PD user to violate the spec.
- PD has no access to PSE Tinrush timer…we are in the PD.
- PD Iinrush ends due to PD physics that must force PD inrush to end within 50msec.

Concerns raised during 802.3bt discussions.

#	Concern	Remedy
1	Can't charge Cport within 50msec at worst case conditions. Tinrush=C*V/Ich= 180uF*57/(0.4A-0.35A)=205.2msec>50ms.	Use lower Cport or lower load current or start your PWM with longer soft-start or design for Steady State at 36V<39V: 100uF*39V//(0.4A-0.25A)=46.7msec
2	PD Vendor look at PD input voltage and wait for 99% of voltage to get steady state and then turn ON load while PD really didn't get to Steady State….	PD Vendor need to design PD to finish Iinrush due to its internal implementation physics (Cport(t), ILOAD(t) soft start etc. **and not anything else**. We can do nothing with wrong implementations.
3	PD vendor turn ON load >350mA during POWER UP time and fails startup.	The spec requires not to do it. See 33.3.7.3 and state machine.
4	PSE looks at PD Vport voltage and check only DC Voltage and determined completion of PD Inrush based on it.	**PSE can't look at PD voltage.** He can look only on PSE PI voltage. PSE PI voltage is not identical to PD PI voltage at all times. In addition PSE requirements are covered by PSE legacy power-up variable. *It is not relevant for the PD start and end point process definition.*

Definition of Inrush Process

- Inrush Process
  - Iinrush is the current(t) or voltage(t) behavior when applying voltage to a CAPACITIVE load until it reaches to STEADY STATE
- Iinrush time
- It is the time starting with the application of voltage to the load until it reaches to steady state.

- Steady State is achieved when:
  - d(Vc) / dt ➔➔ ε=0.01 or other acceptable value OR
  - d(Ic) / dt ➔➔ ε=0.01 or other acceptable value OR

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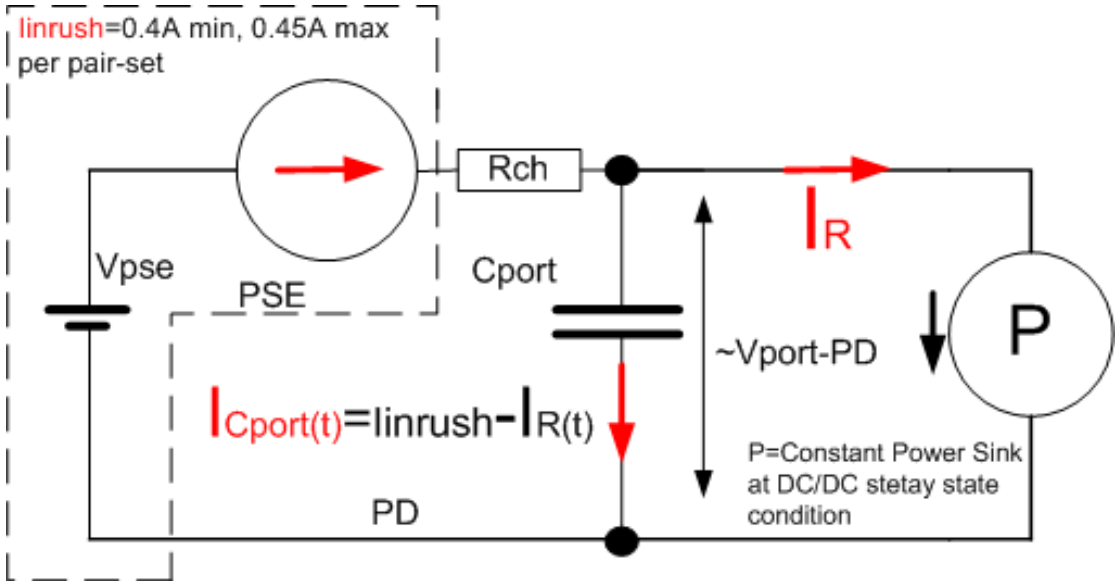
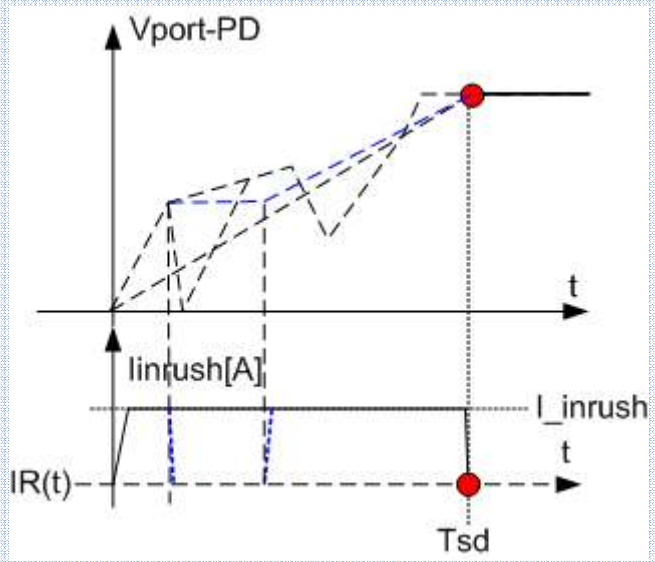
(Not the PSE Tinrush Timer..)



$$Vc = Vport = \int_0^{Tsd} \frac{(Iinrush - I_R(t))}{C(t)} \cdot dt$$



Vport-PD may vary due to primary and secondary start ups but eventually will reach to steady state (Tsd)!

$$Tinrush \cong \sum_{i=1}^{n} \frac{C_i \cdot \Delta V_{C_i}}{(Iinrush - I_{Ri})} \leq Tst = 50mSec$$

- PSE guarantees Iinrush_min over each pair set for 50ms min.
- PD has to finish PD inrush process within 50msec max
  (50msec ≤ Tinrush_min in Table 33-11 to guarantee Inrush_min support from PSE).

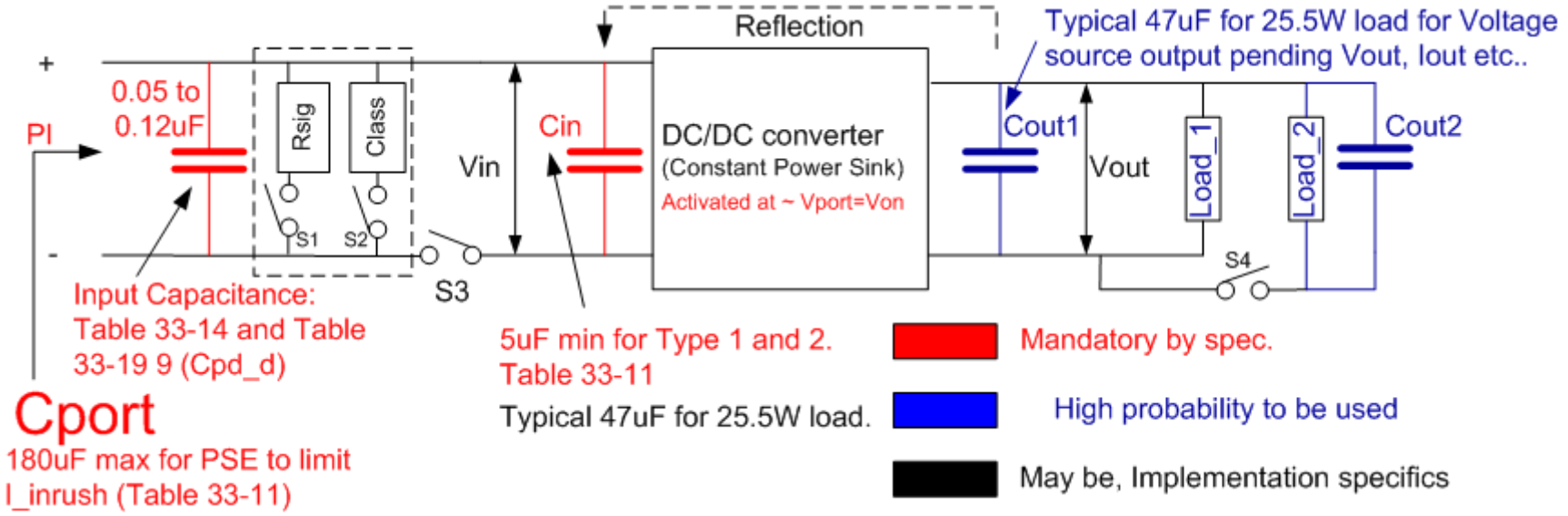
  Regardless of:
  - $I_{R(t)}$ value (350mA max) during Iinrush period
  - Cport(t) profile.
    - ***$I_R(t)$ and Cport(t) are time depended. When PWM starts operation, secondary capacitive loads WHEN connected the DC/DC output are reflected to the PD input.***

Main concern: How we prevent users to consume power during POWERUP?

- The facts are:
  - Users can consume up to 350mA for all PD types. They can not consume more than Type 1 current during POWERUP. This is clearly covered by the spec.
  - For Type 2 and up, PD needs to wait 80msec until consuming current above 350mA per PD Pclass.
  - The changes in D1.1 WILL NOT prevent PD designs to violate the spec due the fact that it addresses the wrong root cause of the question above.
    - The above question can be asked for any spec parameter i.e. how we prevent the user not to meet the standard..?

- We can prevent users to consume power during POWERUP by clear spec. and clear guidelines e.g.:
  - To add the following note:
    - Note: For successful startup, a PSE supplying Iinrush-2P minimum value and a PD not drawing more than Type 1 maximum DC current results in stable voltage ramping across the PD input capacitor which is important for successful POWER UP. In addition, Cport value and PD load current may be time dependent. As a result PD implementers need to ensure that for any combinations of Cport and Type 1 maximum DC current during POWERUP, the PD inrush period should not exceed 50msec and higher PD load power should be used only after Tdelay.

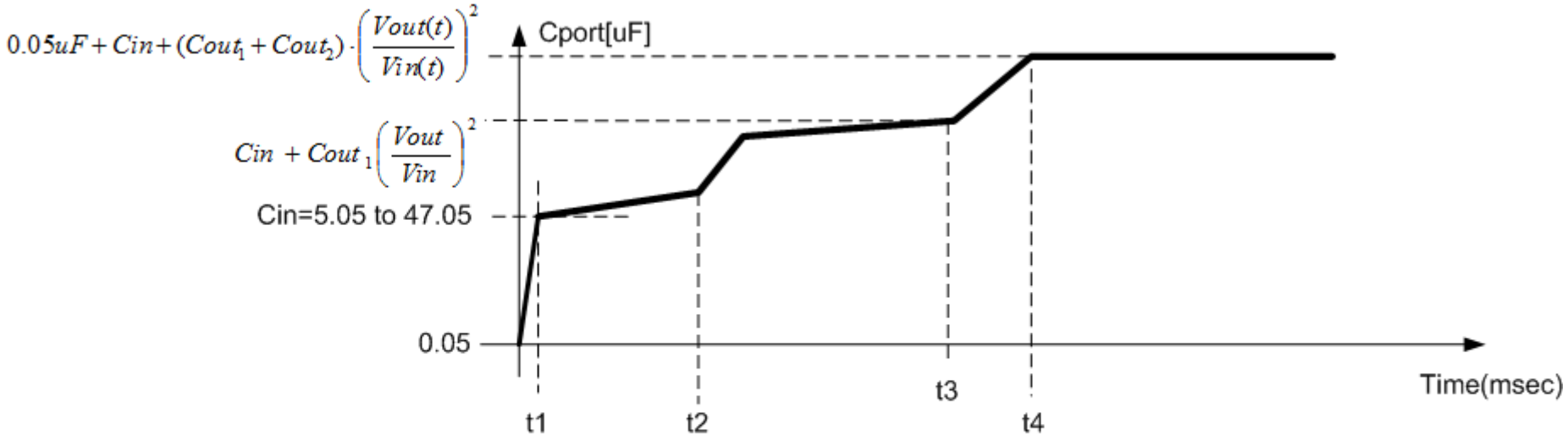
Annex A: PD Typical Block Diagram



- There is mandatory minimum capacitance for a compliant PD (=5.05uF).
- When PSE is tested for compliance, it must contain minimum capacitance requirement.
- Cport is defined for the sum of all capacitive components at PD input AND all the reflected PD DC/DC output capacitors (Cout1, Cout2 etc.)
- Type 2 maximum TOTAL equivalent Input capacitance that PSE has to support with Iinrush_min is 180uF. It includes Cin+Cpd_d+ Reflected Cout1 etc.

Annex B: PD Cport possible variations during POWERUP time duration

$$Cport(t) \cong 0.05uF + Cin + u(t-\tau 1)\cdot Cout_1\left(\frac{Vout(t)}{Vin(t)}\right)^2 + u(t-\tau 2)\cdot Cout_2\left(\frac{Vout(t)}{Vin(t)}\right)^2 .....$$



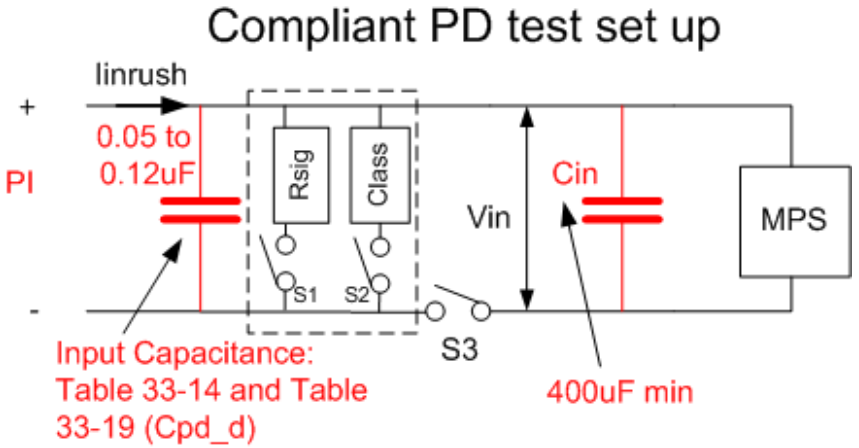
Behavioral qualitative description of PD input capacitance over time.

Notes:
1. t1,t2,t3 and t4 are implementation specifics.
2. Slopes of capacitance change is function of DC/DC transfer function and soft start.

- Regardless of actual Cport profile (implementation specifics), PD must get to steady state (Vport-PD dv/dt ➔ε, practical ε ≅ 0.01) within 50msec.
- Only PD physics affect the completion of PD Inrush.
- PSE Tinrush timer has no effect on the completion of PD inrush time.

Annex C: compliant PD test setup for testing PSE POWERUP Iinrush and Tinrush requirements

- PSE has to supply startup energy for the worst case conditions.
- The PD test setup will contain big capacitor at its input so Inrush can be monitored for at least 50msec.
- Worst case STARTUP energy is given by:
- 0.5*Vpse_max*Iinrush_max*Tinrush_min=0.5*C*Vpse_max^2. Resulting with Iinrush_max*Tinrush_min=C*Vpse_max
- Cin_min in the test setup is: Iinrush_max*Tinrush_min/Vpse_max=0.45*0.05/57=394uF.
- Use 400uF min and measure Iport that is within Iinrush_min/max range for at least 50ms.



- Advantages:
- Implementation independent if PSE uses Tinrush timer or legacy POWERUP to determine PD ended Iinrush process.
  - Simple proof that PSE delivers Iinrush_min for at least 50msec.
- Real compliant PD with capacitive load.
- Uses only the correct stress on PSE circuitry compared to uncompliant PD test setups that is using constant current source of >450mA which represent short circuit condition (twice the energy) and not POWERUP which is half the energy as calculated above.
- The above is for each pair set. As a result, Type 1, 2, 3 and 4 can be tested with 400uF min at each pair set of the PD test setup.

Annex D

- PD is not allowed to turn ON power above Type 1 current before Tdelay time is done.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
6	Inrush to operating state delay per pair set	$T_{delay-2P}$	s	0.080		2, 3, 4	See 33.3.7.3

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer
A timer used to prevent the Type 2 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.