Editor's Note: Editor to consult with staff on duplication of definitions. Waiting for response from staff - note will be removed once response is received.

Change title and text of 33.1.4 as follows:

33.1.4 ~~Type 1 and Type 2~~ System parameters

A power system consists ~~consisting~~ of a single PSE, ~~link segment, and~~ a single PD, and the link section connecting them. ~~defined~~ The power system is defined by the lowest type of PSE or PD in a system ~~as either Type 1, or Type 2~~ and has certain basic parameters defined according to Table 33–1. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 33.2 and 33.3.

Replace Table 33-1 as follows:

Table 33–1—System power parameters Vs system Type

System Type (Lowest type of PSE and PD)	Nominal Highest Current per pair (I_{Cable}, A)	Channel pairset maximum DC loop resistance (R_{ch}, Ω)	Minimum Cabling Type[1]
Type 1	0.350	20.0	twisted-pair cabling per 14.4 and 14.5 (Class D recommended)
Type 2	0.600	12.5	Class D (ISO/IEC 11801:1995)
Type 3	0.600[2]	12.5	Class D (ISO/IEC 11801:2002)
Type 4[3]	0.960[2]	12.5	Class D (ISO/IEC 11801:2002)

[1]See sections 33.1.4.1 and 33.1.4.2.
[2]In Type 3 and Type 4 operation, the current per pairset will be impacted by pair-to-pair system resistance unbalance. See section 33.2.7.4.1a. (fix reference when finalized)
[3]For additional information, see TIA TSB-184-A.

Editor's Note: Type 3 and Type 4 current for extended power are presently under study in this draft. These numbers should converge to I_{con-2P} in Table 33-11.

Liason underway with TIA and others to study the effect of unbalance on temperature rise. Liason links can be found at http://www.ieee802.org/3/bt/public/mar15/Liaisons.pdf

I_{Cable} is the current on one twisted pair in the multi-twisted pair cable. For Type 1 and Type 2 systems, two twisted pairs are required to source I_{Cable}—one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI. All four twisted pairs, connected from PSE PI to PD PI are required to source greater than class 4 power at the PSE PI - two pairsets each having one twisted pair carrying (+ I_{Cable}) and one twisted pair carrying (– I_{Cable}), from the perspective of the PI.

It should be noted that the cable references use "DC loop resistance," which refers to a single conductor. This clause uses "DC pair loop resistance," which refers to a pair of conductors in parallel. Therefore, R_{Ch} is related to, but not equivalent to, the "DC loop resistance" called out in the cable references.

Change variable class_num_events as follows:

class_num_events

A variable indicating the maximum number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values:0: PSE does not perform Physical Layer classification.

1: PSE performs 1-Event Physical Layer classification.

2: PSE performs ~~2~~Multiple-Event Physical Layer classification with a maximum of 2 class events.

4: PSE performs Multiple-Event Physical Layer classification with a maximum of 4 class events.

5: PSE performs Multiple-Event Physical Layer classification with a maximum of 5 class events.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10.

Values:FALSE:No fault indication.

TRUE:A fault indication exists.

Change variables I_{Inrush} and I_{Port} as follows:

$I_{Inrush\text{-}2P}$

Output current per pairset during POWER_UP (see Table 33–11 and Figure 33–13).

$I_{Port\text{-}2P}$

Output current (see 33.2.7.6).

Editor's Note: Change I_{Port} to $I_{Port\text{-}2P}$ in state diagram as well.

Change variable legacy_powerup as follows:

legacy_powerup

This variable is provided for PSEs that monitor the ~~PI~~ per pairset voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the ~~PI~~ pairset voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed T_{Inrush} period is recommended. A variable that is set in an implementation-dependent manner.

Values:TRUE:The PSE supports legacy power up; this value is not recommended.

FALSE:The PSE does not support legacy power up. Type 3 and Tyep 4 PSEs shall use this value. It is highly recommended that new equipment use this value.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values:FALSE:If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.

TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

Change variable mr_pse_alternative as follows:

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values:A: The PSE uses PSE pinout Alternative A.

B: The PSE uses PSE pinout Alternative B.

BOTH: The PSE uses both Alternative A and Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values:disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.

enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.

force_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:FALSE:Do not perform detection during ted_timer interval.

TRUE:Perform detection during ted_timer interval.

Change variable option_vport_lim as follows:

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values:FALSE:V_{PSE} is within the V_{PSE} operating range as defined in Table 33–11.

TRUE:V_{PSE} is outside of the V_{PSE} operating range on at least one pairset as defined in Table 33–11.

Change the parameter ovld_detected as follows:

ovld_detected

A variable indicating if the PSE output current over at least one pairset has been in an overload condition (see 33.2.7.6) for at least T_{CUT} of a one second sliding time.

Values:FALSE:The PSE has not detected an overload condition.

TRUE:The PSE has detected an overload condition on at least one pairset.

Change the variable pd_dll_power_type as follows:

pd_dll_power_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the type of PD as advertised through Data Link Layer classification.

Values:1: PD is a Type 1 PD (default)

2: PD is a Type 2 PD

3: PD is a Type 3 PD

4: PD is a Type 4 PD

33.2.4.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

Change the timer tcle1_timer as follows:

tcle1_timer
: A timer used to limit the first classification event time in ~~2~~Multiple-Event classification for Type 1 and Type 2 PSE; see T_{CLE1} in Table 33–10.

Change the timer tcle2_timer as follows:

tcle2_timer
: A timer used to limit the second classification event time in ~~2~~Multiple-Event classification; see T_{CLE2} in Table 33–10.

Insert two new timers tcle3_timer and tlcf_timer after tcle2_timer as follows:

tcle3_timer
: A timer used to limit the third through fifth classification event time in Multiple-Event classification; see T_{CLE3} in Table 33–10.

tlcf_timer
: A timer used to limit the first classification event time in Multiple-Event classification for Type 3 and Type 4 PSEs; see T_{LCF} in Table 33–10.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

Change timer tinrush_timer as follows:

tinrush_timer
: A timer used to monitor the duration of the inrush event on a single pairset; see T_{Inrush} in Table 33–11.

Change timers tme1_timer and tme2_timer as follows:

tme1_timer
: A timer used to limit mark event times for all but the last ~~the first~~ mark event ~~time in~~ during ~~2~~Multiple-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
: A timer used to limit the ~~second~~ final mark event time in ~~2~~Multiple-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

Editor's Note: "Mutual identification not complete" in above paragraph needs to be clear. Team to pay close attention to above paragraph during reviews.

When a ~~Type 2~~ PSE powers a ~~Type 1~~ PD of lower Type ($Type_{PD}$) than its own native type ($Type_{PSE}$), the PSE shall meet the PI electrical requirements of a ~~Type 1 PSE the PD Type~~ ($Type_{PD}$), ~~but may choose to meet the electrical requirements of a Type 2 PSE~~ except for I_{Cut}, I_{LIM}, T_{LIM}, and P_{Type} (see Table 33–11), for which the PSE shall select to meet the requirements of its Type or a less Type such that, $Type_{PD} \leq$ PSE Type $\leq Type_{PSE}$.

Editor's Note: This above paragraph needs further study.

33.2.4.7 State diagrams

Insert new section 33.2.5.6 after section 33.2.5.5 as follows:

33.2.5.6 4PID requirements

Type 3 and Type 4 PSEs shall determine whether an attached PD with classes 0 to 4 is a candidate to receive power on both pairsets prior to applying power to the second pairset. This determination is referred to as 4PID. 4PID shall be initially (TBD) determined as a logical function of the detection state of both pairsets, the result of connection check as described in 33.2.5.0, mutual identification, and the results of other system information. It shall be stored in the variable pd_4pair_candidate, defined in 33.2.4.4.

33.2.6 PSE classification of PDs and mutual identification

Change text of Section 33.2.6 as follows:

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2, Type 3 or Type 4 PD to differentiate between Type 1, ~~PSEs from~~ Type 2, Type 3 and Type 4 PSEs. Additionally, mutual identification allows Type 2, Type 3 or Type 4 PSEs to differentiate between Type 1, ~~and~~ Type 2, Type 3 and Type 4 single-signature PDs (abbreviated Type 3/SS and Type 4/SS respectively) and Type 3 and Type 4 dual-signature PDs (abbreviated Type 3/DS and Type 4/DS respectively). PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer (DLL) classification ~~(DLL)~~.

Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto ~~the PI~~ a pairset and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and ~~2~~Multiple-Event Physical Layer classification (see 33.2.6.2).

The PSE shall provide V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10 only for a pairset with a valid detection signature. Polarity shall be the same as defined for V_{PSE} in 33.2.3 and timing specifications shall be as defined in Table 33–10.

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use V_{PSE} = V_{PSE} min and R_{Chan} = R_{Ch} max ~~when~~ powerin g using a single pairset, or R_{Chan} = R_{Ch}/2 when powering using two pairsets and to ~~arri~~ve at over-margine d values as shown in Table 33–7.

If the PD connected to the PSE performs Autoclass (see 33.3.5.3 and Annex 33B), the PSE may set its minimum power output based on the power drawn during Autoclass, increased by at least the margin associated with the PD class as listed in Table 33–10a, in order to account for potential increase in channel resistance due to temperature increase, with a maximum value defined in Table 33–7 of the corresponding PD class and a minimum of 4.0 Watts. PSEs that have additional information about the actual channel DC resistance may choose to use a lower Autoclass margin than those listed in Table 33–10a.

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_W \qquad (33–3)$$

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state.

When a dual-signature PD is detected, the PSE shall supply at least the requested power over a pairset per the class code detected over that pairset.

Editor's Note: Measurement method and PSE margin for Autoclass still need to be addressed.

33.2.6.1 PSE 1-Event Physical Layer classification

Change text of Section 33.2.6.1 as follows:

When 1-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event—1-EVENT_CLASS—as defined in the state diagram in Figure 33–9.

~~The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10. Polarity shall be the same as defined for $V_{Port\_PSE\_2P}$ in 33.2.3 and timing specifications shall be as defined by T_{pdc} in Table 33–10.~~

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current according to Table 33–9. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state.

Change title and text of Section 33.2.6.2 as follows:

33.2.6.2 PSE ~~2~~Multiple-Event Physical Layer classification

When ~~2~~Multiple-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1 or CLASS_EV1_LCF, MARK_EV1, CLASS_EV2, ~~and~~ MARK_EV2, CLASS_EV3, MARK_EV3, CLASS_EV4, MARK_EV4, CLASS_EV5 and MARK_EV_LAST—as defined in the state diagram in Figure 33–9.

Type 2 PSEs shall provide a maximum of 2 class and 2 mark events. Type 3 PSEs shall provide a maximum of 4 class and 4 mark events. Type 4 PSEs shall provide a maximum of 5 class and 5 mark events.

~~The~~ A PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10. ~~The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.~~

A PSE in the state CLASS_EV1_LCF shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{LCF} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9 between 6 ms and 75 ms after transitioning into the state CLASS_EV1_LCF. The PSE may continue to monitor the current past 75 ms. If the PSE did not measure I_{Class} in the range of Class 0 before T_{ACS} min and the PSE measures I_{Class} in the range of Class 0 after T_{ACS} max this indicates the PD will perform Autoclass. (see 33.3.5.3).

When the PSE is in the state MARK_EV1, MARK_EV2, MARK_EV3, or MARK_EV4 the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. ~~The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.~~

~~When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.~~

When the PSE is in the state CLASS_EV3, CLASS_EV4, or CLASS_EV5 the PSE shall provide to the PI V_{Class}, subject to the T_{CLE3} timing specification, as defined in Table 33–10.

In states CLASS_EV1, CLASS_EV2, and CLASS_EV3, the PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV_LAST, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10 The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1, ~~and~~ MARK_EV2, MARK_EV3, MARK_EV4 and MARK_EV_LAST commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

PSEs that implement CLASS_EV1_LCF, when connected to single-signature PDs, shall transition directly from CLASS_EV1_LCF to MARK_EV_LAST if they implement only one class event.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2, Type 3 or Type 4 PSE shall return to the IDLE state. The PSE shall limit class event currents to ~~s shall meet the~~ I_{Class_LIM} ~~current limitation. The~~ and shall limit mark event currents to ~~s shall meet the~~ I_{Mark_LIM} ~~current limitation~~. All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{PSE} in 33.2.3.

The PSE shall complete 2M~~u~~ltiple-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, ~~the~~ a Type 2 PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, ~~the~~ a Type 2 PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event. If the result of the first class event is any of Classes 0, 1, 2, or 3, a Type 3 or Type 4 PSE treats a single-signature PD as a Type 1 PD and shall omit the subsequent mark and class events and classify the PD according to the result of the first class event. If the class signature detected during

Editor's Note: All other instances of the above statement to be removed from draft. If commentators find any please comment against them.

Change Table 33-11 as follows:

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage per pairset in the POWER_ON state	V_{PSE}	V	44.0	57.0	1	See 33.2.7.1.
				50.0	57.0	2, 3	
				52.0	57.0	4	
1a	Output Voltage pair-to-pair difference of pairs with the same polarity in the POWER_ON state	V_{PSE_DIFF}	mV		2	3, 4	Open Load Voltage. Test Setup TBD.
2	Voltage transient below V_{PSE} min	K_{Tran_lo}	%		7.6	2, 3, 4	See 33.2.7.2.
3	Power feeding ripple and noise:						
	f < 500 Hz		V_{pp}		0.500	~~1, 2~~ All	See 33.2.7.3.
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
4	Continuous output current capability in POWER_ON state over both pairsets	I_{Con}	A	P_{Class} / V_{PSE}		1, 2, 3, 4	See 33.2.7.4.
4a	Pairset current due to E2ERunb within E2ERunb range for class 5	I_{Con-2P}	A	TBD		3	See 33.2.7.4a
	Pairset current due to E2ERunb within E2ERunb range for class 6			0.668		3	
	Pairset current due to E2ERunb within E2ERunb range for class 7			TBD		4	
	Pairset current due to E2ERunb within E2ERunb range class 8			0.931		4	

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
5	Output current in POWER_UP state	I_{Inrush}	A	0.400	See info	1, 2, 3, 4	For Type 1 and Type 2 PDs. See 33.2.7.5. Max value defined by Figure 33–13.
5a	Output current per pairset in POWER_UP state	$I_{Inrush-2P}$	A	0.400	See info	3, 4	For Type 3 and Type 4 PDs. See 33.2.7.5. Max value defined by Figure 33–13.
6	Inrush time per pairset	T_{Inrush}	s	0.050	0.075	~~1, 2~~ All	See 33.2.7.5
7	Overload current per pairset, detection range	I_{CUT}	A	P_{Class} / V_{PSE}	I_{LIM}	1,2	Optional limit; see 33.2.7.6, Table 33–7. K_I_{cut3} = 0.556 K_I_{cut4} = 0.538
				$K\_I_{cut3} \times P_{Class} / V_{PSE}$		3	
				$K\_I_{cut4} \times P_{Class} / V_{PSE}$		4	
8	Overload time limit per pairset	T_{CUT}	s	0.050	0.075	~~1, 2~~ All	See 33.2.7.7.
9	Output current per pairset – at short circuit condition	I_{LIM}	A	0.400	See info	1	For class 0-3. See 33.2.7.7. Max value defined by Figure 33–14.
				1.14 × I_{Cable}		2	For class 4. See 33.2.7.7. Max value defined by Figure 33–14.
				TBD		3	For class 5. See 33.2.7.7. Max value defined by Figure 33–14.
				0.817		3	For class 6. See 33.2.7.7. Max value defined by Figure 33–14.
				TBD		4	For class 7. See 33.2.7.7. Max value defined by Figure 33–14.
				1.162		4	For class 8. See 33.2.7.7. Max value defined by Figure 33–14.
10	Short circuit time limit per pairset	T_{LIM}	s	0.050	See info	1	See 33.2.7.1 and 33.2.7.7.
				0.010		2, 3	
				0.006		4	
11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		~~1, 2~~ All	See 33.2.7.10, Table 33–7.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
12	PSE Type power ~~minimum~~	P_{Type}	W	I_{Cable} × (V_{PSE}-min)		1, 2	See 33.1.4, 33.2.7.11a
				I_{Cable} × (V_{PSE} min)		3[1]	
				2 x I_{Cable} × (V_{PSE}-min)		3	
				90	99.9	4	
13	Power turn on time	T_{pon}	s		0.400	1, 2, 3, 4	See 33.2.7.12.
14	Turn on rise time	T_{Rise}	µs	15.0		~~1, 2~~ All	From 10 % to 90 % of the voltage difference at the PI in POWER_ON state from the beginning of POWER_UP.
15	Turn off time	T_{Off}	s		0.500	~~1, 2~~ All	See 33.2.7.8.
16	Turn off voltage per pairset	V_{Off}	V		2.80	~~1, 2~~ All	See 33.2.7.9.
17	DC MPS current when measured over a pairset connected to a single-signature PD[2]	I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
				0.002	0.005	3, 4	Applies to P_{Class} ≤ class 4 power. Applies to highest current pair. See 33.2.9.1.2.
				0.002	0.007	3, 4	Applies to P_{Class} ≥ class 5 power. Applies to highest current pair. See 33.2.9.1.2.
17a	DC MPS current when measured over a pairset connected to a dual-signature PD[3]			0.002	0.007	3, 4	MPS need to be detected over each pairset. See 33.2.9.1.2.
17b	DC MPS current when total sum of both pairs with the same polarity is measured, connected to a single-signature PD[3]			0.004	0.009	3, 4	P_{Class} ≤ class 4 power. See 33.2.9.1.2.
				0.004	0.014		P_{Class} ≥ class 5 power. See 33.2.9.1.2.
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
				0.320		3, 4	
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.060		1, 2	See 33.2.9.
				0.006		3, 4	

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
20	Intra-pair ~~C~~current unbalance	I_{unb}	A		3 % × I_{Cable}	1	See 33.2.7.11, 33.4.8. NOTE—For practical implementations, it is recommended that Type 1 PSEs support Type 2, 3, 4 I_{unb} requirements.
					3 % × I_{Peak}	2, 3, 4	
21	Alternative B detection backoff time	T_{dbo}	s	2.00		1, 2, 3, 4	
22	Output capacitance during detection state over a pairset	C_{out}	µF		0.520	1, 2, 3, 4	
23	Detection timing	T_{det}	s		0.500	1, 2, 3, 4	Time to complete detection of a PD.
24	Error delay timing	T_{ed}	s	0.750		1, 2, 3, 4	Delay before PSE may attempt subsequent powering after power removal because of error condition.

[1]A Type 3 PSE that is limited to class 3 power may use Type 1 values for I_{cable} and V_{pse} min. A Type 3 PSE that is limited to class 4 power may use Type 2 values for I_{cable} and V_{pse} min.
[2] Item 17 and 17a apply to PSEs that implement MPS detection per pairset.
[3]Item 17b applies to PSEs that implement MPS detection by measuring sum of the pairset currents of the same polarity.

Editor's Note (for Table 33-11):

1. I_{con} and I_{peak} need to be addressed for Extended power case where P_{Class_PD} is very close to P_{Class}. It will result with higher currents on the pair with minimum resistance but will not change the

total 4P current. For the above parameters in extended power, we will have to add two new rows that will specify maximum current at this case. Total PSE power will not change.

2. PSE Vdiff is still under investigation. It may be changed.

3. I_{cut} min values (K_I_{cut3} and K_I_{cut4}) are subject to final E2EP2P_Iunb/Runb results after conducting statistical analysis (if required) which will result with lower values. The current values are derived from worst case analysis model.

4. The following case needs to be addressed: If PSE is using active or passive pair-to-pair current balancing circuitry, K_I_{cut3} or K_I_{cut4} may be lower (down to 0.5) per equation TBD.

5. Information to be added to item 9 for Type 3 and Type 4 that I_{lim} min value is including E2EP2P_Iunb/Runb.

6. To address a T_{lim_max} that is not shown in Figure 33-14.

7. I_{lim} min and I_{cut} is specified per class to allow for cost effective designs (avoid forcing transformers to support high I_{lim} on a system that supports lower class levels only). This same concept will apply to I_{con} and I_{con-2P} per class. Comments will be submitted to address this for I_{con} and I_{con-2P}.

8. E2EP2P_Iunb is the highest (~30%) on the pairs were we don't sense the current and lower on the pair we sense current (~15%). While specifying the PSE port current capacity per the highest P2P_Iunb is the correct approach (which we already did), it is worth to consider if I_{lim} and I_{cut} need to be calculated per the pairs with highest unbalance or per the pairs with lower unbalance. The reason for this question is: I_{cut} and I_{lim} values are set to much higher values than the actual current measure due to much higher P2P_UNB. As a result the actual I_{lim} protection will be activated ~11.1% above Type 4 maximum power. The solution is: I_{cut}, I_{peak}, I_{lim} will be allowed to be decreased if PSE Rmax and Rmin are increased by a small constant resistance per equation TBD which is actually what happened in the negative pairs. To be discussed in the group.

33.2.7.1 Output voltage in the POWER_ON state

Change text of Section 33.2.7.1 as follows:

The specification for V_{PSE} in Table 33–11 shall be met with a (I_{Hold} max × V_{PSE} min) t o P_{Type} min load step at a rate of change of at least 15 mA/µs. The voltage transients as a result of loa d changes up to 35 mA/µs shall be limited to 3.5 V/µs max.

A PSE in the POWER_ON state may remove power from ~~the PI~~ a pairset when the~~ PI~~ pairset voltage ndonger meets the V_{PSE} specification.

A Type 3 or Type 4 PSE that is connected to a class 0-4 single-signature PD and is in the POWER_ON state may transition between 2-pair and 4-pair power at any time, including after the expiration of T_{pon}.

33.2.7.2 Voltage transients

Change text of Section 33.2.7.2 as follows:

A Type 2, Type 3, and Type 4 PSE shall maintain an output voltage no less than K_{Tran_lo} below V_{PSE} min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.7.7.

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows a Type 1 or Type ~~2~~ the PD to operate for any input voltage transien t lasting less than 30 µs. Transients lasting more than 250 µs shall meet the V_{PSE} specification.

33.2.7.3 Power feeding ripple and noise

Change text of Section 33.2.7.3 as follows:

The specification for power feeding ripple and noise in Table 33–11 shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{PSE} min) to P_{Type} min for PSEs a t static operating V_{PSE}. The limits are meant to preserve data integrity. To meet EMI standards, lowe r values may be needed. For higher frequencies, see 33.4.4, and 33.4.5 ~~and~~ 33.4.6.

33.2.7.4 Continuous output current capability in the POWER_ON state

Change the text of 33.2.7.4 as follows:

PSEs shall meet I_{Con} as specified in Table 33–11. Type 3 and Type 4 PSEs when connected to a single-signature PD shall meet I_{Con-2P} as specified in Table 33-11 item 4a.

~~_~~ I_{Con} is the total current of both pairs with the same polarity that a PSE has to support. I_{Con-2P} is the maximum current the PSE is required to support over one of the pairs of same polarity under E2EP2PRunb condition in the POWER_ON state. In addition to I_{Con} and I_{Con-2P} as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of V_{Port_PSE}:

I_{Peak} minimum for T_{CUT} minimum and 5 % duty cycle minimum, where

$$I_{Peak} = 1 + K\left(\left\{ \frac{V_{PSE\text{-}2P} - \sqrt{V_{PSE\text{-}2P}^2 - 4(R_{Chan})(P_{Peak\_PD\text{-}2P})}}{2(R_{Chan})} \right\}_A \right) \qquad (33\text{–}4)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.423

R_{Chan} is the channel loop resistance ~~as defined in 33.1.4~~; this parameter has a worst-case value of R_{Ch}~~.~~ R_{Ch} is defined in Table 33–1

$P_{Peak\_PD\text{-}2P}$ is the peak power a PD may draw per pairset for its class; see Table 33–18. For classes 5 to 8, $P_{Peak\_PD\text{-}2P}$ is calculated as $P_{Peak\_PD\text{-}2P} = 0.5 * P_{Peak\_PD}$

K is the ratio between I_{Peak} due to system end to end pair-to-pair current unbalance effect and I_{Peak} of a system with perfect system end to end pair to pair balance in Type 3 and Type 4 systems. K=0 for two pair systems (Type 1 and Type 2 systems). The value of K which is based on curve fit and is dimensionless, for a Type 3 and Type 4 system that operates as 4-pair system is given by Equation (33–4a).

$$K = \begin{cases} min(0.1882 \times R_{chan}^{-0.337}, 0.28) & \text{for Type 3} \\ min(0.1777 \times R_{chan}^{-0.329}, 0.26) & \text{for Type 4} \end{cases} \qquad (33\text{–}4a)$$

Insert Section 33.2.7.4a and Section 33.2.7.4b after section 33.2.7.4 as follows:

33.2.7.4.1 PSE PI pair-to-pair resistance and current unbalance

Type 3 and Type 4 PSEs operating over 4-pair are subject to unbalance requirements in this section. The contribution of PSE PI pair-to-pair effective resistance unbalance (PSE_P2PRunb) to the whole effective system end to end resistance unbalance (E2EP2PRunb), is specified by PSE maximum (R_{Pair_max}) and minimum (R_{Pair_min}) common mode effective resistance in the powered pairs of same polarity.

The PSE_P2PRunb determined by R_{Pair_max} and R_{Pair_min} ensures that along with any other parts of the system - i.e. channel (cables and connectors) and the PD, the maximum pair current due to E2EP2PRunb, is not exceeding I_{con-2P} as defined in Table 33–11 during normal operating conditions. I_{con-2P} maximum is the average pair current due to E2EP2PRunb that is higher than I_{con} specified in Table 33–11. I_{con-2P} maximum is specified for total channel common mode pair resistance from 0.1 Ω to 12.5 Ω. For channels with common mode pair resistance lower than 0.1 Ω, see guidelines in Annex 33A.

R_{Pair_max} and R_{Pair_min} are specified and measured under maximum P_{Class} sourcing conditions. Conformance with Equation (33–4b) shall be met for R_{Pair_max} and R_{Pair_min}.

$$R_{Pair\_max} = \left\{ \begin{array}{ll} k1 \times R_{Pair\_min} + a1 & \text{for class 5} \\ 1.894 \times R_{Pair\_min} - 0.053 & \text{for class 6} \\ k2 \times R_{Pair\_min} + a2 & \text{for class 7} \\ 1.760 \times R_{Pair\_min} - 0.042 & \text{for class 8} \end{array} \right\}_{\Omega} \quad (33\text{–}4b)$$

where

R_{Pair_max} is the maximum PSE common mode effective resistance in the powered pairs of same polarity.

R_{Pair_min} is the minimum PSE common mode effective resistance in the powered pairs of same polarity.

The values of R_{Pair_max} and R_{Pair_min} are implementation specific and need to satisfy Equation (33–4b).

Editor's Note: k1, k2, a1 and a2 in Equation (33-4b) will be added in D1.3

33.2.7.4.2 Test setup and test conditions for R_{Pair_max} and R_{Pair_min}

See Annex 33A.

33.2.7.5 Output current in POWER_UP mode

Editor's Note: Timing requirements for 4-pair power to be added to this section.

Change the text of 33.2.7.5 as follows:

POWER_UP mode occurs on each pairset between the PSE's transition to the POWER_UP state on that pairset and either the expiration of T_{Inrush} or the conclusion of PD inrush currents on that pairset (see 33.3.7.3). Type 3 and Type 4 PSEs that apply power to both pairsets when connected to a single-signature PD shall reach POWER_ON on both pairsets within T_{Inrush} max, starting with the first pairset transitioning into the POWER_UP state. ~~However, for practical implementations, it is recommended that the POWER_UP mode on a pairset persist for the complete duration of T_{Inrush_2P}, as the PSE may not be able to~~

~~correctly ascertain the conclusion of a PD's inrush behavior.~~ See legacy_powerup variable in section 33.2.4.4 for more information on the POWER_UP to POWER_ON transition.

The PSE shall limit the maximum current sourced ~~at the PI~~ per pairset during POWER_UP. The maximum inrush current sourced by the PSE per pairset shall not exceed the per pairset ~~PSE~~ inrush template in Figure 33–13 and Equation (33–5).

a) During POWER_UP, for ~~PI~~ pairset voltages between 0 V and 10 V, the minimum $I_{Inrush\text{-}2P}$ requirement is 5 mA.
b) During POWER_UP, for ~~PI~~ pairset voltages between 10 V and 30 V, the minimum $I_{Inrush\text{-}2P}$ requirement is 60 mA.
c) During POWER_UP, for ~~PI~~ pairset voltages above 30 V, the minimum $I_{Inrush\text{-}2P}$ requirement is as specified in Table 33–11.
d) For Type 1 PSE, measurement of minimum $I_{Inrush\text{-}2P}$ requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses 1-Event Physical Layer classification, and requires the 1 ms settling time, shall power up a class 4 PD as if it used ~~2~~Multiple-Event Physical Layer classification.

Replace Figure 33-13 with the following:

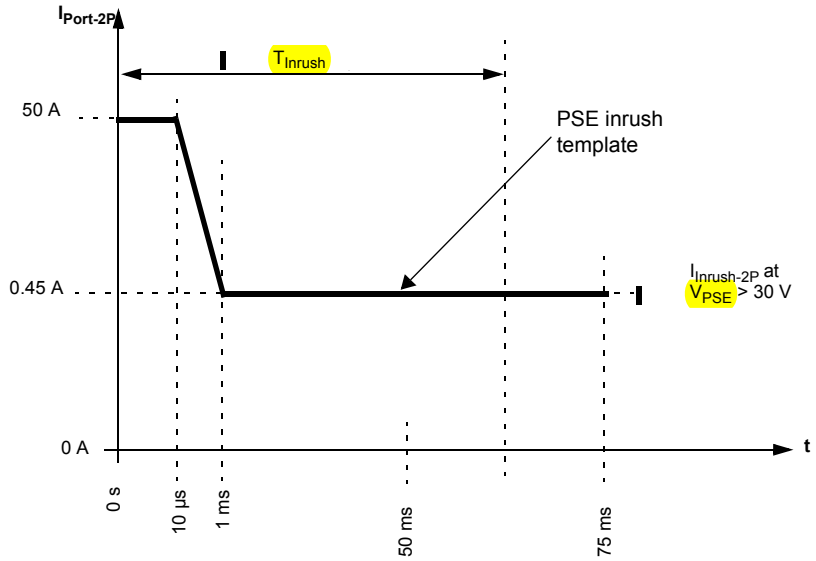


Figure 33–13—$I_{Inrush\text{-}2P}$ current and timing limits, per pairset in POWER_UP

The PSE inrush template is defined by the following segments:

$$\text{PSE inrush template} = \left\{ \begin{array}{ll} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ 50.0 - \dfrac{(t - 10.0\times10^{-6}) \times 49.6}{0.990\times10^{-6}} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ 0.450 & 0.001 \le t < 0.075 \end{array} \right\}_{A} \quad (33\text{–}5)$$

where

t is the time in seconds

33.2.7.6 Overload current

Change the text of 33.2.7.6 as follows:

If $I_{Port\text{-}2P}$, the current supplied per pairset by the PSE to the PI, exceeds I_{CUT} for longer than T_{CUT}, the PSE may remove power from the ~~PIthat~~ pairset. The cumulative duration of T_{CUT} is measured with a sliding window of at least 1 second width.

The I_{CUT} threshold may equal the I_{Peak} value determined by Equation (33–4).

33.2.7.7 Output current—at short circuit condition

Change the text of Section 33.2.7.7 as follows:

A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33–14. Power shall be removed from ~~the~~ a pairset ~~PI~~ of a PSE before the pairset ~~PI~~ current exceeds the "PSE upperbound template" in Figure 33–14. When connected to a single signature PD, a Type 3 or Type 4 PSE should (TBD) remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

Replace Figure 33-14 with the following:.

The maximum value of I_{LIM} is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template is defined by the following segments:

$$\text{PSE upperbound template} = \left\{ \begin{array}{ll} 50.0 & \text{for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\dfrac{K}{t}} & \text{for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 & \text{for } (8.20\times10^{-3} \le t < T_{\text{cut-2Pmax}}) \\ I_{\text{lim min}} & \text{for } T_{\text{cut max}} \le t(\quad) \end{array} \right\}_{A} \quad (33\text{–}6)$$

where

t is the duration in seconds that the PSE sources $I_{Port\text{-}2P}$

K is 0.025 A^2s, an energy limitation constant for the ~~port~~ pairset current when it is not in steady state normal operation

$T_{\text{cut max}}$ is T_{CUT} max per pairset, as defined in Table 33–11

$I_{\text{lim min}}$ is I_{LIM} min per pairset, as defined in Table 33–11

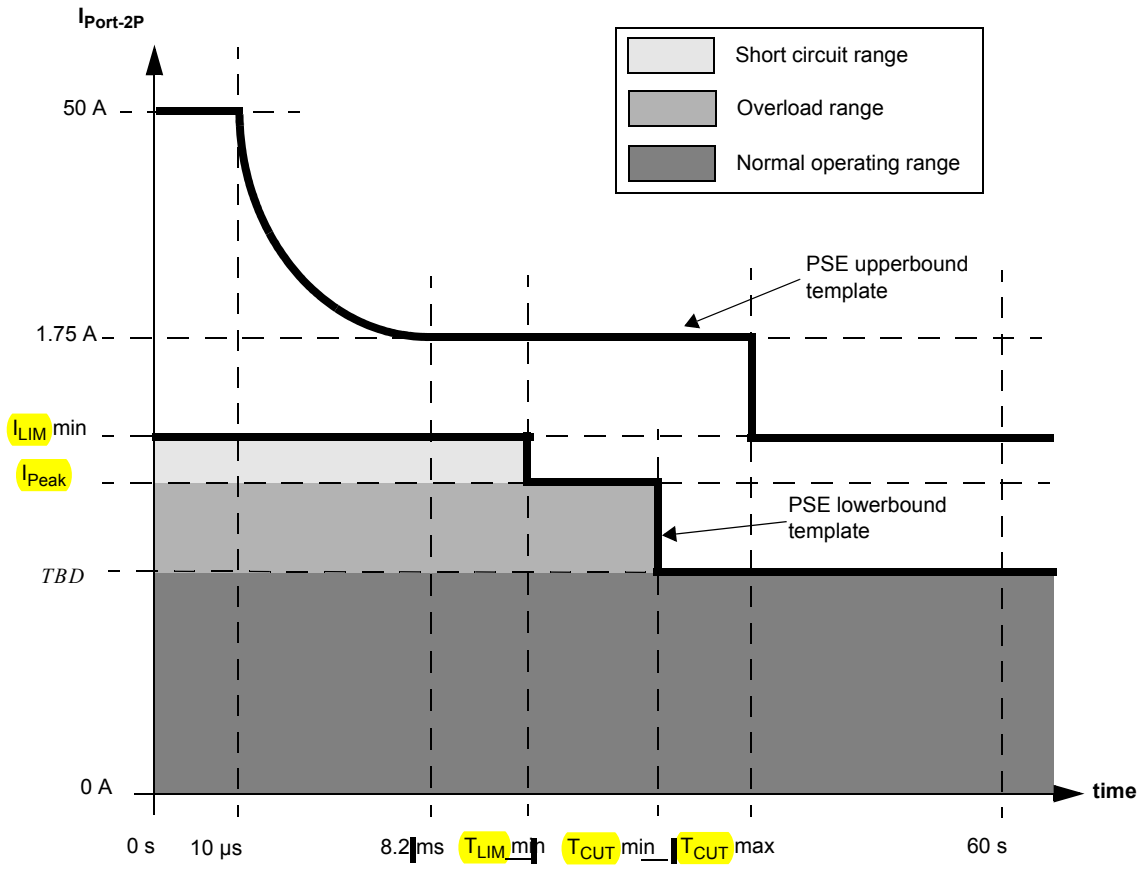


Figure 33–14—POWER_ON state, per pairset operating current templates

The PSE shall limit ~~the~~ a pairset current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the ~~PI~~ pairset. The cumulative duration of T_{LIM} may be measured with a sliding window.

The PSE lowerbound template is defined by the following segments:

$$\text{PSE lowerbound template} = \left\{ \begin{array}{ll} I_{LIM\text{-}2Pmin} & \text{for } (0 \le t < T_{lim\text{-}2Pmin}) \\ I_{Peak\text{-}2P} & \text{for } (T_{lim\text{-}2Pmin} \le t < T_{cut\text{-}2Pmin}) \\ TBD & \text{for } (T_{cut\text{-}2Pmin} \le t) \end{array} \right\}_{A} \quad (33\text{–}7)$$

where

I_{LIM_min} is the I_{LIM} min value per pairset for the PSE (see Table 33–11)

t is the duration that the PI sources $I_{Port\text{-}2P}$

T_{lim_min} is T_{LIM} min per pairset as defined in Table 33–11

T_{cut_min}	is T_{CUT} min per pairset, as defined in Table 33–11
I_{Peak}	is I_{Peak} per pairset, as defined in Equation (33–4)
~~P_{Class}~~	~~is P_{Class}, as defined in Table 33–7~~
~~V_{PSE}~~	~~is the voltage at the PSE PI~~

If a short circuit condition is detected on a pairset, power removal from ~~the PI~~ that pairset shall begin withi n T_{LIM} as specified in Table 33–11. If $I_{Port-2P}$ exceeds the PSE lowerbound template, the PSE outpu t voltage may drop below V_{PSE} min.

A PSE in the POWER_ON state may remove power from a pairset without regard to T_{LIM} when the pairset voltage no longer meets the V_{PSE} specification.

33.2.7.8 Turn off time

Change text in section 33.2.7.8 as follows:

The specification for T_{Off} in Table 33–11 shall apply to the discharge time from V_{PSE} to V_{Off} of a pairset with a test resistor of 320 kΩ attached to that pairsetthe ~~PI. In~~ addition, it is recommended that th e pairset ~~PI~~ be discharged when turned off. T_{Off} starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered variable is cleared (see Figure 33–9). T_{Off} ends when $V_{PSE} \leq V_{Off}$ max. The PSE remains in the IDLE state as long as the average voltage across the pairset ~~PI~~ is below V_{Off} max. The IDLE state is the state when the PSE is not in detection, classification, or normal powering states.

33.2.7.9 Turn off voltage

The specification for V_{Off} in Table 33–11 shall apply to the PI voltage in the IDLE State.

33.2.7.10 Continuous output power capability in POWER_ON state

Change text of Section 33.2.7.10 as follows:

P_{Class} is the class power defined in 33.2.6 and Equation (33–3), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss.

P_{Con} is valid over the range of V_{PSE} defined in Table 33–11. Measurement of P_{Con} should be averaged using any sliding window with a width of 1 s.

A PSE may remove power from a PD that causes the PSE to source more than P_{Class}.

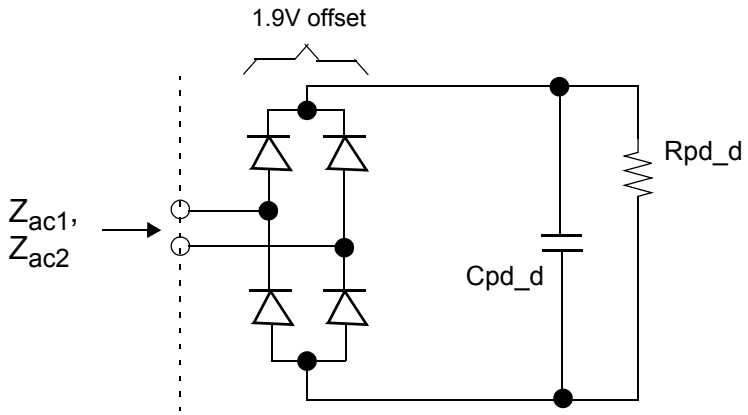
Editor's Note: Effects of single and dual-signature PDs to be considered.

Change title and text of Section 33.2.7.11 as follows:

33.2.7.11 intra-pair ~~C~~current unbalance

The specification for I_{unb} in Table 33–11 shall apply to the current unbalance between the two conductors of a power pair over the current load range.

Type 2, Type 3 and Type 4 Endpoint PSEs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).



NOTE—Rpd_d and Cpd_d are specified in Table 33–19. Cpd_d may be located either in parallel with Z_{ac1} or as shown above.

Figure 33–15—Z_{ac1} and Z_{ac2} definition as indicated in Table 33–12

Editor's Note: Yair to review AC MPS for 4-pair.

Change text in section 33.2.9.1.2 as follows:

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if $I_{Port\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ on both pairsets of the same polarity is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if $I_{Port\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ on both pairsets of the same polarity is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if $I_{Port\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ on both pairsets of the same polarity is in the range of I_{Hold}.

The values of $I_{Port\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ on both pairsets of the same polarity and the corresponding values of I_{Hold} shall meet the conditions specified in Table 33–11.

A Type 3 or 4 PSE, when connected to a single-signature PD, shall monitor either the sum of $I_{port\text{-}2P}$ of both pairsets of the same polarity or the pairset with the highest $I_{Port\text{-}2P}$ current value and use the appropriate I_{Hold} level shown in Table 33–11. Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

A Type 3 or 4 PSE, when connected to a dual-signature PD shall monitor each pairset and use the appropriate I_{Hold} level shown in Table 33-11. The PSE shall remove power from any pairset on which the DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when $I_{Port\text{-}2P}$ or the sum of $I_{Port\text{-}2P}$ of both pairsets of the same polarity is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every T_{MPS} + T_{MPDO}, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Change variable pse_dll_power_type as follows:

pse_dll_power_level~~type~~

A control variable output by the PD power control state diagram (Figure 33–28) that indicates the ~~type~~ power level of the PSE by which the PD is being powered.

Values:1: The PSE is delivering class 3 power or less ~~a Type 1 PSE~~ (default).

2: The PSE is delivering class 4 power.~~a Type 2 PSE.~~

3: The PSE is delivering class 5 or class 6 power.

4: The PSE is delivering class 7 or class 8 power.

Change variable pse_power_type as follows:

pse_power_level~~type~~

A control variable that indicates to the PD the level of power the PSE is supplying.~~the type of PSE by which it is being powered.~~

Values:1: The PSE is delivering the PD's requested power or Class 3 power, whichever is less ~~a Type 1 PSE~~.

2: The PSE is delivering the PD's requested power or Class 4 power, whichever is less ~~a Type 2 PSE~~.

3: The PSE is delivering the PD's requested power or Class 6 power, whichever is less.

4: The PSE is delivering the PD's requested power or Class 8 power, whichever is less.

V_{PD}

Voltage at the PD PI as defined in 1.4.422.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

Change the timer tpowerdly_timer as follows:

tpowerdly_timer

A timer used to prevent the Type 2, 3, or 4 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.

Insert 33.3.3.4a after 33.3.3.4 as follows:

33.3.3.4a Functions

do_class_timing

This function is used by a Type 3 or Type 4 PD to evaluate the type of PSE connected to the link by measuring the length of the classification event. The classification event timing requirements are defined in Table 33–17. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.

Values: TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

Table 33–17a—Autoclass PD timing requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Autoclass signature timing	T_{ACS}	ms	75.5	84.5	Measured from transition to state CLASS_EV1
2	Autoclass power draw start time	T_{AUTO_PD1}	s		1.35	Measured from when V_{Port_PD} rises above V_{Port_PD} min
3	Autoclass power draw end time	T_{AUTO_PD2}	s	3.28		Measured from when V_{Port_PD} rises above V_{Port_PD} min

The default value of pse_power_level~~type~~ is 1. After a successful ~~2~~Multiple-Event Physical Layer classification has completed the pse_power_level is set to either 2, 3, or 4.~~or~~ After a successful Data Link Layer classification has completed, the pse_power_level~~type~~ is set to either 1, 2, 3 or 4.

The PD resets the pse_power_level~~type~~ to '1' when the PD enters the DO_DETECTION state.

33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Change Table 33-18 as follows:

Editor's Note: Input average power for class 5 is rounded off from 39.94W to 40W.

33.3.7.1 Input voltage

Change text of Section 33.3.7.1 as follows:

The specification for V_{PD} in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD} = V_{PSE} - (R_{Chan} \times I_{Port\text{-}2P})$. For Dual-signature PDs, Vpd specs shall be met on each pairset.
The PD shall turn on at a voltage less than or equal to V_{On_PD}. After the PD turns on, the PD shall stay o n over the entire V_{PD} range. The PD shall turn off at a voltage less than V_{PD} minimum and greate r than or equal to V_{Off_PD}.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V_{PSE} min to V_{PSE} max (as defined in Table 33–11) with a series resistance within the range of valid Channel Resistance.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage per pairset, Class 1	V_{PD}	V	~~37.0~~42.1	57.0	1, 3	See 33.3.7.1, Table 33–1
	Input voltage per pairset, Class 2			~~42.5~~40.8		~~2~~1, 3	
	Input voltage per pairset, Class 0, 3			37.0		1, 3	
	Input voltage per pairset, Class 4			42.5		2, 3	
	Input voltage per pairset, Class 5, Single-signature			44.3		3	
	Input voltage per pairset, Class 5, Dual-signature			41.1		4	
	Input voltage per pairset, Class 6			42.5		3	
	Input voltage per pairset, Class 7			42.9		4	
	Input voltage per pairset, Class 8			41.2		4	
2	Transient operating input voltage per pairset	(deleted)	V	36.0		2, 3, 4	For time duration defined in 33.2.7.2
3	Input voltage range per pairset during overload	(deleted)	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2, 3	
				39.5	57.0	4	
4	Input available average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1, 3	See 33.3.7.2, Table 33–1
	Input available average power, Class 1				3.84	1, 3	
	Input available average power, Class 2				6.49	1, 3	
	Input available average power, Class 4				25.5	2, 3	
	Input available average power, Class 5, Single-signature				40.0	3	
	Input available average power, Class 5, Dual-signature				35.5	4	
	Input available average power, Class 6				51.0	3	
	Input available average power, Class 7				62.0	4	
	Input available average power, Class 8				71.0	4	

Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
5	Input inrush current per pairset	I_{Inrush_PD-2P}	A		0.400	1, 2, 3, 4	Peak value—See 33.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2, 3, 4	See 33.3.7.3 Single-signature PDs only
6a	Inrush to operating state delay per pairset	T_{delay}	s	0.080		3, 4	Dual-signature PDs only
7	Peak operating power, Class 0 and Class 3	P_{Peak_PD}	W		14.4	1, 3	See 33.3.7.4
	Peak operating power, Class 1				5.00	1, 3	
	Peak operating power, Class 2				8.36	1, 3	
	Peak operating power, Class 4				$1.11 \times P_{Class\_PD}$	2, 3	
	Peak operating power, Class 5				$1.05 \times P_{Class\_PD}$	3, 4	
8	Input current transient (absolute value)		mA/µs		4.70	1, 2, 3, 4	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		1, 2, 3, 4	See 33.3.7.6, 33.3.7.3
10	Ripple and noise, < 500 Hz	V_{pp}			0.500	1, 2, 3, 4	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
11	~~a)~~ PD Power supply turn on voltage	V_{On_PD}	V		42.0	1, 2, 3, 4	See 33.3.7.1
	~~b)~~ PD power supply turn off voltage	V_{Off_PD}	V	30.0		1, 2, 3, 4	
12	PD classification stability time	T_{class}	s		0.005	1, 2, 3, 4	See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80	1, 2, 3, 4	See 33.3.7.9

33.3.7.2 Input average power

Change text of section 33.3.7.2 as follows:

The maximum average power, P_{Class_PD} in Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6. PDs may also adjust their maximum required operating power below P_{Class_PD} by using Autoclass (see 33.3.5.3).

NOTE—Average power is calculated using any sliding window with a width of 1 s.

For Class 6 or Class 8 PDs, the input available average power is the maximum power the PD shall consume when no additional information is available to the PD regarding actual channel DC resistance. If such a PD has additional information and does not cause the PSE to source more than P_{Class} it may exceed the maximum input available average power.

33.3.7.2.1 System stability test conditions during startup and steady state operation

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–9):

$$P_{Port\_PD} = \{V_{Port\_PD} \times I_{Port}\}_W \quad (33–9)$$

where

P_{Port_PD}	is the average input power at the PD PI
V_{Port_PD}	is the static input voltage at the PD PI
I_{Port}	is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Replace first paragraph of Section 33.3.7.3 with the following:

Inrush current per pairset is drawn beginning with the application of input voltage at the pairset complian t with V_{PD} requirements as defined in Table 33–18, and ending before T_{Inrush} min per Table 33–11. After T_{Inrush} min, the PD shall meet P_{Class_PD} as specified in Table 33–18.

Change second, third and fourth paragraph of Section 33.3.7.3 as follows:

Type 2, Type 3 and Type 4 PDs with pse_power_level~~type~~ state variable set to 2, 3 and 4 respectively prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} for each pairset starts when V_{PD-2P} crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from $I_{Inrush-2P}$ to I_{LIM}.

Input inrush current at startup is limited by the PSE if C_{Port} per pairset < 180 µF, as specified in Table 33–11.

If C_{Port} per pairset ≥ 180 µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} per pairset max is satisfied.

Insert the following note at the end of section 33.3.7.3 as follows:

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches99% of steady state or after Tinrush min. See 33.2.7.4 for details.

C_{port} in Table 33–18 is the total PD input capacitance during POWER UP and POWER ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, C_{port} value requirements are specified in 33.2.7.6. See PSE-PD simplified C_{port} implementation model in Annex TBD.

33.3.7.4 Peak operating power

Change text in section 33.3.7.4 as follows:

(Voverload text removed - remove from Table 33-18 also?)

At any static voltage at the PI, and any PD operating condition, with the exception of class 6 or class 8 PDs, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 an d 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

For class 6 and class 8 PDs in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Class} at the PSE PI for more than T_{CUT} min, as defined in Table 33–11 and with 5% duty cycle.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max, or P_{Class} at the PSE PI for class 6 and class 8 PDs.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

$$I_{Port} = \{\sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2}\}_A \quad (33–10)$$

where

I_{Port}	is the RMS input current
I_{Port_dc}	is the DC component of the input current
I_{Port_ac}	is the RMS value of the AC component of the input current

The maximum I_{Port} value for all PDs except those in class 6 or class 8, over the operating V_{PD} range shall be defined by Equation (33–11) ~~the following equation~~:

Replace Equation 33-11 with the following:

$$I_{portmax} = \left\{\frac{P_{Class\_PD}}{V_{Port\_PD\text{-}2P}}\right\}_A \quad (33–11)$$

where

$I_{portmax}$	is the maximum DC and RMS input current
V_{PD}	is the ~~static input voltage~~ minimum specified input voltage at ~~the~~ a PD pairset~~PI~~
P_{Class_PD}	is the maximum power, P_{Class_PD} max, as defined in Table 33–18

The maximum I_{Port} value for all PDs in class 6 or class 8, over the operating V_{PD} range shall be defined by Equation (33–11a):

Replace Figure 33-18 with the following figure:

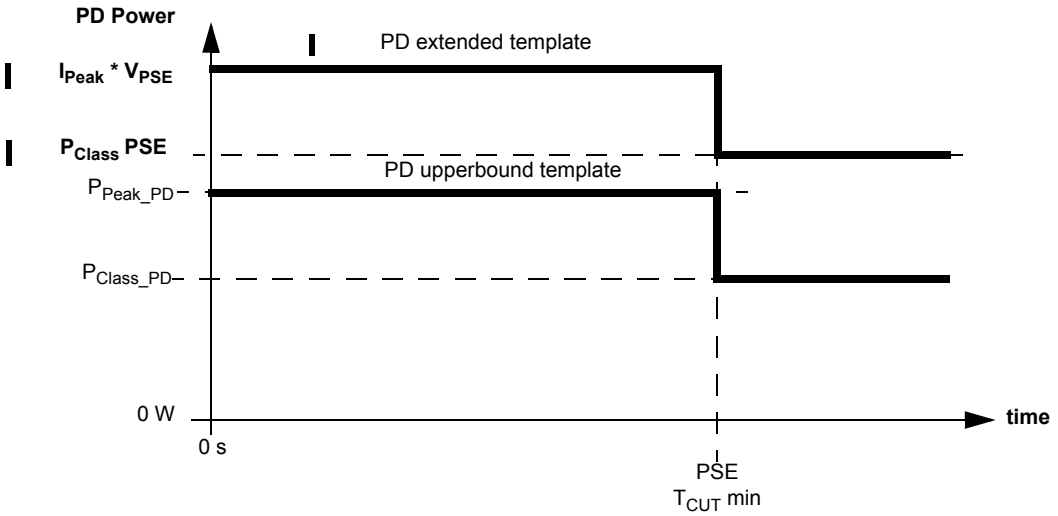


Figure 33–18—PD static operating mask

The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–13):

$$P_{\text{PDUT}}(t) = \left\{ \begin{array}{ll} P_{\text{Peak\_PD}} & \text{for } (0 \le t < T_{\text{cutmin}}) \\ P_{\text{Class\_PD}} & \text{for } (T_{\text{cutmin}} \le t) \end{array} \right\}_{\text{W}} \qquad (33\text{–}13)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
$P_{\text{Peak\_PD}}$	is the peak operating power, $P_{\text{Peak\_PD}}$ max, as defined in Table 33–18
$P_{\text{Class\_PD}}$	is the maximum power, $P_{\text{Class\_PD}}$ max, as defined in Table 33–18 is
T_{cutmin}	T_{CUT} min, as defined in Table 33–11

Insert Equation 33-13a after equation 33-13 as follows:

The PD extended template in Figure 33-18, P_{PDET}, is described by Equation (33-13a):

$$P_{\text{PDET}}(t) = \left\{ \begin{array}{ll} I_{\text{Peak}} \times V_{PSE} & \text{for } (0 \le t < T_{\text{cutmin}}) \\ P_{\text{Class}} & \text{for } (T_{\text{cutmin}} \le t) \end{array} \right\}_{\text{W}} \qquad (33\text{–}13a)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
I_{Peak}	is the peak operating current, I_{Peak} max, as defined in Equation (33–4)
V_{PSE}	is the voltage at PSE.
P_{Class}	is the minimum power output by the PSE, as defined in Table 33-7 and Section 33.2.6
T_{cutmin}	is T_{CUT} min, as defined in Table 33–11

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least T_{LIM} min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

Change text in section 33.3.7.6 as follows:

Editor's Note:

1. Type 3 and Type 4 to be added (to parts other than the newly added first paragraph).

2. A drop out specification needs to be added to this section that requires PDs to ride out PSE transients. This is in place of increasing Cport.

Type 1, Type 2, and single-signature Type 3 PDs with classes 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9. Type 3 dual-signature PDs with class 0 to 4 shall meet the requirement for Cport as defined in Table 33–18 item 9 for each pairset. For class 5 and 6 single-signature PDs, if $C_{Port\_min} \geq 10\mu F$, transient behavior has no further requirements. For dual-signature class 5 PDs, this recommendation applies to each pairset. For class 7 and 8 single signature PDs, if CPort_min ≥ 20μF, transient behavior has no further requirements. See 33.2.7.2 (TBD) or the transient conditions

A Type 1 PD with input capacitance of 180 μF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 μF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 PD shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/μs, a source impedance of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance is R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI I_{LIM} per Equation (33–14).

Change equation 33-14 as follows:

The current limit per pairset at the MDI (MDI I_{LIM}) is defined by Equation (33–14):

$$\{pse_{ILIM\text{-}2Pmin}\}_{mA} < \{mdi_{ILIM\text{-}2P}\}_{mA} \leq \{pse_{ILIM\text{-}2Pmin}\}_{mA} + 5.00 \qquad (33\text{–}14)$$

where

pse_{ILIM_min} is the PSE I_{LIM} min as defined in Table 33–11
mdi_{ILIM} is the per pairset current limit at the MDI (MDI I_{LIM})

33.3.7.7 Ripple and noise

Change first paragraph of Section 33.3.7.7 as follows:

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of V_{PD}, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

33.3.7.8 PD classification stability time

Following a valid detection and a rising voltage transition from V_{valid} to V_{Class}, the PD Physical Layer classification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed V_{bfd} max as specified in Table 33–18. When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed V_{bfd} max.

Insert new section 33.3.7.10 and section 33.3.7.10.1 after section 33.3.7.9 as follows:

33.3.7.10 PD PI pair-to-pair resistance and current unbalance

All Class 5 and higher PDs shall not exceed I_{con-2P} (Table 33–11, item 4a) on either pairset when tested according to section 33.3.7.10.1.

See Annex 33A for design guide lines for meeting the above requirements.

33.3.7.10.1 Test setup and test conditions for PD PI pair-to-pair resistance and current unbalance

The test setup described in Figure 33–18a and its test conditions (shown in Table 33–18a) shall be used to verify that the requirements in section 33.3.7.10 are met.

Table 33–18a—Test conditions and test requirements for PD PI pair-to-pair current unbalance and resistance unbalance test setup

Item	Parameter	Unit	Value	Additional Information
1	Vin	V	$V_{Port\_PSE\text{-}2P}$ min	
2	R_{pair_min}	Ω	0.16±1%	
3	R_{pair_max}	Ω	0.19±1%	
4	PD power	W	Set to maximum per its class	

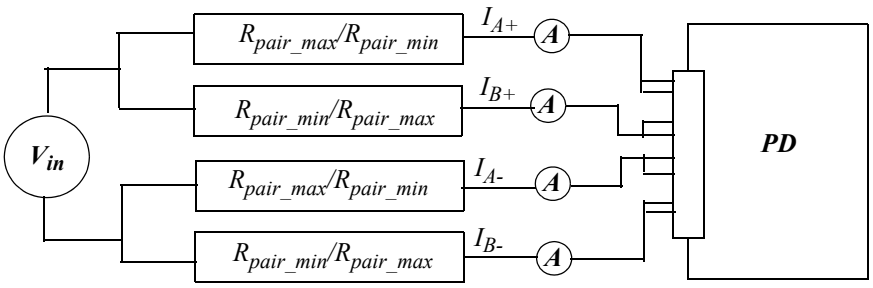


Figure 33–18a—PI fault tolerance test circuit

R_{pair_max} and R_{pair_min} represents PSE and channel effective source impedance that includes the effect of $V_{Port\_PSE\_diff}$ as specified by Table 33–11 item 1a.

Change 33.3.8 as follows:

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall consist of current draw equal to or above I_{port_MPS} for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}. The values of I_{port_MPS}, T_{MPS_PD}, and T_{MPDO_PD} are shown in Table 33–19a. A Type 1 or Type 2 PD, or a PD which does not detect a long first class event, shall in addition show the input impedance with resistive and capacitive components defined in Table 33–19.

Types 3 and 4 PDs which detect a long first class event in the range of T_{LCF_PD} may reduce T_{MPS_PD} in order to draw a lower standby MPS power. In absence of a long first class event the minimum T_{MPS_PD} is higher, and the standby MPS power is also higher.

A Type 3 or Type 4 PD shall have T_{MPS_PD} measured with a series resistance representing the worst case cable resistance between the measurement point and the PD PI.

5) Repeat for I_3, I_4.

6) Verify that the current unbalance in each case does not exceed $I_{con\text{-}2P}$ minimum in Table 33–11 item 4a.

Verification of $I_{con\text{-}2P}$ in step 6 confirms PSE conformance to Equation (33–4b).

33A.10Channel resistance with less than 0.1Ω

$I_{cont\_2P\_unb}$ max is specified for total channel common mode pair resistance from 0.1Ω to 12.5Ω and worst case unbalance contribution by a PD. When the PSE is tested for channel common mode resistance less than 0.1 Ω, i.e. 0 Ω <R_{ch_x} <0.1 Ω, the PSE shall be tested with (R_{load_min} - R_{ch_x}) and (R_{load_max} - R_{ch_x}).

Editor's Note: To consider the value of adding informative section to present R_{load_max} and R_{load_min} equation derivation and values.